Correlating On Extended Data Lengths with the HSP45256

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Correlations of data sets longer than the maximum length of the HSP45256 are implemented in one of two ways. The first method is to use multiple correlator chips in the manner shown in the HSP45256 data sheet. This will perform a classical correlation on data sets up to 4096 samples of one bit data with no external logic. The limitation on the number of samples is the 16 stage programmable delay register. The advantage of this method is that the user will be guaranteed of finding the data set that best matches the reference no matter where that set lies in the data stream.

The second method involves using external logic to perform a piecewise correlation. The data and reference are each divided into blocks of N samples, and the data is processed block by block. By reloading the reference memory while processing, the correlation can be carried out at the full data rate while using fewer correlators than would be necessary with the first method. This method will work for any length data sets, but the user must have an initial estimate of the offset between the data and the reference. The true correlation peak will only be found if the data and the corresponding reference fall within the same block. If this block is longer than 256 samples, then multiple correlators are used.

A block diagram of a circuit to perform correlation with a 512 sample reference is shown in Figure 1. The reference is divided into two blocks; the first block is loaded into the reference memory prior to data being sent into the part. The correlation of the data with the current block of the reference is calculated with the HSP45256; as each correlation score comes out, it is stored in the HSP9501, which is set for a delay of 256 clocks. The output of the HSP9501 is sent to the cascade input of the HSP45256 such that the correlation score for each sample in the current block is added to the score from the corresponding sample of the previous block. While the first block is being processed, the reference for the second block is being loaded into the shadow registers of the reference memory of the HSP45256. At the end of the first block, the TXFR# line is pulsed to load the shadow registers into the operating reference memory, and correlation of the second block takes place. At the end of the second block, the HSP9501 will contain the correlation scores for the entire set of data. This method will work up to the highest correlation score that can be stored in the 10 bit data word of the HSP9501: 2^{10} - 1, or 1023. See Figure 2 for an example of data that has been processed by the circuit shown. This method could be extended to 8191 samples by using two HSP9501's in parallel to store the full 13 bit output of the Correlator. For longer correlations, an external adder would be necessary. Figure 3 is a block diagram for a circuit with a maximum correlation score of 2^{20} - 1.

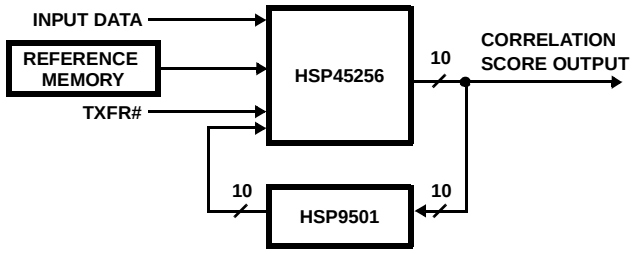

FIGURE 1. CORRELATION OF LENGTH UP TO 1023

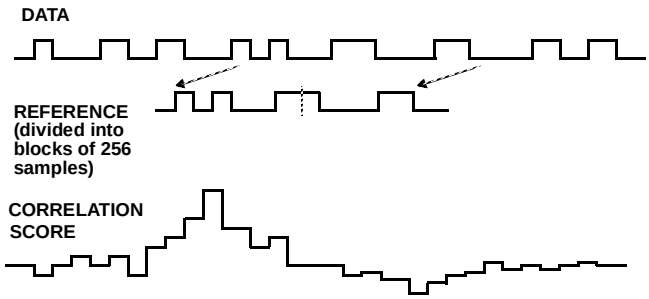

FIGURE 2. CORRELATION RESULTS

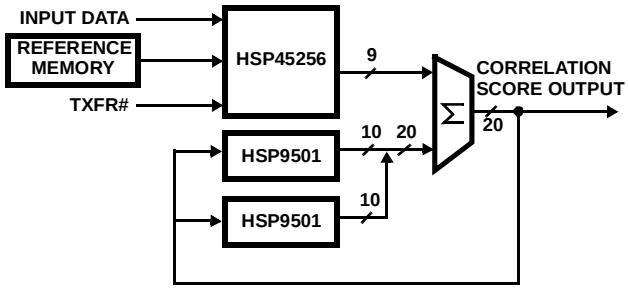

FIGURE 3. CORRELATION OF LENGTH GREATER THAN 8191

Figure 4 shows an implementation of a M tap correlation where the uncertainty in the data alignment is greater than 256 samples. The reference is divided into blocks and the correlation is performed one block at a time. The results of these partial correlations are then added to form a piecewise correlation. The amount of hardware required depends on the length of the correlation desired and the initial misalignment of the data. The total delay in the HSP9501's is set for a delay of one block of data; the correlators compute the correlation score for one block of data at a time, where one correlator is needed for every 256 samples in the block.

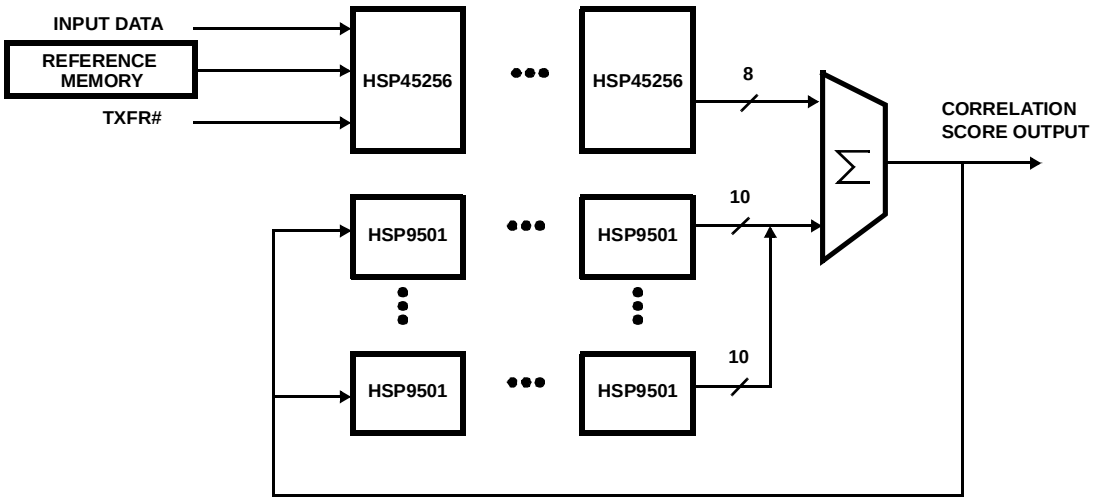

FIGURE 4. LONG CORRELATION WITH LARGE DATA/REFERENCE MISALIGNMENT

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