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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74HC668/HD74HC669

Synchronous UP/Down Decade Counter Synchronous Up/Down 4-bit binary Counter



ADE-205-520 (Z)

1st. Edition

Sep. 2000

Description

This synchronous presettable decade counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters.

A buffered clock input triggers the four master-slave flip-flops on the rising (positive going) edge of the clock waveform. This counter is fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count enable inputs and a carry output. Both count enable inputs (\bar{P} and \bar{T}) must be low to count. The direction of the count is determined by the level of the up/down input. when the input is high, the counter counts up; when low, it counts down. Input \bar{T} is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable \bar{P} or \bar{T} inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transission-line effects, thereby simplifying system design. This counter features a fully independent clock circuit. Changes at control inputs (enable \bar{P} , Enable \bar{T} , load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

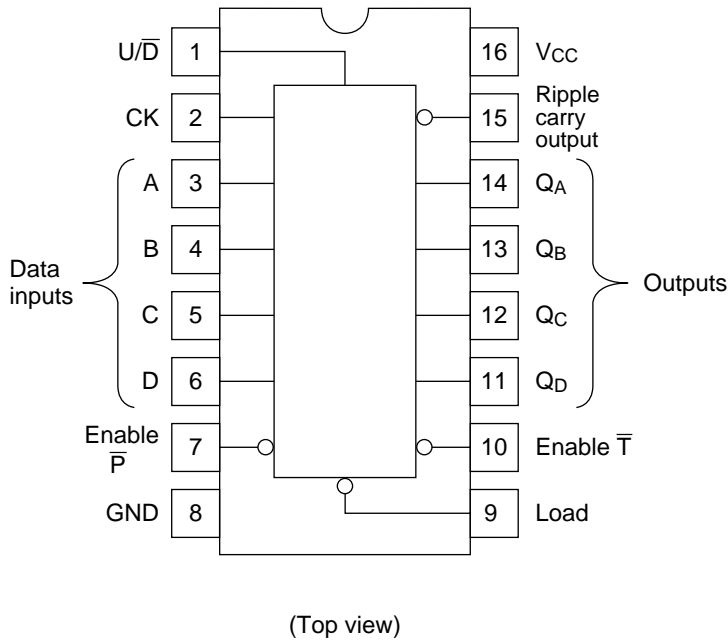
- High Speed Operation
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μA max

HD74HC668/HD74HC669

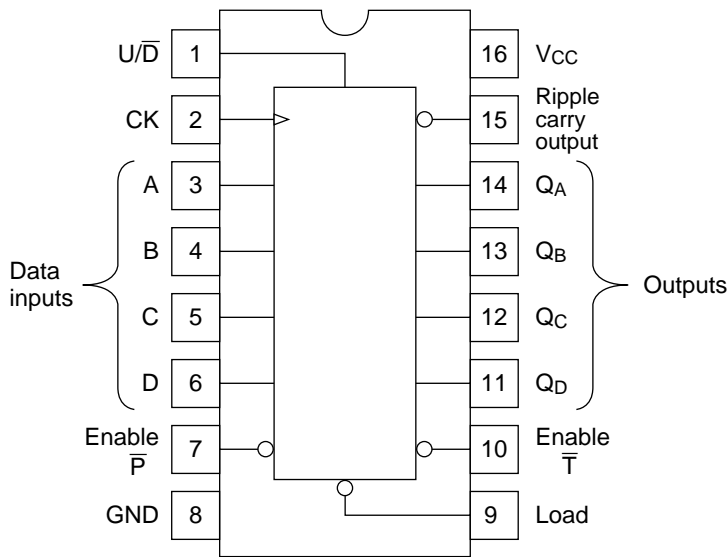
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)

Pin Arrangement

HD74HC668



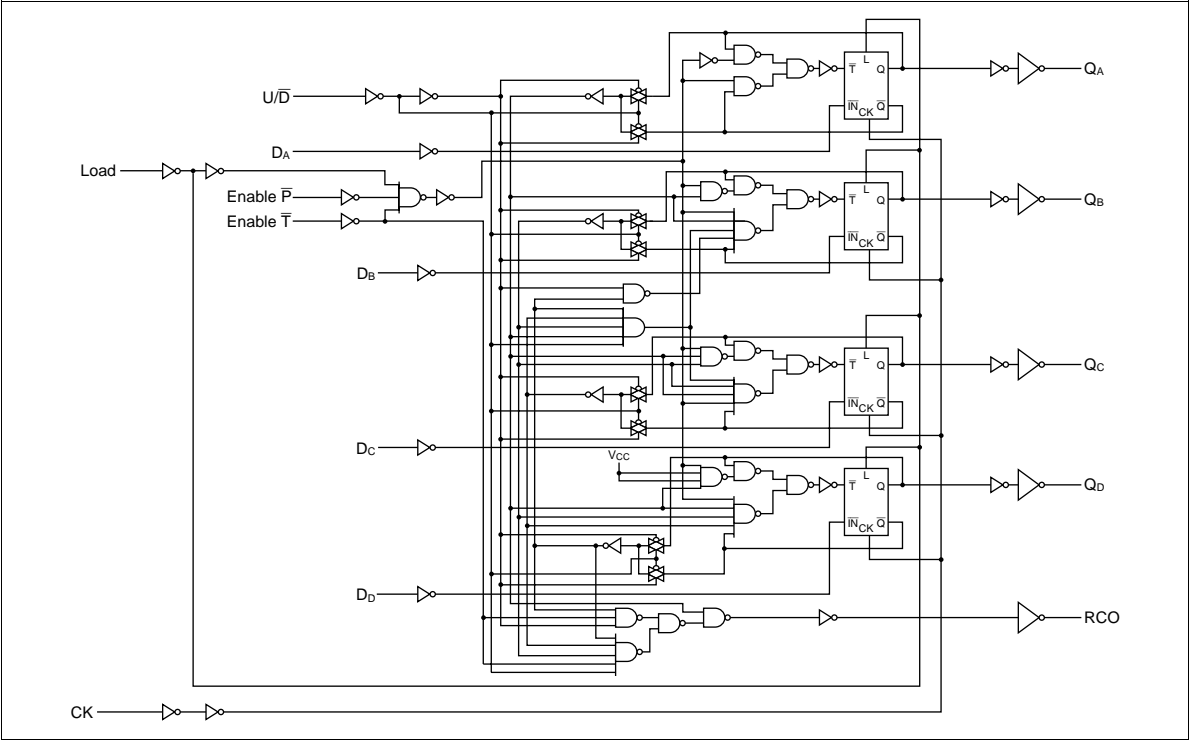
HD74HC669



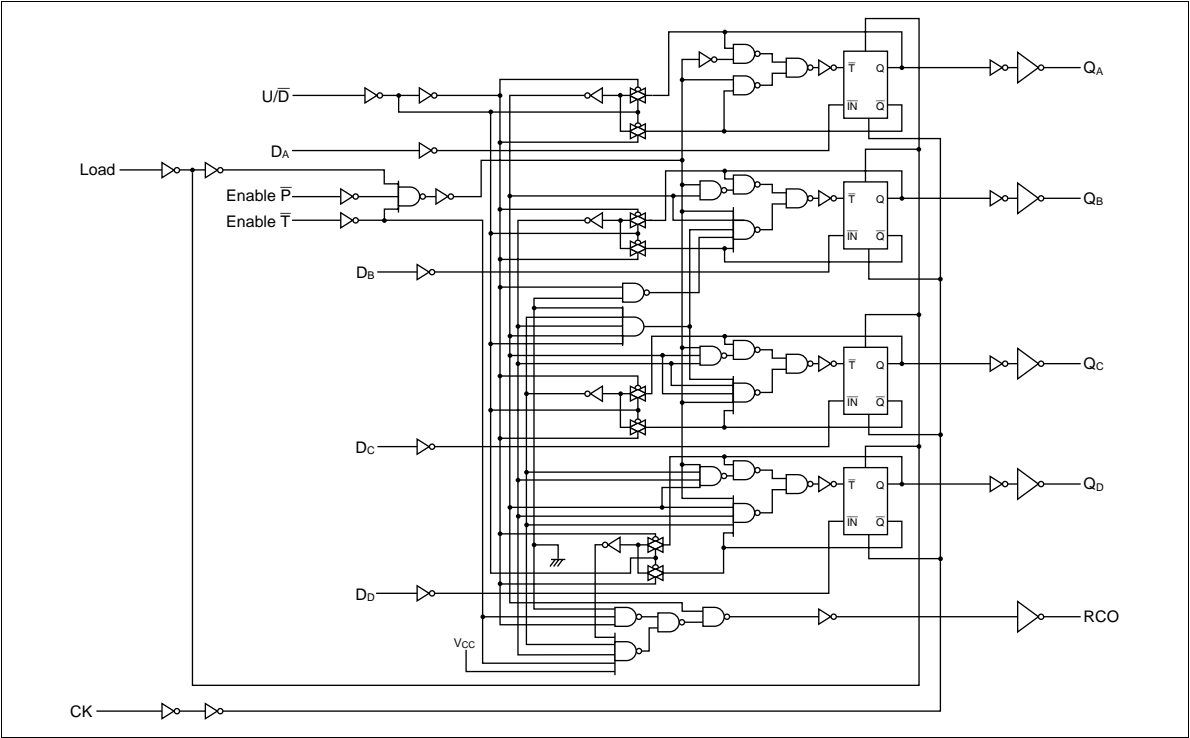
(Top view)

Logic Diagram

HD74HC668

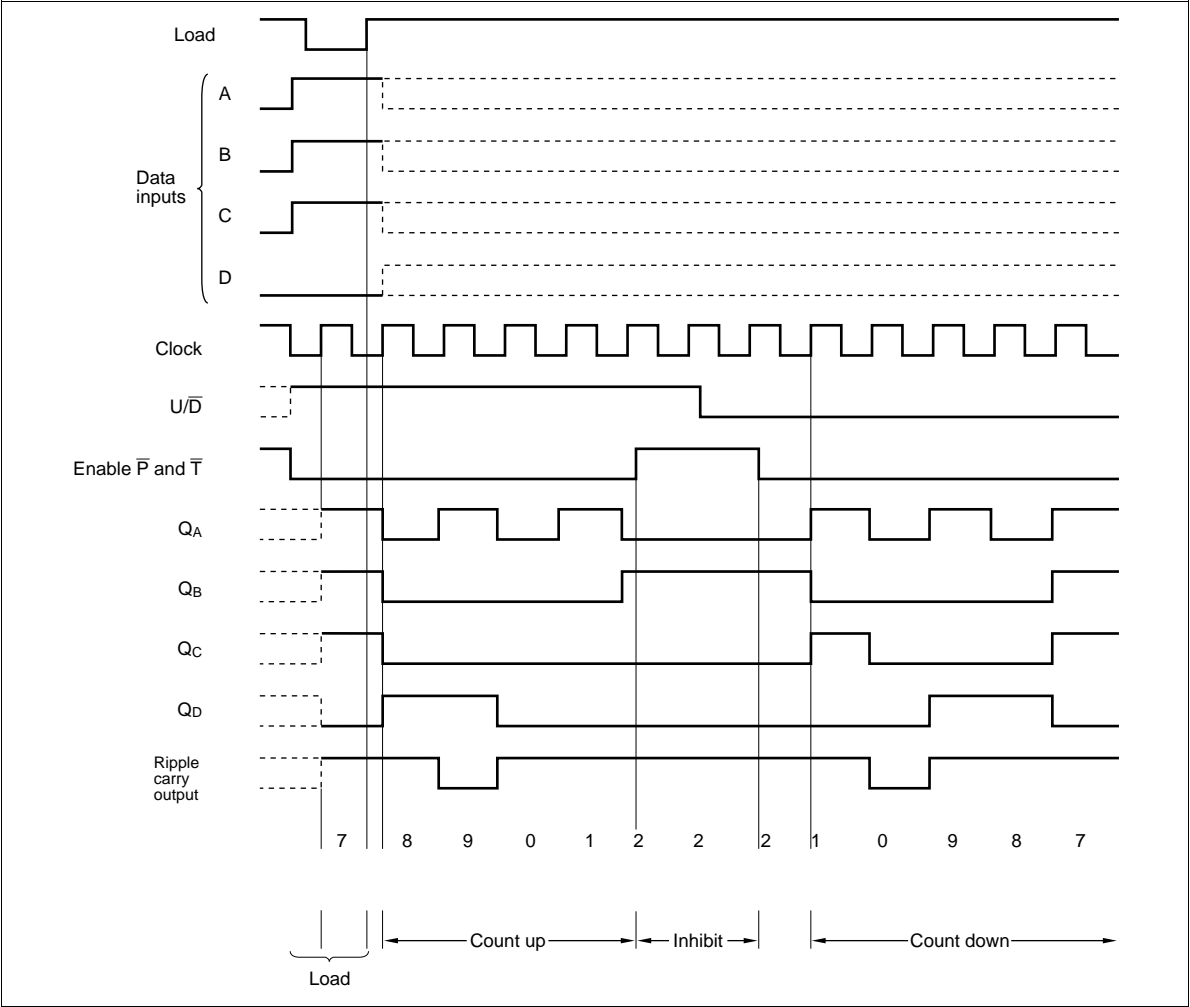


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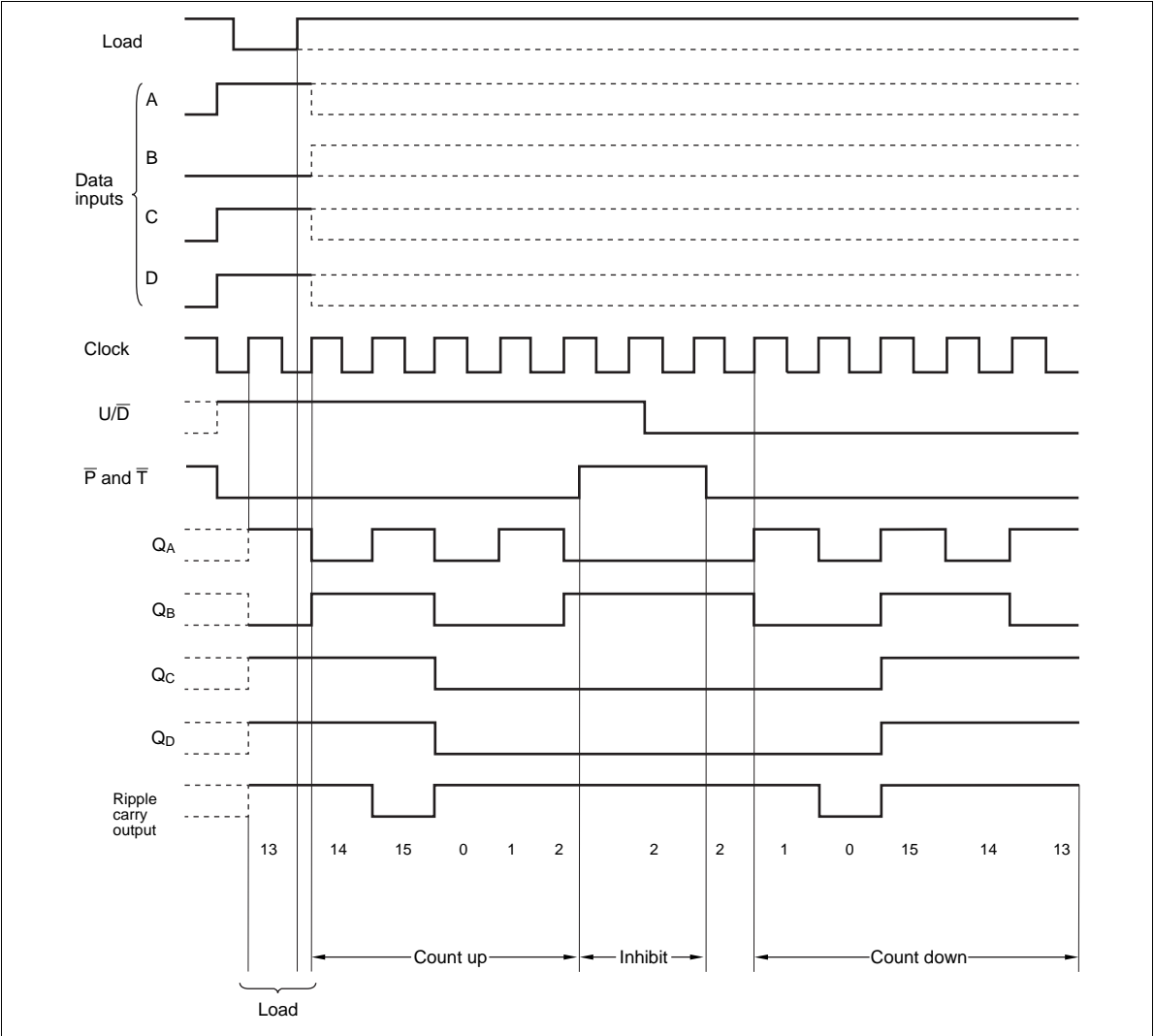


Timing Chart

HD74HC668



HD74HC669



DC Characteristics

| Item | Symbol | V _{CC} (V) | Ta = 25°C | | | Ta = -40 to +85°C | | Unit | Test Conditions | |
|--------------------------|-----------------|---------------------|-----------|-----|------|-------------------|------|------|---|---------------------------|
| | | | Min | Typ | Max | Min | Max | | | |
| Input voltage | V _{IH} | 2.0 | 1.5 | — | — | 1.5 | — | V | | |
| | | 4.5 | 3.15 | — | — | 3.15 | — | | | |
| | | 6.0 | 4.2 | — | — | 4.2 | — | | | |
| | V _{IL} | 2.0 | — | — | 0.5 | — | 0.5 | V | | |
| | | 4.5 | — | — | 1.35 | — | 1.35 | | | |
| | | 6.0 | — | — | 1.8 | — | 1.8 | | | |
| Output voltage | V _{OH} | 2.0 | 1.9 | 2.0 | — | 1.9 | — | V | Vin = V _{IH} or V _{IL} I _{OH} = -20 μA | |
| | | 4.5 | 4.4 | 4.5 | — | 4.4 | — | | | |
| | | 6.0 | 5.9 | 6.0 | — | 5.9 | — | | | |
| | | 4.5 | 4.18 | — | — | 4.13 | — | | | I _{OH} = -4 mA |
| | | 6.0 | 5.68 | — | — | 5.63 | — | | | I _{OH} = -5.2 mA |
| | V _{OL} | 2.0 | — | 0.0 | 0.1 | — | 0.1 | V | Vin = V _{IH} or V _{IL} I _{OL} = 20 μA | |
| | | 4.5 | — | 0.0 | 0.1 | — | 0.1 | | | |
| | | 6.0 | — | 0.0 | 0.1 | — | 0.1 | | | |
| | | 4.5 | — | — | 0.26 | — | 0.33 | | | I _{OL} = 4 mA |
| | | 6.0 | — | — | 0.26 | — | 0.33 | | | I _{OL} = 5.2 mA |
| Input current | I _{in} | 6.0 | — | — | ±0.1 | — | ±1.0 | μA | Vin = V _{CC} or GND | |
| Quiescent supply current | I _{CC} | 6.0 | — | — | 4.0 | — | 40 | μA | Vin = V _{CC} or GND, I _{out} = 0 μA | |

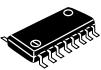
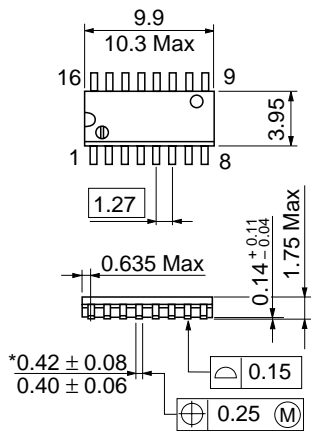
AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

| Item | Symbol | V_{CC} (V) | Ta = 25°C | | | Ta = -40 to +85°C | | Unit | Test Conditions |
|-------------------------|-----------|--------------|-----------|-----|-----|-------------------|-----|------|---------------------------------------|
| | | | Min | Typ | Max | Min | Max | | |
| Maximum clock Frequency | f_{max} | 2.0 | — | — | 5 | — | 4 | MHz | |
| | | 4.5 | — | — | 27 | — | 21 | | |
| | | 6.0 | — | — | 32 | — | 25 | | |
| Propagation delay time | t_{PLH} | 2.0 | — | — | 200 | — | 250 | ns | Clock to Ripple carry out |
| | | 4.5 | — | — | 40 | — | 50 | | |
| | | 6.0 | — | — | 34 | — | 43 | | |
| | t_{PHL} | 2.0 | — | — | 225 | — | 280 | ns | Clock to Q |
| | | 4.5 | — | — | 45 | — | 56 | | |
| | | 6.0 | — | — | 38 | — | 48 | | |
| | t_{PLH} | 2.0 | — | — | 150 | — | 190 | ns | Enable \bar{T} to Ripple carry out |
| | | 4.5 | — | — | 30 | — | 38 | | |
| | | 6.0 | — | — | 26 | — | 33 | | |
| | t_{PHL} | 2.0 | — | — | 200 | — | 250 | ns | U/\bar{D} to Ripple carry out |
| | | 4.5 | — | — | 40 | — | 50 | | |
| | | 6.0 | — | — | 34 | — | 43 | | |
| Pulse width | t_w | 2.0 | 80 | — | — | 100 | — | ns | |
| | | 4.5 | 16 | — | — | 20 | — | | |
| | | 6.0 | 14 | — | — | 17 | — | | |
| Setup time | t_{su} | 2.0 | 100 | — | — | 125 | — | ns | Data to Clock |
| | | 4.5 | 20 | — | — | 25 | — | | |
| | | 6.0 | 17 | — | — | 21 | — | | |
| | t_{su} | 2.0 | 150 | — | — | 190 | — | ns | Enable \bar{P} , \bar{T} to Clock |
| | | 4.5 | 30 | — | — | 38 | — | | |
| | | 6.0 | 26 | — | — | 33 | — | | |
| | t_{su} | 2.0 | 150 | — | — | 190 | — | ns | Loadk to Clock |
| | | 4.5 | 30 | — | — | 38 | — | | |
| | | 6.0 | 26 | — | — | 33 | — | | |
| | t_{su} | 2.0 | 150 | — | — | 190 | — | ns | U/\bar{D} to Clock |
| | | 4.5 | 30 | — | — | 38 | — | | |
| | | 6.0 | 26 | — | — | 33 | — | | |

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns) (cont)

| Item | Symbol | V _{cc} (V) | Ta = 25°C | | | Ta = -40 to +85°C | | Unit | Test Conditions |
|-----------------------|--------------------------------------|---------------------|-----------|-----|-----|-------------------|-----|------|-----------------|
| | | | Min | Typ | Max | Min | Max | | |
| Hold time | t _h | 2.0 | 5 | — | — | 5 | — | ns | |
| | | 4.5 | 5 | — | — | 5 | — | | |
| | | 6.0 | 5 | — | — | 5 | — | | |
| Output rise/fall time | t _{TLH} t _{THL} | 2.0 | — | — | 75 | — | 95 | ns | |
| | | 4.5 | — | 5 | 15 | — | 19 | | |
| | | 6.0 | — | — | 13 | — | 16 | | |
| Input capacitance | C _{in} | — | — | 5 | 10 | — | 10 | pF | |

Unit: mm



*Dimension including the plating thickness
Base material dimension

| | |
|------------------------|----------|
| Hitachi Code | FP-16DN |
| JEDEC | Conforms |
| EIAJ | Conforms |
| Mass (reference value) | 0.15 g |

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

| | | |
|-----|--------------|---|
| URL | NorthAmerica | : http://semiconductor.hitachi.com/ |
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For further information write to:

Hitachi Semiconductor
(America) Inc.

179 East Tasman Drive,
San Jose, CA 95134

Tel: <1> (408) 433-1990

Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic Components Group

Dornacher Straße 3
D-85622 Feldkirchen, Munich

Germany

Tel: <49> (89) 9 9180-0

Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.

Electronic Components Group.

Whitebrook Park

Lower Cookham Road

M Maidenhead

Berkshire SL6 8YA, United Kingdom

Tel: <44> (1628) 585000

Fax: <44> (1628) 585160

Hitachi Asia Ltd.

Hitachi Tower

16 Collyer Quay #20-00,

Singapore 049318

Tel: <65>-538-6533/538-8577

Fax: <65>-538-6933/538-3877

URL: <http://www.hitachi.com.sg>

Hitachi Asia Ltd.

(Taipei Branch Office)

4/F, No. 167, Tun Hwa North Road,

Hung-Kuo Building,

Taipei (105), Taiwan

Tel: <886>-(2)-2718-3666

Fax: <886>-(2)-2718-8180

Telex: 23222 HAS-TP

URL: <http://www.hitachi.com.tw>

Hitachi Asia (Hong Kong) Ltd.

Group III (Electronic Components)

7/F., North Tower,

World Finance Centre,

Harbour City, Canton Road

Tsim Sha Tsui, Kowloon,

Hong Kong

Tel: <852>-(2)-735-9218

Fax: <852>-(2)-730-0281

URL: <http://www.hitachi.com.hk>