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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74HC592

8-bit Register/Binary Counter

ADE-205-513 (Z)
1st. Edition
Sep. 2000

Description

The HD74HC592 consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive edge-triggered clocks. In addition, the counter has direct load and clear functions. Expansion is easily accomplished by connecting $\overline{RCO}$ of the first stage to the count enable of the second stage, etc.

Features

- High Speed Operation: t_{pd} (CCK to $\overline{RCO}$) = 24 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max (Ta = 25°C)

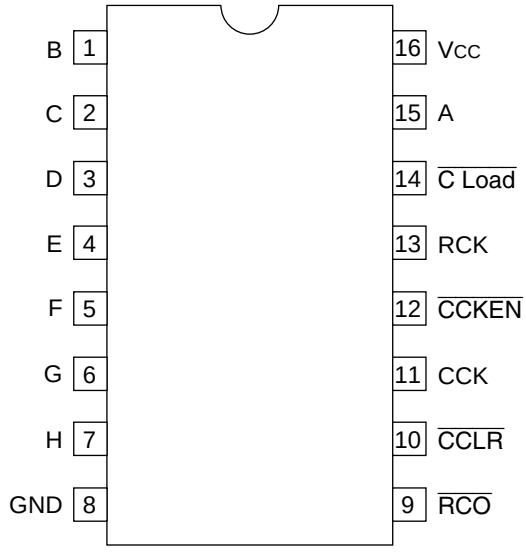
Function Table

Inputs

RCK	$\overline{CLoad}$	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	Function
X	L	H	X	X	Regiater data loaded into counter
X	H	L	X	X	Counter clear
⎍	H	H	X	X	Input data A to H stored into register
⎺_	H	H	X	X	No change in register
X	H	H	L	⎍	Count up
X	H	H	L	⎺_	No count
X	H	H	H	X	No cont

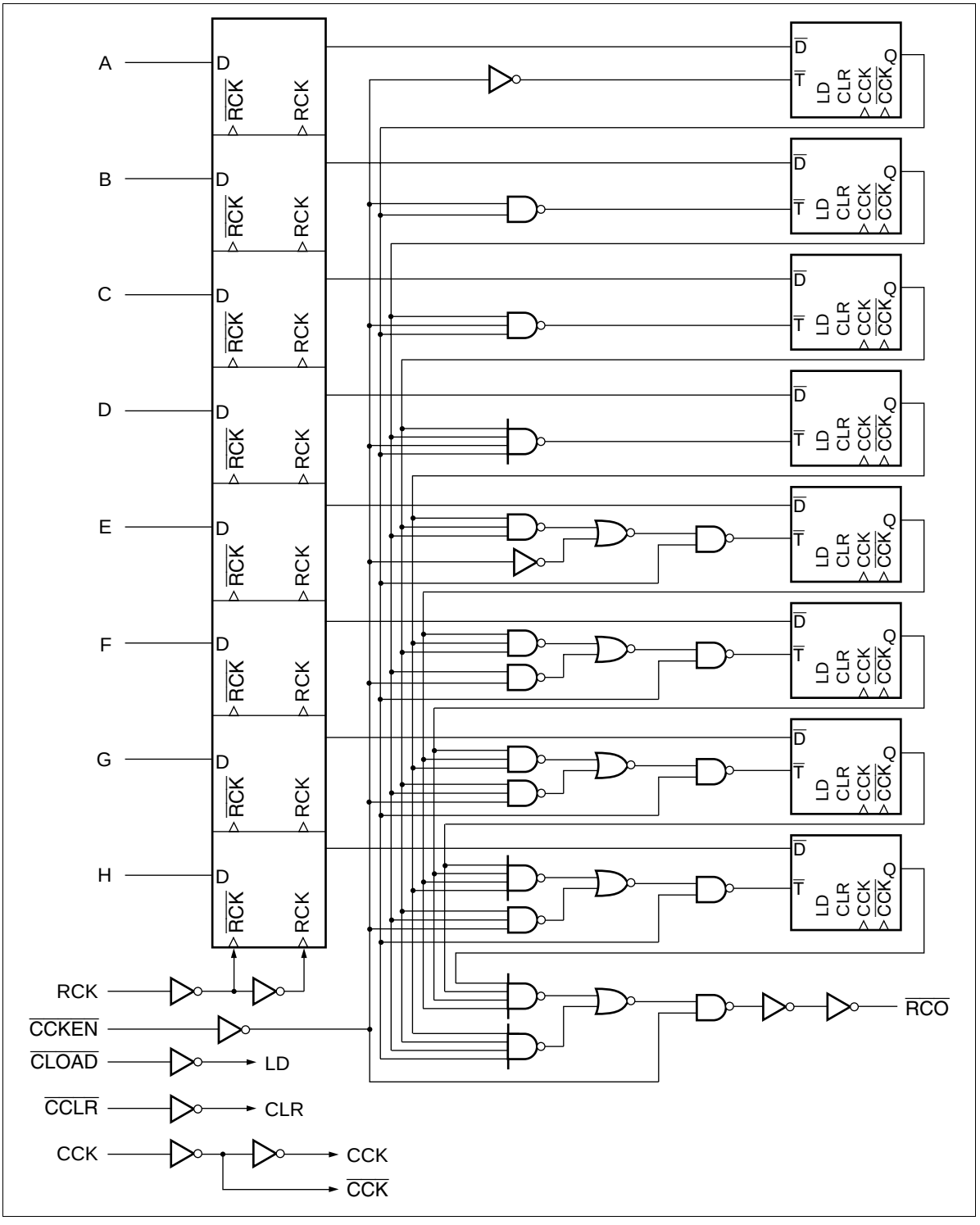
$\overline{RCO}$ = $\overline{QA' \cdot QB' \cdot QC' \cdot QD' \cdot QE' \cdot QF' \cdot QG' \cdot QH' \cdot (\overline{CCKEN})}$ (QA' to QH': Output of Internal Counter)

Pin Arrangement



(Top view)

Logic Diagram



DC Characteristics

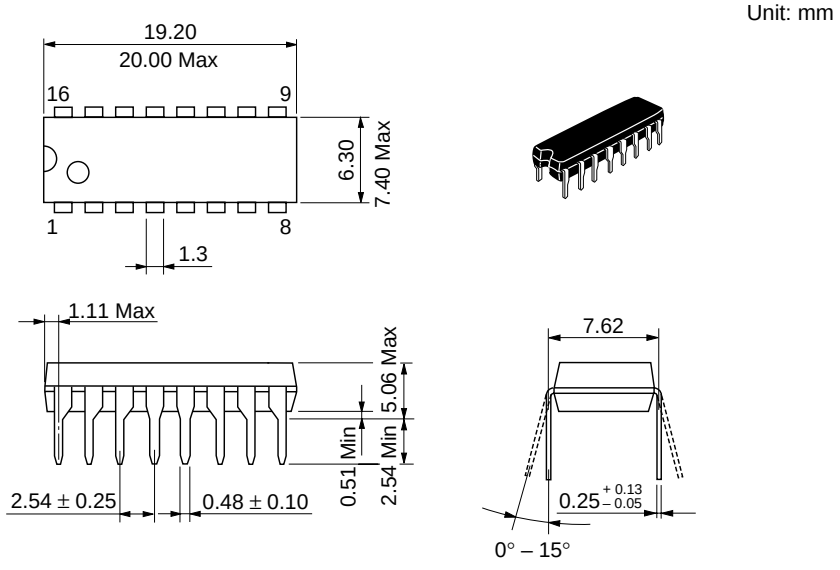
Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions	
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	CCK to $\overline{RCO}$
		4.5	—	24	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	$\overline{C\ Load}$ to $\overline{RCO}$
		4.5	—	27	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH}	2.0	—	—	200	—	250	ns	$\overline{CCLR}$ to $\overline{RCO}$
		4.5	—	26	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH} t_{PHL}	2.0	—	—	300	—	375	ns	RCK to $\overline{RCO}$
		4.5	—	29	60	—	75		
		6.0	—	—	51	—	64		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	8	–	20	—		
		6.0	14	—	—	17	—		
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	$\overline{CCLR}$ to CCK
		4.5	20	12	—	25	—		
		6.0	17	—	—	21	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	$\overline{CCKEN}$ to CCK
		4.5	20	0	—	25	—		
		6.0	17	—	—	21	—		
		2.0	200	—	—	250	—	ns	CCK to RCK
		4.5	40	14	—	50	—		
		6.0	34	—	—	43	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

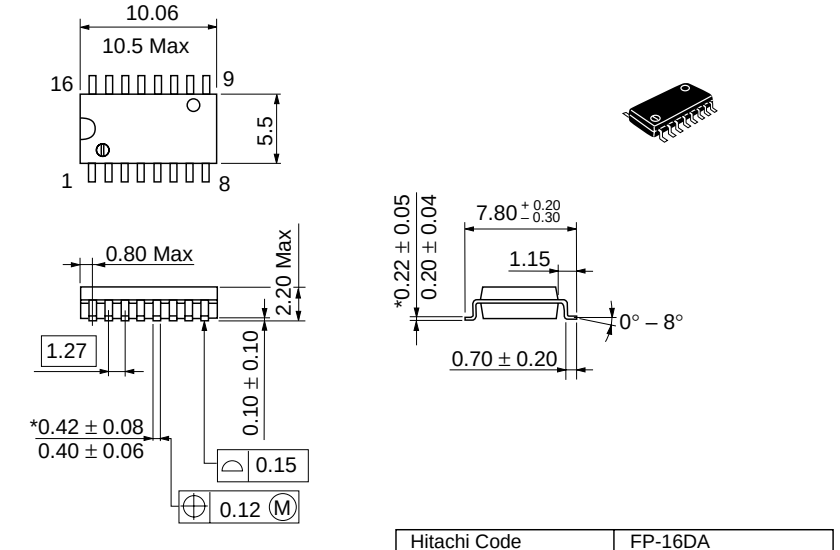
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

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