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Hitachi 16-Bit Single-Chip Microcomputer

# H8S/2128 Series, H8S/2124 Series

# H8S/2128F-ZTAT™

Hardware Manual
— Supplement —

ADE-602-114B
Rev. 3.0
5/22/02
Hitachi, Ltd.

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February 2002

# Announcement of Changes to Hardware Manual Contents

This is to announce that, with the addition of H8S/2128S and H8S/2127S products, a Supplement has been prepared for the following sections of the Hitachi single-chip microcomputer H8S/2128 Series and H8S/2124 Series Hardware Manual.

Applicable Manual:

H8S/2128 Series, H8S/2124 Series, H8S/2128F-ZTAT Hardware Manual, 2nd Edition (ADE-602-114A), published September 1999

Applicable Sections:

Section 16, $I^2C$ Bus Interface → Replaced with “Supplement, Section 16”
Sections 22–23, Electrical Characteristics → Replaced with “Supplement, Section 22”
Appendix F, Product Code Lineup → Replaced with “Supplement, Appendix F”

Semiconductor & Integrated Circuits
Hitachi, Ltd.

# Contents

# Section 16 $I^2C$ Bus Interface [Option]

A two-channel $I^2C$ bus interface is available as an option in the H8S/2128 Series. The $I^2C$ bus interface is not available for the H8S/2124 Series. Observe the following notes when using this option.

1. For mask-ROM versions, a W is added to the part number in products in which this optional function is used.

   Examples: HD6432127SWFA

2. The product number is identical for F-ZTAT versions. However, be sure to inform your Hitachi sales representative if you will be using this option.

## 16.1 Overview

A two-channel $I^2C$ bus interface is available for the H8S/2128 Series as an option. The $I^2C$ bus interface conforms to and provides a subset of the Philips $I^2C$ bus (inter-IC bus) interface functions. The register configuration that controls the $I^2C$ bus differs partly from the Philips configuration, however.

Each $I^2C$ bus interface channel uses only one data line (SDA) and one clock line (SCL) to transfer data, saving board and connector space.

### 16.1.1 Features

- Selection of addressing format or non-addressing format
  - — $I^2C$ bus format: addressing format with acknowledge bit, for master/slave operation
  - — Serial format: non-addressing format without acknowledge bit, for master operation only
- Conforms to Philips $I^2C$ bus interface ($I^2C$ bus format)
- Two ways of setting slave address ($I^2C$ bus format)
- Start and stop conditions generated automatically in master mode ($I^2C$ bus format)
- Selection of acknowledge output levels when receiving ($I^2C$ bus format)
- Automatic loading of acknowledge bit when transmitting ($I^2C$ bus format)
- Wait function in master mode ($I^2C$ bus format)
  A wait can be inserted by driving the SCL pin low after data transfer, excluding acknowledgement. The wait can be cleared by clearing the interrupt flag.

- Wait function in slave mode ($I^2C$ bus format)

  A wait request can be generated by driving the SCL pin low after data transfer, excluding acknowledgement. The wait request is cleared when the next transfer becomes possible.

- Three interrupt sources
  - Data transfer end (including transmission mode transition with $I^2C$ bus format and address reception after loss of master arbitration)
  - Address match: when any slave address matches or the general call address is received in slave receive mode ($I^2C$ bus format)
  - Stop condition detection

- Selection of 16 internal clocks (in master mode)

- Direct bus drive (with SCL and SDA pins)
  - Two pins—P52/SCL0 and P47/SDA0—(normally NMOS push-pull outputs) function as NMOS open-drain outputs when the bus drive function is selected.
  - Two pins—P24/SCL1 and P23/SDA1—(normally CMOS pins) function as NMOS-only outputs when the bus drive function is selected.

- Automatic switching from formatless mode to $I^2C$ bus format (channel 0 only)
  - Slave mode addressless (no start condition/end condition, non-addressing) operation
  - Operation using common data pin (SDA) and independent clock pin (VSYNCI, SCL) pin configuration
  - Automatic switching from formatless mode to $I^2C$ bus format on fall of SCL

### 16.1.2 Block Diagram

Figure 16.1 shows a block diagram of the $I^2C$ bus interface.

Figure 16.2 shows an example of I/O pin connections to external circuits. Channel 0 I/O pins and channel 1 I/O pins differ in structure, and have different specifications for permissible applied voltages. For details, see section 22, Electrical Characteristics.

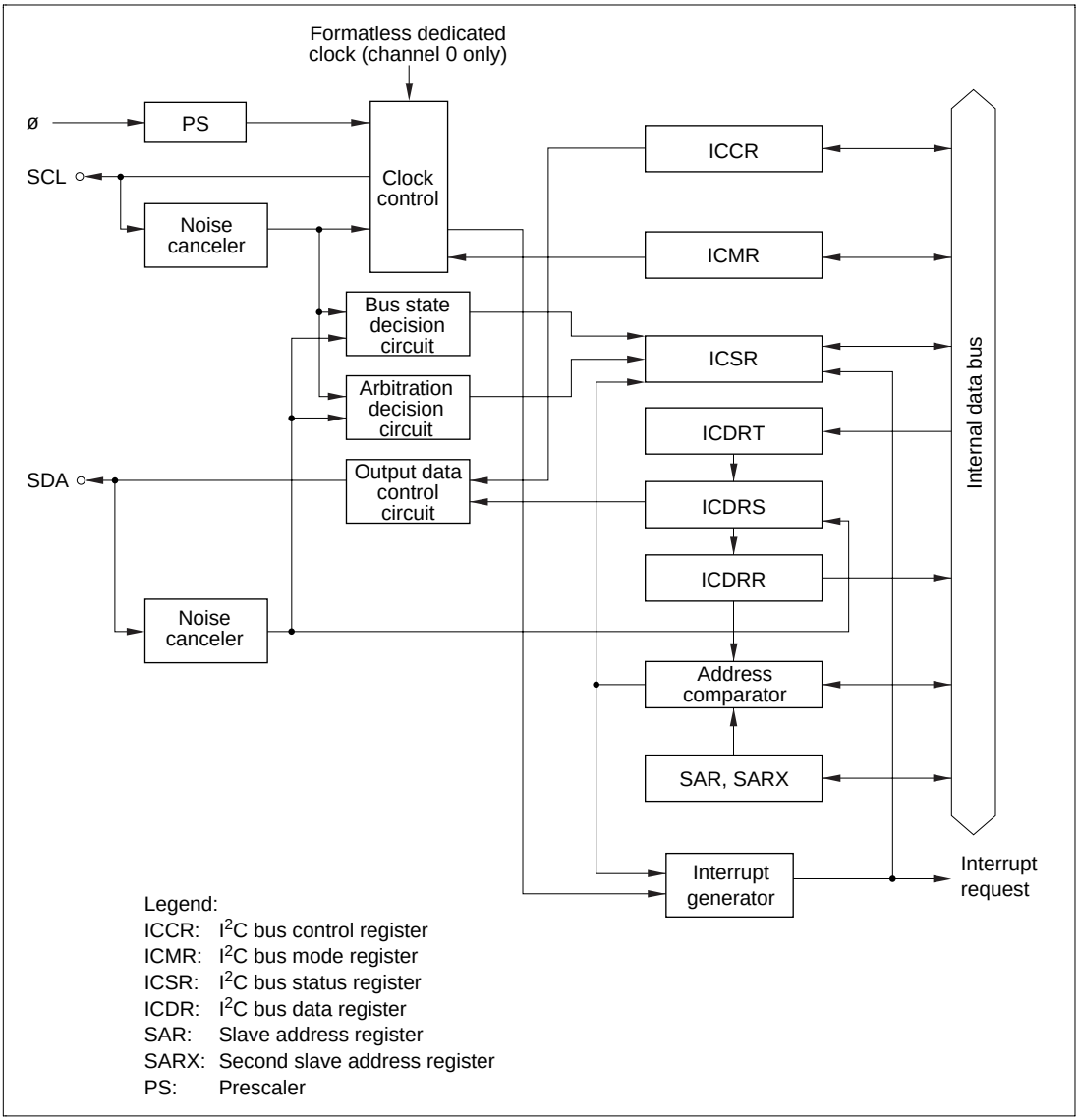



**Figure 16.1 Block Diagram of I²C Bus Interface**

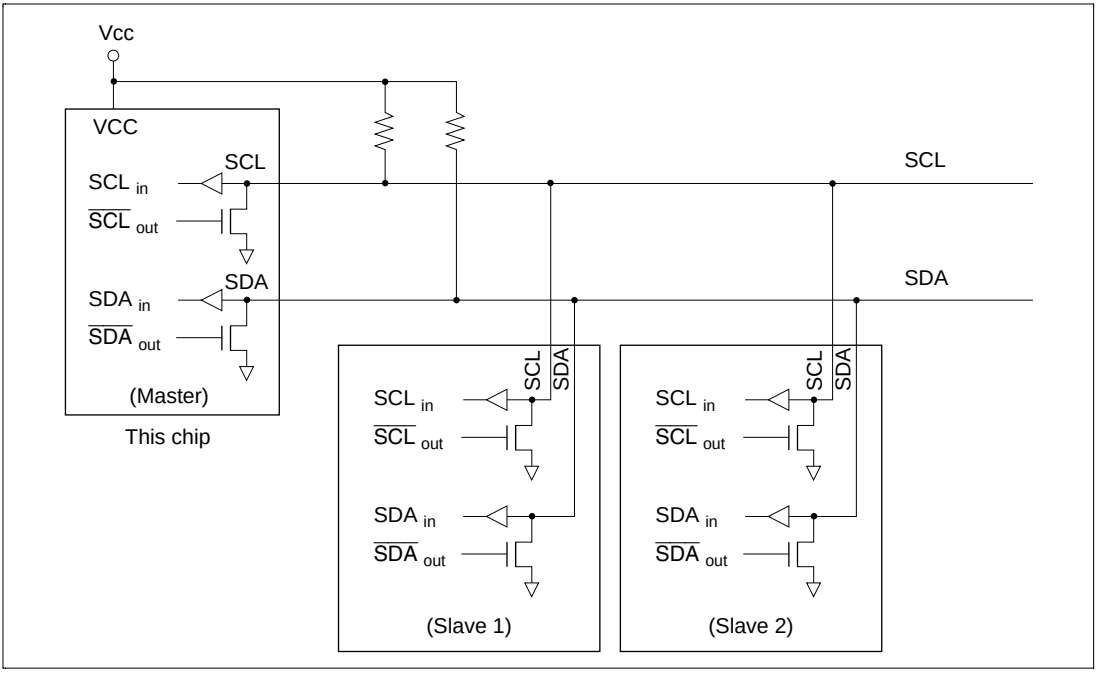



**Figure 16.2 I²C Bus Interface Connections (Example: This Chip as Master)**

### 16.1.3 Input/Output Pins

Table 16.1 summarizes the input/output pins used by the I²C bus interface.

**Table 16.1 I²C Bus Interface Pins**

| Channel | Name | Abbreviation* | I/O | Function |
|---|---|---|---|---|
| 0 | Serial clock | SCL0 | I/O | IIC0 serial clock input/output |
| | Serial data | SDA0 | I/O | IIC0 serial data input/output |
| | Formatless serial clock | VSYNCI | Input | IIC0 formatless serial clock input |
| 1 | Serial clock | SCL1 | I/O | IIC1 serial clock input/output |
| | Serial data | SDA1 | I/O | IIC1 serial data input/output |

Note: * In the text, the channel subscript is omitted, and only SCL and SDA are used.

### 16.1.4 Register Configuration

Table 16.2 summarizes the registers of the I²C bus interface.

**Table 16.2 Register Configuration**

| Channel | Name | Abbreviation | R/W | Initial Value | Address*1 |
|---|---|---|---|---|---|
| 0 | I²C bus control register | ICCR0 | R/W | H'01 | H'FFD8 |
| | I²C bus status register | ICSR0 | R/W | H'00 | H'FFD9 |
| | I²C bus data register | ICDR0 | R/W | — | H'FFDE*2 |
| | I²C bus mode register | ICMR0 | R/W | H'00 | H'FFDF*2 |
| | Slave address register | SAR0 | R/W | H'00 | H'FFDF*2 |
| | Second slave address register | SARX0 | R/W | H'01 | H'FFDE*2 |
| 1 | I²C bus control register | ICCR1 | R/W | H'01 | H'FF88 |
| | I²C bus status register | ICSR1 | R/W | H'00 | H'FF89 |
| | I²C bus data register | ICDR1 | R/W | — | H'FF8E*2 |
| | I²C bus mode register | ICMR1 | R/W | H'00 | H'FF8F*2 |
| | Slave address register | SAR1 | R/W | H'00 | H'FF8F*2 |
| | Second slave address register | SARX1 | R/W | H'01 | H'FF8E*2 |
| Common | Serial/timer control register | STCR | R/W | H'00 | H'FFC3 |
| | DDC switch register | DDCSWR | R/W | H'0F | H'FEE6 |
| | Module stop control register | MSTPCRH | R/W | H'3F | H'FF86 |
| | | MSTPCRL | R/W | H'FF | H'FF87 |

Notes: *1 Lower 16 bits of the address.

*2 The register that can be written or read depends on the ICE bit in the I²C bus control register. The slave address register can be accessed when ICE = 0, and the I²C bus mode register can be accessed when ICE = 1.

The I²C bus interface registers are assigned to the same addresses as other registers. Register selection is performed by means of the IICE bit in the serial/timer control register (STCR).

## 16.2 Register Descriptions

### 16.2.1 I²C Bus Data Register (ICDR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ICDR7 | ICDR6 | ICDR5 | ICDR4 | ICDR3 | ICDR2 | ICDR1 | ICDR0 |
| Initial value | — | — | — | — | — | — | — | — |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

- ICDRR

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ICDRR7 | ICDRR6 | ICDRR5 | ICDRR4 | ICDRR3 | ICDRR2 | ICDRR1 | ICDRR0 |
| Initial value | — | — | — | — | — | — | — | — |
| Read/Write | R | R | R | R | R | R | R | R |

- ICDRS

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ICDRS7 | ICDRS6 | ICDRR5 | ICDRS4 | ICDRS3 | ICDRS2 | ICDRS1 | ICDRS0 |
| Initial value | — | — | — | — | — | — | — | — |
| Read/Write | — | — | — | — | — | — | — | — |

- ICDRT

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ICDRT7 | ICDRT6 | ICDRT5 | ICDRT4 | ICDRT3 | ICDRT2 | ICDRT1 | ICDRT0 |
| Initial value | — | — | — | — | — | — | — | — |
| Read/Write | W | W | W | W | W | W | W | W |

- TDRE, RDRF (internal flags)

| Bit | | | | | | | — | — |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | TDRE | RDRF |
| Initial value | | | | | | | 0 | 0 |
| Read/Write | | | | | | | — | — |

ICDR is an 8-bit readable/writable register that is used as a transmit data register when transmitting and a receive data register when receiving. ICDR is divided internally into a shift register (ICDRS), receive buffer (ICDRR), and transmit buffer (ICDRT). ICDRS cannot be read or written by the CPU, ICDRR is read-only, and ICDRT is write-only. Data transfers among the three registers are performed automatically in coordination with changes in the bus state, and affect the status of internal flags such as TDRE and RDRF.

If IIC is in transmit mode and the next data is in ICDRT (the TDRE flag is 0) following transmission/reception of one frame of data using ICDRS, data is transferred automatically from ICDRT to ICDRS. If IIC is in receive mode and no previous data remains in ICDRR (the RDRF flag is 0) following transmission/reception of one frame of data using ICDRS, data is transferred automatically from ICDRS to ICDRR.

If the number of bits in a frame, excluding the acknowledge bit, is less than 8, transmit data and receive data are stored differently. Transmit data should be written justified toward the MSB side when MLS = 0, and toward the LSB side when MLS = 1. Receive data bits read from the LSB side should be treated as valid when MLS = 0, and bits read from the MSB side when MLS = 1.

ICDR is assigned to the same address as SARX, and can be written and read only when the ICE bit is set to 1 in ICCR.

The value of ICDR is undefined after a reset.

The TDRE and RDRF flags are set and cleared under the conditions shown below. Setting the TDRE and RDRF flags affects the status of the interrupt flags.

| TDRE | Description |
|---|---|
| 0 | The next transmit data is in ICDR (ICDRT), or transmission cannot be started (Initial value)<br>[Clearing conditions]<br>• When transmit data is written in ICDR (ICDRT) in transmit mode (TRS = 1)<br>• When a stop condition is detected in the bus line state after a stop condition is issued with the $I^2C$ bus format or serial format selected<br>• When a stop condition is detected with the $I^2C$ bus format selected<br>• In receive mode (TRS = 0)<br>(A 0 write to TRS during transfer is valid after reception of a frame containing an acknowledge bit) |
| 1 | The next transmit data can be written in ICDR (ICDRT)<br>[Setting conditions]<br>• In transmit mode (TRS = 1), when a start condition is detected in the bus line state after a start condition is issued in master mode with the $I^2C$ bus format or serial format selected<br>• At the first transmit mode setting (TRS = 1) (first transmit mode setting only) after the mode is switched from $I^2C$ bus mode to formatless mode<br>• When data is transferred from ICDRT to ICDRS<br>(Data transfer from ICDRT to ICDRS when TRS = 1 and TDRE = 0, and ICDRS is empty)<br>• When detecting a start condition and then switching from slave receive mode (TRS = 0) state to transmit mode (TRS = 1) (first transmit mode switching only). |

| RDRF | Description |
|---|---|
| 0 | The data in ICDR (ICDRR) is invalid (Initial value)<br>[Clearing condition]<br>When ICDR (ICDRR) receive data is read in receive mode |
| 1 | The ICDR (ICDRR) receive data can be read<br>[Setting condition]<br>When data is transferred from ICDRS to ICDRR<br>(Data transfer from ICDRS to ICDRR in case of normal termination with TRS = 0 and RDRF = 0) |

### 16.2.2 Slave Address Register (SAR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SVA6 | SVA5 | SVA4 | SVA3 | SVA2 | SVA1 | SVA0 | FS |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

SAR is an 8-bit readable/writable register that stores the slave address and selects the communication format. When the chip is in slave mode (and the addressing format is selected), if the upper 7 bits of SAR match the upper 7 bits of the first frame received after a start condition, the chip operates as the slave device specified by the master device. SAR is assigned to the same address as ICMR, and can be written and read only when the ICE bit is cleared to 0 in ICCR.

SAR is initialized to H'00 by a reset and in hardware standby mode.

**Bits 7 to 1—Slave Address (SVA6 to SVA0):** Set a unique address in bits SVA6 to SVA0, differing from the addresses of other slave devices connected to the $I^2C$ bus.

**Bit 0—Format Select (FS):** Used together with the FSX bit in SARX and the SW bit in DDCSWR to select the communication format.

- $I^2C$ bus format: addressing format with acknowledge bit
- Synchronous serial format: non-addressing format without acknowledge bit, for master mode only
- Formatless mode (channel 0 only): non-addressing format with or without acknowledge bit, slave mode only, start/stop conditions not detected

The FS bit also specifies whether or not SAR slave address recognition is performed in slave mode.

| DDCSWR Bit 6 | SAR Bit 0 | SARX Bit 0 | |
|---|---|---|---|
| **SW** | **FS** | **FSX** | **Operating Mode** |
| 0 | 0 | 0 | $I^2C$ bus format<br>• SAR and SARX slave addresses recognized |
| | | 1 | $I^2C$ bus format (Initial value)<br>• SAR slave address recognized<br>• SARX slave address ignored |
| | 1 | 0 | $I^2C$ bus format<br>• SAR slave address ignored<br>• SARX slave address recognized |
| | | 1 | Synchronous serial format<br>• SAR and SARX slave addresses ignored |
| 1 | 0 | 0 | Formatless mode (start/stop conditions not detected) |
| | 0 | 1 | • Acknowledge bit used |
| | 1 | 0 | |
| | 1 | 1 | Formatless mode* (start/stop conditions not detected)<br>• No acknowledge bit |

Note: * Do not set this mode when automatic switching to the $I^2C$ bus format is performed by means of the DDCSWR setting.

### 16.2.3 Second Slave Address Register (SARX)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SVAX6 | SVAX5 | SVAX4 | SVAX3 | SVAX2 | SVAX1 | SVAX0 | FSX |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

SARX is an 8-bit readable/writable register that stores the second slave address and selects the communication format. When the chip is in slave mode (and the addressing format is selected), if the upper 7 bits of SARX match the upper 7 bits of the first frame received after a start condition, the chip operates as the slave device specified by the master device. SARX is assigned to the same address as ICDR, and can be written and read only when the ICE bit is cleared to 0 in ICCR.

SARX is initialized to H'01 by a reset and in hardware standby mode.

**Bits 7 to 1—Second Slave Address (SVAX6 to SVAX0):** Set a unique address in bits SVAX6 to SVAX0, differing from the addresses of other slave devices connected to the $I^2C$ bus.

**Bit 0—Format Select X (FSX):** Used together with the FS bit in SAR and the SW bit in DDCSWR to select the communication format.

- $I^2C$ bus format: addressing format with acknowledge bit
- Synchronous serial format: non-addressing format without acknowledge bit, for master mode only
- Formatless mode: non-addressing format with or without acknowledge bit, slave mode only, start/stop conditions not detected

The FSX bit also specifies whether or not SARX slave address recognition is performed in slave mode. For details, see the description of the FS bit in SAR.

### 16.2.4 $I^2C$ Bus Mode Register (ICMR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | MLS | WAIT | CKS2 | CKS1 | CKS0 | BC2 | BC1 | BC0 |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

ICMR is an 8-bit readable/writable register that selects whether the MSB or LSB is transferred first, performs master mode wait control, and selects the master mode transfer clock frequency and the transfer bit count. ICMR is assigned to the same address as SAR. ICMR can be written and read only when the ICE bit is set to 1 in ICCR.

ICMR is initialized to H'00 by a reset and in hardware standby mode.

**Bit 7—MSB-First/LSB-First Select (MLS):** Selects whether data is transferred MSB-first or LSB-first.

If the number of bits in a frame, excluding the acknowledge bit, is less than 8, transmit data and receive data are stored differently. Transmit data should be written justified toward the MSB side when MLS = 0, and toward the LSB side when MLS = 1. Receive data bits read from the LSB side should be treated as valid when MLS = 0, and bits read from the MSB side when MLS = 1.

Do not set this bit to 1 when the $I^2C$ bus format is used.

**Bit 7**

| MLS | Description | |
|---|---|---|
| 0 | MSB-first | (Initial value) |
| 1 | LSB-first | |

**Bit 6—Wait Insertion Bit (WAIT):** Selects whether to insert a wait between the transfer of data and the acknowledge bit, in master mode with the $I^2C$ bus format. When WAIT is set to 1, after the fall of the clock for the final data bit, the IRIC flag is set to 1 in ICCR, and a wait state begins (with SCL at the low level). When the IRIC flag is cleared to 0 in ICCR, the wait ends and the acknowledge bit is transferred. If WAIT is cleared to 0, data and acknowledge bits are transferred consecutively with no wait inserted.

The IRIC flag in ICCR is set to 1 on completion of the acknowledge bit transfer, regardless of the WAIT setting.

The setting of this bit is invalid in slave mode.

**Bit 6**

| WAIT | Description | |
|---|---|---|
| 0 | Data and acknowledge bits transferred consecutively | (Initial value) |
| 1 | Wait inserted between data and acknowledge bits | |

**Bits 5 to 3—Serial Clock Select (CKS2 to CKS0):** These bits, together with the IICX1 (channel 1) or IICX0 (channel 0) bit in the STCR register, select the serial clock frequency in master mode. They should be set according to the required transfer rate.

| STCR Bit 5 or 6 | Bit 5 | Bit 4 | Bit 3 | | Transfer Rate | | | | |
|---|---|---|---|---|---|---|---|---|---|
| IICX | CKS2 | CKS1 | CKS0 | Clock | ø = 5 MHz | ø = 8 MHz | ø = 10 MHz | ø = 16 MHz | ø = 20 MHz |
| 0 | 0 | 0 | 0 | ø/28 | 179 kHz | 286 kHz | 357 kHz | 571 kHz* | 714 kHz* |
| | | | 1 | ø/40 | 125 kHz | 200 kHz | 250 kHz | 400 kHz | 500 kHz* |
| | | 1 | 0 | ø/48 | 104 kHz | 167 kHz | 208 kHz | 333 kHz | 417 kHz* |
| | | | 1 | ø/64 | 78.1 kHz | 125 kHz | 156 kHz | 250 kHz | 313 kHz |
| | 1 | 0 | 0 | ø/80 | 62.5 kHz | 100 kHz | 125 kHz | 200 kHz | 250 kHz |
| | | | 1 | ø/100 | 50.0 kHz | 80.0 kHz | 100 kHz | 160 kHz | 200 kHz |
| | | 1 | 0 | ø/112 | 44.6 kHz | 71.4 kHz | 89.3 kHz | 143 kHz | 179 kHz |
| | | | 1 | ø/128 | 39.1 kHz | 62.5 kHz | 78.1 kHz | 125 kHz | 156 kHz |
| 1 | 0 | 0 | 0 | ø/56 | 89.3 kHz | 143 kHz | 179 kHz | 286 kHz | 357 kHz |
| | | | 1 | ø/80 | 62.5 kHz | 100 kHz | 125 kHz | 200 kHz | 250 kHz |
| | | 1 | 0 | ø/96 | 52.1 kHz | 83.3 kHz | 104 kHz | 167 kHz | 208 kHz |
| | | | 1 | ø/128 | 39.1 kHz | 62.5 kHz | 78.1 kHz | 125 kHz | 156 kHz |
| | 1 | 0 | 0 | ø/160 | 31.3 kHz | 50.0 kHz | 62.5 kHz | 100 kHz | 125 kHz |
| | | | 1 | ø/200 | 25.0 kHz | 40.0 kHz | 50.0 kHz | 80.0 kHz | 100 kHz |
| | | 1 | 0 | ø/224 | 22.3 kHz | 35.7 kHz | 44.6 kHz | 71.4 kHz | 89.3 kHz |
| | | | 1 | ø/256 | 19.5 kHz | 31.3 kHz | 39.1 kHz | 62.5 kHz | 78.1 kHz |

Note: * Outside the $I^2C$ bus interface specification range (normal mode: max. 100 kHz; high-speed mode: max. 400 kHz).

**Bits 2 to 0—Bit Counter (BC2 to BC0):** Bits BC2 to BC0 specify the number of bits to be transferred next. With the I²C bus format (when the FS bit in SAR or the FSX bit in SARX is 0), the data is transferred with one addition acknowledge bit. Bit BC2 to BC0 settings should be made during an interval between transfer frames. If bits BC2 to BC0 are set to a value other than 000, the setting should be made while the SCL line is low.

The bit counter is initialized to 000 by a reset and when a start condition is detected. The value returns to 000 at the end of a data transfer, including the acknowledge bit.

| Bit 2 | Bit 1 | Bit 0 | Bits/Frame | | |
|---|---|---|---|---|---|
| BC2 | BC1 | BC0 | Synchronous Serial Format | I²C Bus Format | |
| 0 | 0 | 0 | 8 | 9 | (Initial value) |
| | | 1 | 1 | 2 | |
| | 1 | 0 | 2 | 3 | |
| | | 1 | 3 | 4 | |
| 1 | 0 | 0 | 4 | 5 | |
| | | 1 | 5 | 6 | |
| | 1 | 0 | 6 | 7 | |
| | | 1 | 7 | 8 | |

### 16.2.5 I²C Bus Control Register (ICCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ICE | IEIC | MST | TRS | ACKE | BBSY | IRIC | SCP |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/(W)* | W |

Note: * Only 0 can be written, to clear the flag.

ICCR is an 8-bit readable/writable register that enables or disables the I²C bus interface, enables or disables interrupts, selects master or slave mode and transmission or reception, enables or disables acknowledgement, confirms the I²C bus interface bus status, issues start/stop conditions, and performs interrupt flag confirmation.

ICCR is initialized to H'01 by a reset and in hardware standby mode.

**Bit 7—I²C Bus Interface Enable (ICE):** Selects whether or not the I²C bus interface is to be used. When ICE is set to 1, port pins function as SCL and SDA input/output pins and transfer operations are enabled. When ICE is cleared to 0, the I²C bus interface module is halted and its internal states are cleared.

The SAR and SARX registers can be accessed when ICE is 0. The ICMR and ICDR registers can be accessed when ICE is 1.

**Bit 7**

| ICE | Description | |
|---|---|---|
| 0 | I²C bus interface module disabled, with SCL and SDA signal pins set to port function | (Initial value) |
| | I²C bus interface module internal states initialized | |
| | SAR and SARX can be accessed | |
| 1 | I²C bus interface module enabled for transfer operations (pins SCL and SCA are driving the bus) | |
| | ICMR and ICDR can be accessed | |

**Bit 6—I²C Bus Interface Interrupt Enable (IEIC):** Enables or disables interrupts from the I²C bus interface to the CPU.

**Bit 6**

| IEIC | Description | |
|---|---|---|
| 0 | Interrupts disabled | (Initial value) |
| 1 | Interrupts enabled | |

**Bit 5—Master/Slave Select (MST)**

**Bit 4—Transmit/Receive Select (TRS)**

MST selects whether the I²C bus interface operates in master mode or slave mode.

TRS selects whether the I²C bus interface operates in transmit mode or receive mode.

In master mode with the I²C bus format, when arbitration is lost, MST and TRS are both reset by hardware, causing a transition to slave receive mode. In slave receive mode with the addressing format (FS = 0 or FSX = 0), hardware automatically selects transmit or receive mode according to the R/$\overline{W}$ bit in the first frame after a start condition.

Modification of the TRS bit during transfer is deferred until transfer of the frame containing the acknowledge bit is completed, and the changeover is made after completion of the transfer.

MST and TRS select the operating mode as follows.

| Bit 5 | Bit 4 | | |
|---|---|---|---|
| **MST** | **TRS** | **Operating Mode** | |
| 0 | 0 | Slave receive mode | (Initial value) |
| | 1 | Slave transmit mode | |
| 1 | 0 | Master receive mode | |
| | 1 | Master transmit mode | |

**Bit 5**

| MST | Description | |
|---|---|---|
| 0 | Slave mode<br>[Clearing conditions]<br>1. When 0 is written by software<br>2. When bus arbitration is lost after transmission is started in $I^2C$ bus format master mode | (Initial value) |
| 1 | Master mode<br>[Setting conditions]<br>1. When 1 is written by software (in cases other than clearing condition 2)<br>2. When 1 is written in MST after reading MST = 0 (in case of clearing condition 2) | |

**Bit 4**

| TRS | Description | |
|---|---|---|
| 0 | Receive mode<br>[Clearing conditions]<br>1. When 0 is written by software (in cases other than setting condition 3)<br>2. When 0 is written in TRS after reading TRS = 1 (in case of clearing condition 3)<br>3. When bus arbitration is lost after transmission is started in $I^2C$ bus format master mode<br>4. When the SW bit in DDCSWR changes from 1 to 0 | (Initial value) |
| 1 | Transmit mode<br>[Setting conditions]<br>1. When 1 is written by software (in cases other than clearing conditions 3 and 4)<br>2. When 1 is written in TRS after reading TRS = 0 (in case of clearing conditions 3 and 4)<br>3. When a 1 is received as the R/$\overline{W}$ bit of the first frame in $I^2C$ bus format slave mode | |

**Bit 3—Acknowledge Bit Judgement Selection (ACKE):** Specifies whether the value of the acknowledge bit returned from the receiving device when using the $I^2C$ bus format is to be ignored and continuous transfer is performed, or transfer is to be aborted and error handling, etc., performed if the acknowledge bit is 1. When the ACKE bit is 0, the value of the received acknowledge bit is not indicated by the ACKB bit, which is always 0.

In the H8S/2128 Series, the DTC can be used to perform continuous transfer. The DTC is activated when the IRTR interrupt flag is set to 1 (IRTR is one of two interrupt flags, the other being IRIC). When the ACKE bit is 0, the TDRE, IRIC, and IRTR flags are set on completion of data transmission, regardless of the value of the acknowledge bit. When the ACKE bit is 1, the TDRE, IRIC, and IRTR flags are set on completion of data transmission when the acknowledge bit is 0, and the IRIC flag alone is set on completion of data transmission when the acknowledge bit is 1.

When the DTC is activated, the TDRE, IRIC, and IRTR flags are cleared to 0 after the specified number of data transfers have been executed. Consequently, interrupts are not generated during continuous data transfer, but if data transmission is completed with a 1 acknowledge bit when the ACKE bit is set to 1, the DTC is not activated and an interrupt is generated, if enabled.

Depending on the receiving device, the acknowledge bit may be significant, in indicating completion of processing of the received data, for instance, or may be fixed at 1 and have no significance.

**Bit 3**

| ACKE | Description | |
|---|---|---|
| 0 | The value of the acknowledge bit is ignored, and continuous transfer is performed | (Initial value) |
| 1 | If the acknowledge bit is 1, continuous transfer is interrupted | |

**Bit 2—Bus Busy (BBSY):** The BBSY flag can be read to check whether the $I^2C$ bus (SCL, SDA) is busy or free. In master mode, this bit is also used to issue start and stop conditions.

A high-to-low transition of SDA while SCL is high is recognized as a start condition, setting BBSY to 1. A low-to-high transition of SDA while SCL is high is recognized as a stop condition, clearing BBSY to 0.

To issue a start condition, use a MOV instruction to write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, use a MOV instruction to write 0 in BBSY and 0 in SCP. It is not possible to write to BBSY in slave mode; the $I^2C$ bus interface must be set to master transmit mode before issuing a start condition. MST and TRS should both be set to 1 before writing 1 in BBSY and 0 in SCP.

| Bit 2 | | |
|---|---|---|
| **BBSY** | **Description** | |
| 0 | Bus is free | (Initial value) |
| | [Clearing condition] | |
| | When a stop condition is detected | |
| 1 | Bus is busy | |
| | [Setting condition] | |
| | When a start condition is detected | |

**Bit 1—I²C Bus Interface Interrupt Request Flag (IRIC):** Indicates that the I²C bus interface has issued an interrupt request to the CPU. IRIC is set to 1 at the end of a data transfer, when a slave address or general call address is detected in slave receive mode, when bus arbitration is lost in master transmit mode, and when a stop condition is detected. IRIC is set at different times depending on the FS bit in SAR and the WAIT bit in ICMR. See section 16.3.6, IRIC Setting Timing and SCL Control. The conditions under which IRIC is set also differ depending on the setting of the ACKE bit in ICCR.

IRIC is cleared by reading IRIC after it has been set to 1, then writing 0 in IRIC.

When the DTC is used, IRIC is cleared automatically and transfer can be performed continuously without CPU intervention.

**Bit 1**

| IRIC | Description |
|---|---|
| 0 | Waiting for transfer, or transfer in progress (Initial value)<br>[Clearing conditions]<br>1. When 0 is written in IRIC after reading IRIC = 1<br>2. When ICDR is written or read by the DTC<br>(When the TDRE or RDRF flag is cleared to 0)<br>(This is not always a clearing condition; see the description of DTC operation for details) |
| 1 | Interrupt requested<br>[Setting conditions]<br>• $I^2C$ bus format master mode<br>1. When a start condition is detected in the bus line state after a start condition is issued<br>(when the TDRE flag is set to 1 because of first frame transmission)<br>2. When a wait is inserted between the data and acknowledge bit when WAIT = 1<br>3. At the end of data transfer<br>(at the rise of the 9th transmit/receive clock pulse when no wait is inserted, (WAIT=0) and, when a wait is inserted (WAIT=1), at the fall of the 8th transmit/receive clock pulse)<br>4. When a slave address is received after bus arbitration is lost<br>(when the AL flag is set to 1)<br>5. When 1 is received as the acknowledge bit when the ACKE bit is 1<br>(when the ACKB bit is set to 1)<br>• $I^2C$ bus format slave mode<br>1. When the slave address (SVA, SVAX) matches<br>(when the AAS and AASX flags are set to 1)<br>and at the end of data transfer up to the subsequent retransmission start condition or stop condition detection<br>(when the TDRE or RDRF flag is set to 1)<br>2. When the general call address is detected<br>(when FS = 0 and the ADZ flag is set to 1)<br>and at the end of data transfer up to the subsequent retransmission start condition or stop condition detection<br>(when the TDRE or RDRF flag is set to 1)<br>3. When 1 is received as the acknowledge bit when the ACKE bit is 1<br>(when the ACKB bit is set to 1)<br>4. When a stop condition is detected<br>(when the STOP or ESTP flag is set to 1)<br>• Synchronous serial format, and formatless mode<br>1. At the end of data transfer<br>(when the TDRE or RDRF flag is set to 1)<br>2. When a start condition is detected with serial format selected<br>3. When the SW bit is set to 1 in DDCSWR<br>Except the above, when the conditions to set the TDRE or RDRF internal flag to 1 is generated |

When, with the $I^2C$ bus format selected, IRIC is set to 1 and an interrupt is generated, other flags must be checked in order to identify the source that set IRIC to 1. Although each source has a corresponding flag, caution is needed at the end of a transfer.

When the TDRE or RDRF internal flag is set, the readable IRTR flag may or may not be set. The IRTR flag (the DTC start request flag) is not set at the end of a data transfer up to detection of a retransmission start condition or stop condition after a slave address (SVA) or general call address match in $I^2C$ bus format slave mode.

Even when the IRIC flag and IRTR flag are set, the TDRE or RDRF internal flag may not be set. The IRIC and IRTR flags are not cleared at the end of the specified number of transfers in continuous transfer using the DTC. The TDRE or RDRF flag is cleared, however, since the specified number of ICDR reads or writes have been completed.

Table 16.3 shows the relationship between the flags and the transfer states.

**Table 16.3 Flags and Transfer States**

| MST | TRS | BBSY | ESTP | STOP | IRTR | AASX | AL | AAS | ADZ | ACKB | State |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1/0 | 1/0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Idle state (flag clearing required) |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Start condition issuance |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Start condition established |
| 1 | 1/0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1 | Master mode wait |
| 1 | 1/0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0/1 | Master mode transmit/receive end |
| 0 | 0 | 1 | 0 | 0 | 0 | 1/0 | 1 | 1/0 | 1/0 | 0 | Arbitration lost |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | SAR match by first frame in slave mode |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | General call address match |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | SARX match |
| 0 | 1/0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0/1 | Slave mode transmit/receive end (except after SARX match) |
| 0 | 1/0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Slave mode transmit/receive end (after SARX match) |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | |
| 0 | 1/0 | 0 | 1/0 | 1/0 | 0 | 0 | 0 | 0 | 0 | 0/1 | Stop condition detected |

**Bit 0—Start Condition/Stop Condition Prohibit (SCP):** Controls the issuing of start and stop conditions in master mode. To issue a start condition, write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, write 0 in BBSY and 0 in SCP. This bit is always read as 1. If 1 is written, the data is not stored.

| Bit 0 | |
|---|---|
| **SCP** | **Description** |
| 0 | Writing 0 issues a start or stop condition, in combination with the BBSY flag |
| 1 | Reading always returns a value of 1 (Initial value)<br>Writing is ignored |

### 16.2.6 I²C Bus Status Register (ICSR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ESTP | STOP | IRTR | AASX | AL | AAS | ADZ | ACKB |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/(W)* | R/(W)* | R/(W)* | R/(W)* | R/(W)* | R/(W)* | R/(W)* | R/W |

Note: * Only 0 can be written, to clear the flags.

ICSR is an 8-bit readable/writable register that performs flag confirmation and acknowledge confirmation and control.

ICSR is initialized to H'00 by a reset and in hardware standby mode.

**Bit 7—Error Stop Condition Detection Flag (ESTP):** Indicates that a stop condition has been detected during frame transfer in I²C bus format slave mode.

**Bit 7**

| ESTP | Description | |
|---|---|---|
| 0 | No error stop condition | (Initial value) |
| | [Clearing conditions] | |
| | 1. When 0 is written in ESTP after reading ESTP = 1 | |
| | 2. When the IRIC flag is cleared to 0 | |
| 1 | • In $I^2C$ bus format slave mode<br>Error stop condition detected<br>[Setting condition]<br>When a stop condition is detected during frame transfer | |
| | • In other modes<br>No meaning | |

**Bit 6—Normal Stop Condition Detection Flag (STOP):** Indicates that a stop condition has been detected after completion of frame transfer in $I^2C$ bus format slave mode.

**Bit 6**

| STOP | Description | |
|---|---|---|
| 0 | No normal stop condition | (Initial value) |
| | [Clearing conditions] | |
| | 1. When 0 is written in STOP after reading STOP = 1 | |
| | 2. When the IRIC flag is cleared to 0 | |
| 1 | • In $I^2C$ bus format slave mode<br>Normal stop condition detected<br>[Setting condition]<br>When a stop condition is detected after completion of frame transfer | |
| | • In other modes<br>No meaning | |

**Bit 5—$I^2C$ Bus Interface Continuous Transmission/Reception Interrupt Request Flag (IRTR):** Indicates that the $I^2C$ bus interface has issued an interrupt request to the CPU, and the source is completion of reception/transmission of one frame in continuous transmission/reception for which DTC activation is possible. When the IRTR flag is set to 1, the IRIC flag is also set to 1 at the same time.

IRTR flag setting is performed when the TDRE or RDRF flag is set to 1. IRTR is cleared by reading IRTR after it has been set to 1, then writing 0 in IRTR. IRTR is also cleared automatically when the IRIC flag is cleared to 0.

**Bit 5**

| IRTR | Description | |
|---|---|---|
| 0 | Waiting for transfer, or transfer in progress | (Initial value) |
| | [Clearing conditions] | |
| | 1. When 0 is written in IRTR after reading IRTR = 1 | |
| | 2. When the IRIC flag is cleared to 0 | |
| 1 | Continuous transfer state | |
| | [Setting condition] | |
| | • In $I^2C$ bus interface slave mode<br>When the TDRE or RDRF flag is set to 1 when AASX = 1 | |
| | • In other modes<br>When the TDRE or RDRF flag is set to 1 | |

**Bit 4—Second Slave Address Recognition Flag (AASX):** In $I^2C$ bus format slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVAX6 to SVAX0 in SARX.

AASX is cleared by reading AASX after it has been set to 1, then writing 0 in AASX. AASX is also cleared automatically when a start condition is detected.

**Bit 4**

| AASX | Description | |
|---|---|---|
| 0 | Second slave address not recognized | (Initial value) |
| | [Clearing conditions] | |
| | 1. When 0 is written in AASX after reading AASX = 1 | |
| | 2. When a start condition is detected | |
| | 3. In master mode | |
| 1 | Second slave address recognized | |
| | [Setting condition] | |
| | When the second slave address is detected in slave receive mode while FSX = 0 | |

**Bit 3—Arbitration Lost (AL):** This flag indicates that arbitration was lost in master mode. The $I^2C$ bus interface monitors the bus. When two or more master devices attempt to seize the bus at nearly the same time, if the $I^2C$ bus interface detects data differing from the data it sent, it sets AL to 1 to indicate that the bus has been taken by another master.

AL is cleared by reading AL after it has been set to 1, then writing 0 in AL. In addition, AL is reset automatically by write access to ICDR in transmit mode, or read access to ICDR in receive mode.

**Bit 3**

| AL | Description |
|---|---|
| 0 | Bus arbitration won (Initial value)<br>[Clearing conditions]<br>1. When ICDR data is written (transmit mode) or read (receive mode)<br>2. When 0 is written in AL after reading AL = 1 |
| 1 | Arbitration lost<br>[Setting conditions]<br>1. If the internal SDA and SDA pin disagree at the rise of SCL in master transmit mode<br>2. If the internal SCL line is high at the fall of SCL in master transmit mode |

**Bit 2—Slave Address Recognition Flag (AAS):** In $I^2C$ bus format slave receive mode, this flag is set to 1 if the first frame following a start condition matches bits SVA6 to SVA0 in SAR, or if the general call address (H'00) is detected.

AAS is cleared by reading AAS after it has been set to 1, then writing 0 in AAS. In addition, AAS is reset automatically by write access to ICDR in transmit mode, or read access to ICDR in receive mode.

**Bit 2**

| AAS | Description |
|---|---|
| 0 | Slave address or general call address not recognized (Initial value)<br>[Clearing conditions]<br>1. When ICDR data is written (transmit mode) or read (receive mode)<br>2. When 0 is written in AAS after reading AAS = 1<br>3. In master mode |
| 1 | Slave address or general call address recognized<br>[Setting condition]<br>When the slave address or general call address is detected in slave receive mode while FS = 0 |

**Bit 1—General Call Address Recognition Flag (ADZ):** In $I^2C$ bus format slave receive mode, this flag is set to 1 if the first frame following a start condition is the general call address (H'00).

ADZ is cleared by reading ADZ after it has been set to 1, then writing 0 in ADZ. In addition, ADZ is reset automatically by write access to ICDR in transmit mode, or read access to ICDR in receive mode.

**Bit 1**

| ADZ | Description | |
|---|---|---|
| 0 | General call address not recognized | (Initial value) |
| | [Clearing conditions] | |
| | 1. When ICDR data is written (transmit mode) or read (receive mode) | |
| | 2. When 0 is written in ADZ after reading ADZ = 1 | |
| | 3. In master mode | |
| 1 | General call address recognized | |
| | [Setting condition] | |
| | When the general call address is detected in slave receive mode while FSX = 0 or FS = 0 | |

**Bit 0—Acknowledge Bit (ACKB):** Stores acknowledge data. In transmit mode, after the receiving device receives data, it returns acknowledge data, and this data is loaded into ACKB. In receive mode, after data has been received, the acknowledge data set in this bit is sent to the transmitting device.

When this bit is read, in transmission (when TRS = 1), the value loaded from the bus line (returned by the receiving device) is read. In reception (when TRS = 0), the value set by internal software is read.

When this bit is written to, the acknowledge data transmitted at the receipt is rewritten regardless of the TRS value. The data loaded fom the receiving device is retained, therefore take care of using bit-manipulation instructions.

**Bit 0**

| ACKB | Description | |
|---|---|---|
| 0 | Receive mode: 0 is output at acknowledge output timing | (Initial value) |
| | Transmit mode: Indicates that the receiving device has acknowledged the data (signal is 0) | |
| 1 | Receive mode: 1 is output at acknowledge output timing | |
| | Transmit mode: Indicates that the receiving device has not acknowledged the data (signal is 1) | |

### 16.2.7 Serial/Timer Control Register (STCR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | — | IICX1 | IICX0 | IICE | FLSHE | — | ICKS1 | ICKS0 |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

STCR is an 8-bit readable/writable register that controls register access, the $I^2C$ interface operating mode (when the on-chip IIC option is included), and on-chip flash memory (F-ZTAT versions), and selects the TCNT input clock source. For details of functions not related to the $I^2C$ bus interface, see section 3.2.4, Serial/Timer Control Register (STCR), and the descriptions of the relevant modules. If a module controlled by STCR is not used, do not write 1 to the corresponding bit.

STCR is initialized to H'00 by a reset and in hardware standby mode.

**Bit 7—Reserved:** Do not write 1 to this bit.

**Bit 6 and 5—$I^2C$ Transfer Select 1 and 0 (IICX1 and 0):** This bit, together with bits CKS2 to CKS0 in ICMR, selects the transfer rate in master mode. For details, see section 16.2.4, $I^2C$ Bus Mode Register (ICMR).

**Bit 4—$I^2C$ Master Enable (IICE):** Controls CPU access to the $I^2C$ bus interface data and control registers (ICCR, ICSR, ICDR/SARX, ICMR/SAR), PWMX data and control registers, and SCI control registers.

**Bit 4**

| IICE | Description | |
|---|---|---|
| 0 | CPU access to $I^2C$ bus interface data and control registers is disabled | (Initial value) |
| | CPU access to SCI control registers is enabled | |
| 1 | CPU access to $I^2C$ bus interface data and control registers is enabled | |
| | CPU access to PWMX data and control registers is enabled | |

**Bit 3—Flash Memory Control Register Enable (FLSHE):** Controls CPU access to the flash memory control registers, the power-down mode control registers, and the supporting module control registers. See section 3.2.4, Serial Timer Control Register (STCR), for details.

**Bit 2—Reserved:** Do not write 1 to this bit.

**Bits 1 and 0—Internal Clock Source Select 1 and 0 (ICKS1, ICSK0):** These bits, together with bits CKS2 to CKS0 in TCR, select the clock input to the timer counters (TCNT). For details, see section 12.2.4, Timer Control Register (TCR).

### 16.2.8 DDC Switch Register (DDCSWR)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | SWE | SW | IE | IF | CLR3 | CLR2 | CLR1 | CLR0 |
| Initial value | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/(W)*1 | W*2 | W*2 | W*2 | W*2 |

Notes: *1 Only 0 can be written, to clear the flag.
*2 Always read as 1.

DDCSWR is an 8-bit readable/writable register that is used to initialize IIC and controls IIC internal latch clearance.

DDCSWR is initialized to H'0F by a reset and in hardware standby mode.

**Bits 7—DDC Mode Switch Enable (SWE):** Selects the function for automatically switching IIC channel 0 from formatless mode to the $I^2C$ bus format.

**Bit 7**

| SWE | Description | |
|---|---|---|
| 0 | Automatic switching of IIC channel 0 from formatless mode to $I^2C$ bus format is disabled | (Initial value) |
| 1 | Automatic switching of IIC channel 0 from formatless mode to $I^2C$ bus format is enabled | |

**Bits 6—DDC Mode Switch (SW):** Selects either formatless mode or the $I^2C$ bus format for IIC channel 0.

**Bit 6**

| SW | Description | |
|---|---|---|
| 0 | IIC channel 0 is used with the $I^2C$ bus format<br>[Clearing conditions]<br>1. When 0 is written by software<br>2. When a falling edge is detected on the SCL pin when SWE = 1 | (Initial value) |
| 1 | IIC channel 0 is used in formatless mode<br>[Setting condition]<br>When 1 is written in SW after reading SW = 0 | |

**Bits 5—DDC Mode Switch Interrupt Enable Bit (IE):** Enables or disables an interrupt request to the CPU when automatic format switching is executed for IIC channel 0.

**Bit 5**

| IE | Description | |
|---|---|---|
| 0 | Interrupt when automatic format switching is executed is disabled | (Initial value) |
| 1 | Interrupt when automatic format switching is executed is enabled | |

**Bits 4—DDC Mode Switch Interrupt Flag (IF):** Flag that indicates an interrupt request to the CPU when automatic format switching is executed for IIC channel 0.

**Bit 4**

| IF | Description | |
|---|---|---|
| 0 | No interrupt is requested when automatic format switching is executed<br>[Clearing condition]<br>When 0 is written in IF after reading IF = 1 | (Initial value) |
| 1 | An interrupt is requested when automatic format switching is executed<br>[setting condition]<br>When a falling edge is detected on the SCL pin when SWE = 1 | |

**Bits 3 to 0—IIC Clear 3 to 0 (CLR3 to CLR0):** These bits control initialization of the internal state of IIC0 and IIC1.

These bits can only be written to; if read they will always return a value of 1.

When a write operation is performed on these bits, a clear signal is generated for the internal latch circuit of the corresponding module(s), and the internal state of the IIC module(s) is initialized.

The write data for these bits is not retained. To perform IIC clearance, bits CLR3 to CLR0 must be written to simultaneously using an MOV instruction. Do not use a bit manipulation instruction such as BCLR.

When clearing is required again, all the bits must be written to in accordance with the setting.

| Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
|---|---|---|---|---|
| **CLR3** | **CLR2** | **CLR1** | **CLR0** | **Description** |
| 0 | 0 | — | — | Setting prohibited |
| | 1 | 0 | 0 | Setting prohibited |
| | | | 1 | IIC0 internal latch cleared |
| | | 1 | 0 | IIC1 internal latch cleared |
| | | | 1 | IIC0 and IIC1 internal latches cleared |
| 1 | — | — | — | Invalid setting |

### 16.2.9 Module Stop Control Register (MSTPCR)

| | MSTPCRH | | | | | | | | MSTPCRL | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | MSTP15 | MSTP14 | MSTP13 | MSTP12 | MSTP11 | MSTP10 | MSTP9 | MSTP8 | MSTP7 | MSTP6 | MSTP5 | MSTP4 | MSTP3 | MSTP2 | MSTP1 | MSTP0 |
| Initial value | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

MSTPCR comprises two 8-bit readable/writable registers, and is used to perform module stop mode control.

When the MSTP4 or MSTP3 bit is set to 1, operation of the corresponding IIC channel is halted at the end of the bus cycle, and a transition is made to module stop mode. For details, see section 21.5, Module Stop Mode.

MSTPCR is initialized to H'3FFF by a reset and in hardware standby mode. It is not initialized in software standby mode.

**MSTPCRL Bit 4—Module Stop (MSTP4):** Specifies IIC channel 0 module stop mode.

| MSTPCRL Bit 4 | | |
|---|---|---|
| **MSTP4** | **Description** | |
| 0 | IIC channel 0 module stop mode is cleared | |
| 1 | IIC channel 0 module stop mode is set | (Initial value) |

**MSTPCRL Bit 3—Module Stop (MSTP3):** Specifies IIC channel 1 module stop mode.

| MSTPCRL Bit 3 | | |
|---|---|---|
| **MSTP3** | **Description** | |
| 0 | IIC channel 1 module stop mode is cleared | |
| 1 | IIC channel 1 module stop mode is set | (Initial value) |

## 16.3 Operation

### 16.3.1 $I^2C$ Bus Data Format

The $I^2C$ bus interface has serial and $I^2C$ bus formats.

The $I^2C$ bus formats are addressing formats with an acknowledge bit. These are shown in figures 16.3 (a) and (b). The first frame following a start condition always consists of 8 bits.

IIC channel 0 only is capable of formatless operation, as shown in figure 16.4.

The serial format is a non-addressing format with no acknowledge bit. Although start and stop conditions must be issued, this format can be used as a synchronous serial format. This is shown in figure 16.5.

Figure 16.6 shows the $I^2C$ bus timing.

The symbols used in figures 16.3 to 16.6 are explained in table 16.4.

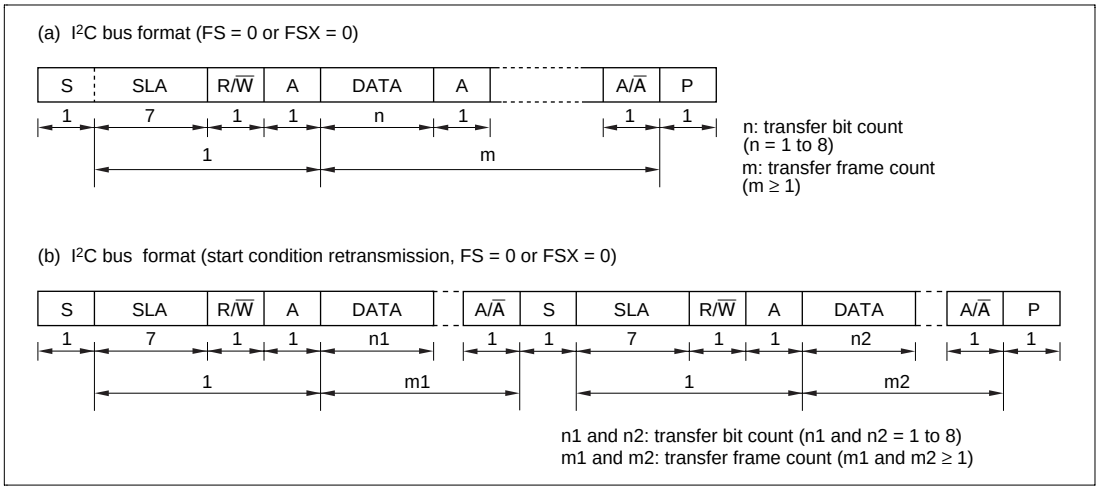



**Figure 16.3 I²C Bus Data Formats (I²C Bus Formats)**

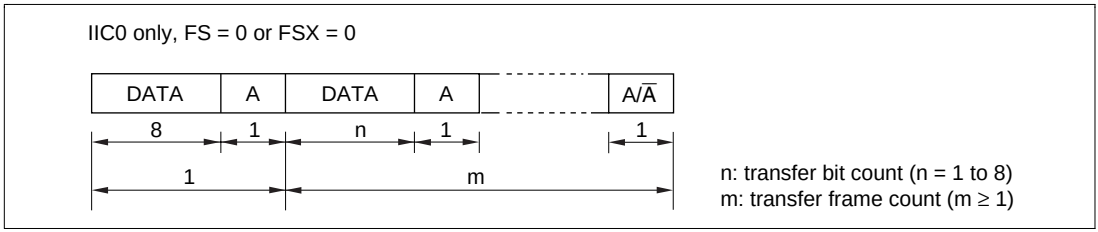



**Figure 16.4 Formatless**

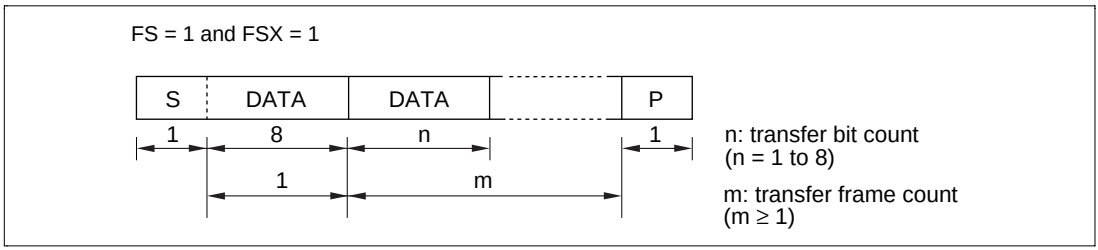



**Figure 16.5 I²C Bus Data Format (Serial Format)**

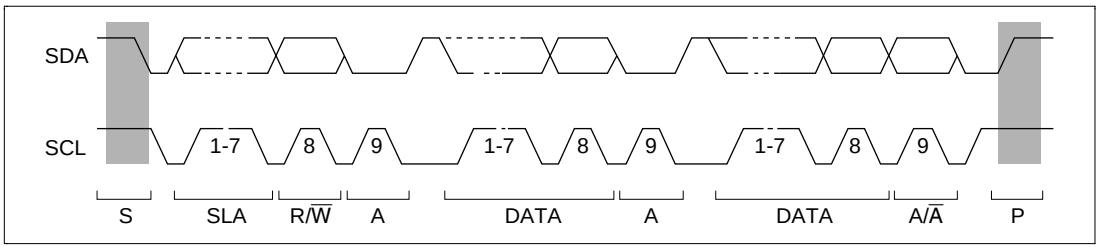



**Figure 16.6 I²C Bus Timing**

**Table 16.4 I²C Bus Data Format Symbols**

| Legend | |
|---|---|
| S | Start condition. The master device drives SDA from high to low while SCL is high |
| SLA | Slave address, by which the master device selects a slave device |
| R/$\overline{W}$ | Indicates the direction of data transfer: from the slave device to the master device when R/$\overline{W}$ is 1, or from the master device to the slave device when R/$\overline{W}$ is 0 |
| A | Acknowledge. The receiving device (the slave in master transmit mode, or the master in master receive mode) drives SDA low to acknowledge a transfer |
| DATA | Transferred data. The bit length is set by bits BC2 to BC0 in ICMR. The MSB-first or LSB-first format is selected by bit MLS in ICMR |
| P | Stop condition. The master device drives SDA from low to high while SCL is high |

### 16.3.2 Master Transmit Operation

In I²C bus format master transmit mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal.

The transmission procedure and operations by which data is sequentially transmitted in synchronization with ICDR write operations, are described below.

(1) Set the ICE bit in ICCR to l. Set bits MLS, WAIT, and CKS2 to CKS0 in ICMR, and bit IICX in STCR, according to the operation mode.

(2) Read the BBSY flag to confirm that the bus is free.

(3) Set the MST and TRS bits to 1 in ICCR to select master transmit mode.

(4) Write 1 to BBSY and 0 to SCP. This switches SDA from high to low when SCL is high, and generates the start condition.

(5) When the start condition is generated, the IRIC and IRTR flags are set to 1. If the IEIC bit in ICCR has been set to l, an interrupt request is sent to the CPU.

(6) Write data to ICDR (slave address + R/$\overline{W}$)

With the I²C bus format (when the FS bit in SAR or the FSX bit in SARX is 0), the first frame data following the start condition indicates the 7-bit slave address and transmit/receive direction.

Then clear the IRIC flag to indicate the end of transfer.

Writing to ICDR and clearing of the IRIC flag must be executed continuously, so that no interrupt is inserted.

If a period of time that is equal to transfer one byte has elapsed by the time the IRlC flag is cleared, the end of transfer cannot be identified.

The master device sequentially sends the transmit clock and the data written to ICDR with the timing shown in figure 16.7. The selected slave device (i.e. , the slave device with the matching slave address) drives SDA low at the 9th transmit clock pulse and returns an acknowledge signal.

(7) When one frame of data has been transmitted, the IRIC flag is set to 1 at the rise of the 9th transmit clock pulse. After one frame has been transmitted, SCL is automatically fixed low in synchronization with the internal clock until the next transmit data is written.

(8) Read the ACKB bit to confirm that ACKB is 0. When the slave device has not returned an acknowledge signal and ACKB remains 1, execute the transmit end processing described in step (12) and perform transmit operation again.

(9) Write the next data to be transmitted in ICDR. To indicate the end of data transfer, clear the IRIC flag to 0.

As described in step (6) above, writing to ICDR and clearing of the IRIC flag must be executed continuously so that no interrupt is inserted.

The next frame is transmitted in synchronization with the internal clock.

(10) When one frame of data has been transmitted, the IRIC flag is set to 1 at the rise of the 9th transmit clock pulse. After one frame has been transmitted, SCL is automatically fixed low in synchronization with the internal clock until the next transmit data is written.

(11) Read the ACKB bit of ICSR. Confirm that the slave device has returned an acknowledge signal and ACKB is 0. When more data is to be transmitted, return to step (9) to execute next transmit operation. If the slave device has not returned an acknowledge signal and ACKB is 1, execute the transmit end processing described in step (12).

(12) Clear the IRIC flag to 0. Write BBSY and SCP of ICCR to 0. By doing so, SDA is changed from low to high while SCL is high and the transmit stop condition is generated.

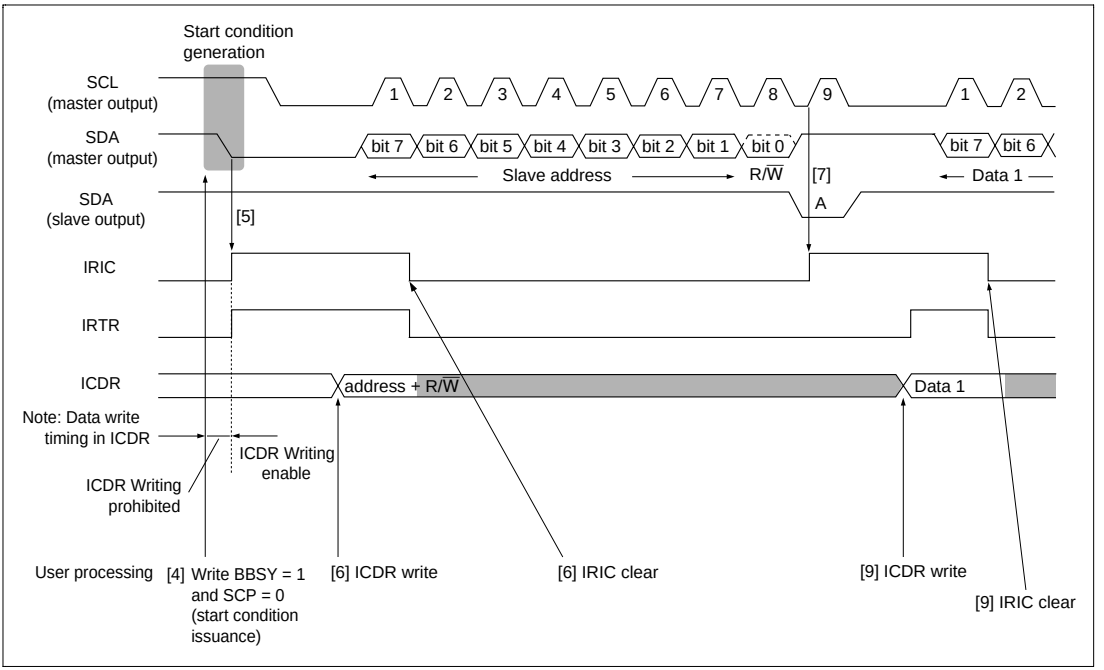



**Figure 16.7 Example of Master Transmit Mode Operation Timing (MLS = WAIT = 0)**

### 16.3.3 Master Receive Operation

In master receive mode, the master device outputs the receive clock, receives data, and returns an acknowledge signal. The slave device transmits data.

The receive procedure and operations by which data is sequentially received in synchronization with ICDR read operations, are described below.

(1) Clear the TRS bit of ICCR to 0 and switch from transmit mode to receive mode. Set the WAIT bit to 1 and clear the ACKB bit of ICSR to 0 (acknowledge data setting).

(2) When ICDR is read (dummy data read), reception is started and the receive clock is output, and data is received, in synchronization with the internal clock. To indicate the wait, clear the IRIC flag to 0.

Reading from ICDR and clearing of the IRIC f1ag must be executed continuously so that no interrupt is inserted.

If a period of time that is equal to transfer one byte has elapsed by the time the IRIC flag is cleared, the end of transfer cannot be identified.

(3) The IRIC flag is set to 1 at the fall of the 8th clock of a one-frame reception clock. At this point, if the IEIC bit of ICCR is set to 1, an interrupt request is generated to the CPU.

SCL is automatically fixed low in synchronization with the internal clock until the IRIC flag is cleared. If the first frame is the final reception frame, execute the end processing as described in (l0).

(4) Clear the IRIC flag to 0 to release from the wait state.

The master device outputs the 9th receive clock pulse, sets SDA to low, and returns an acknowledge signal.

(5) When one frame of data has been transmitted, the IRIC and IRTR flags are set to 1 at the rise of the 9th transmit clock pulse.

The master device continues to output the receive clock for the next receive data.

(6) Read the ICDR receive data.

(7) Clear the IRIC flag to indicate the next wait.

From clearing of the IRIC flag to completion of data transmission as described in steps (5), (6), and (7), must be performed within the time taken to transfer one byte, because releasing of the wait state as described in step (4) (or (9)).

(8) The IRIC flag is set to 1 at the fall of the 8th one-frame reception clock pulse. SCL is automatically fixed low in synchronization with the internal clock until the IRIC flag is cleared. If this frame is the final reception frame, execute the end processing as described in (l0).

(9) Clear the IRIC flag to 0 to release from the wait state. The master device outputs the 9th reception clock pulse, sets SDA to low, and returns an acknowledge signal.

By repeating steps (5) to (9) above, more data can be received.

(l0) Set the ACKB bit of ICSR to 1 and set the acknowledge data for the final reception.

Set the TRS bit of ICCR to 1 to change receive mode to transmit mode.

(11) Clear the IRIC flag to release from the wait state.

(12) When one frame of data has been received, the IRIC flag is set to 1 at the rise of the 9th reception clock pulse.

(13) Clear the WAIT bit of ICMR to 0 to cancel wait mode. Read the ICDR receive data and clear the IRIC flag to 0.

Clear the IRIC flag only when WAIT = 0.

(If the stop-condition generation command is executed after clearing the IRIC flag to 0 and then clearing the WAIT bit to 0, the SDA line is fixed low and the stop condition cannot be generated.)

(14) Write 0 to BBSY and SCP. This changes SDA from low to high when SCL is high, and generates the stop condition.

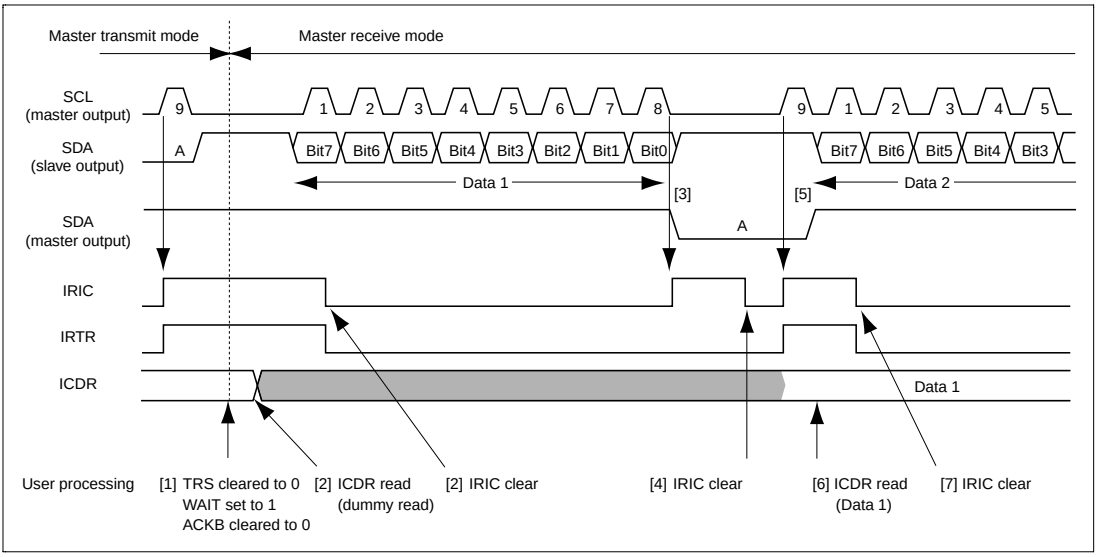



**Figure 16.8 (a) Example of Master Receive Mode Operation Timing (MLS = ACKB = 0, WAIT = 1)**

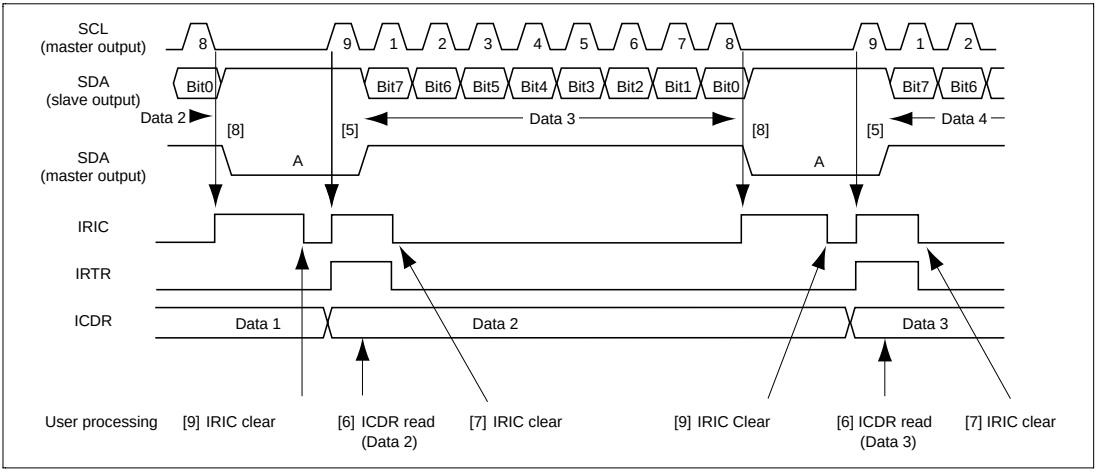



**Figure 16.8 (b) Example of Master Receive Mode Operation Timing (MLS = ACKB = 0, WAIT = 1)**

### 16.3.4 Slave Receive Operation

In slave receive mode, the master device outputs the transmit clock and transmit data, and the slave device returns an acknowledge signal. The reception procedure and operations in slave receive mode are described below.

[1] Set the ICE bit in ICCR to 1. Set the MLS bit in ICMR and the MST and TRS bits in ICCR according to the operating mode.

[2] When the start condition output by the master device is detected, the BBSY flag in ICCR is set to 1.

[3] When the slave address matches in the first frame following the start condition, the device operates as the slave device specified by the master device. If the 8th data bit (R/$\overline{W}$) is 0, the TRS bit in ICCR remains cleared to 0, and slave receive operation is performed.

[4] At the 9th clock pulse of the receive frame, the slave device drives SDA low and returns an acknowledge signal. At the same time, the IRIC flag in ICCR is set to 1. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU. If the RDRF internal flag has been cleared to 0, it is set to 1, and the receive operation continues. If the RDRF internal flag has been set to 1, the slave device drives SCL low from the fall of the receive clock until data is read into ICDR.

[5] Read ICDR and clear the IRIC flag in ICCR to 0. The RDRF flag is cleared to 0.

Receive operations can be performed continuously by repeating steps [4] and [5]. When SDA is changed from low to high when SCL is high, and the stop condition is detected, the BBSY flag in ICCR is cleared to 0.

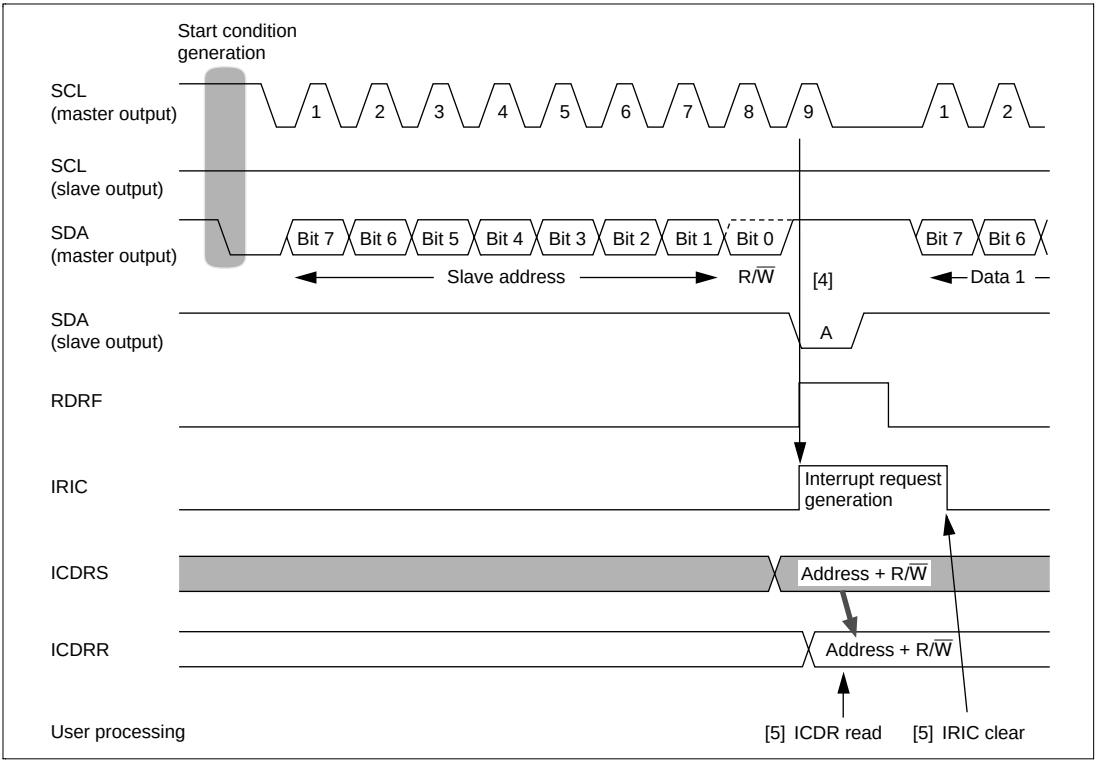



**Figure 16.9 Example of Slave Receive Mode Operation Timing (1) (MLS = ACKB = 0)**

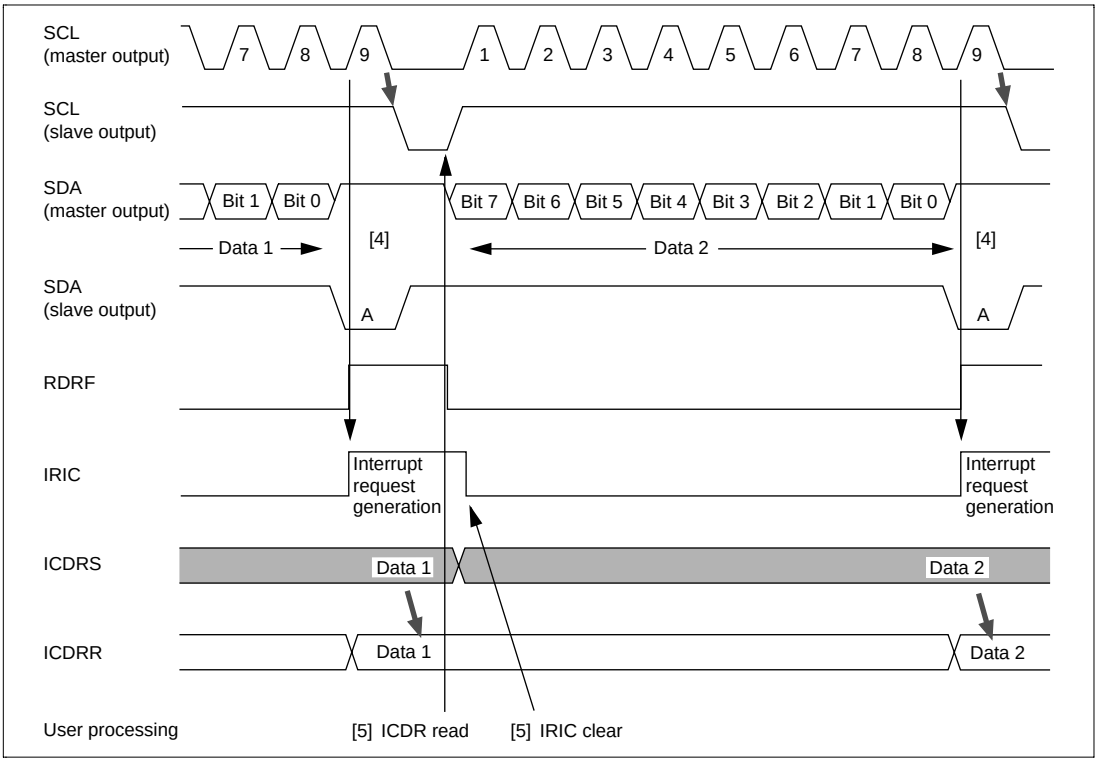



**Figure 16.10 Example of Slave Receive Mode Operation Timing (2) (MLS = ACKB = 0)**

### 16.3.5 Slave Transmit Operation

In slave transmit mode, the slave device outputs the transmit data, while the master device outputs the receive clock and returns an acknowledge signal. The transmission procedure and operations in slave transmit mode are described below.

[1] Set the ICE bit in ICCR to 1. Set the MLS bit in ICMR and the MST and TRS bits in ICCR according to the operating mode.

[2] When the slave address matches in the first frame following detection of the start condition, the slave device drives SDA low at the 9th clock pulse and returns an acknowledge signal. At the same time, the IRIC flag in ICCR is set to 1. If the IEIC bit in ICCR has been set to 1, an interrupt request is sent to the CPU. If the 8th data bit (R/$\overline{W}$) is 1, the TRS bit in ICCR is set to 1, and the mode changes to slave transmit mode automatically. The TDRE internal flag is set to 1. The slave device drives SCL low from the fall of the transmit clock until ICDR data is written.

[3] After clearing the IRIC flag to 0, write data to ICDR. The TDRE internal flag is cleared to 0. The written data is transferred to ICDRS, and the TDRE internal flag and the IRIC and IRTR

flags are set to 1 again. After clearing the IRIC flag to 0, write the next data to ICDR. The slave device sequentially sends the data written into ICDR in accordance with the clock output by the master device at the timing shown in figure 16.11.

[4] When one frame of data has been transmitted, the IRIC flag in ICCR is set to 1 at the rise of the 9th transmit clock pulse. If the TDRE internal flag has been set to 1, this slave device drives SCL low from the fall of the transmit clock until data is written to ICDR. The master device drives SDA low at the 9th clock pulse, and returns an acknowledge signal. As this acknowledge signal is stored in the ACKB bit in ICSR, this bit can be used to determine whether the transfer operation was performed normally. When the TDRE internal flag is 0, the data written into ICDR is transferred to ICDRS, transmission is started, and the TDRE internal flag and the IRIC and IRTR flags are set to 1 again.

[5] To continue transmission, clear the IRIC flag to 0, then write the next data to be transmitted into ICDR. The TDRE internal flag is cleared to 0.

Transmit operations can be performed continuously by repeating steps [4] and [5]. To end transmission, write H'FF to ICDR to release SDA on the slave side. When SDA is changed from low to high when SCL is high, and the stop condition is detected, the BBSY flag in ICCR is cleared to 0.

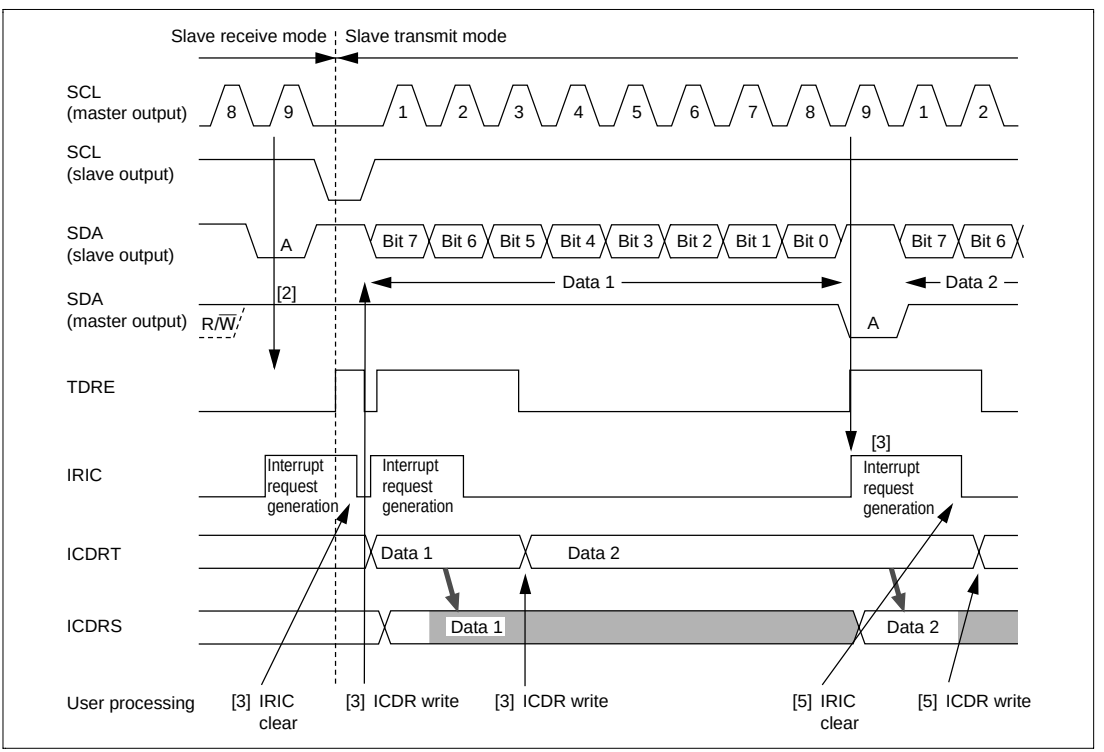



**Figure 16.11 Example of Slave Transmit Mode Operation Timing (MLS = 0)**

### 16.3.6 IRIC Setting Timing and SCL Control

The interrupt request flag (IRIC) is set at different times depending on the WAIT bit in ICMR, the FS bit in SAR, and the FSX bit in SARX. If the TDRE or RDRF internal flag is set to 1, SCL is automatically held low after one frame has been transferred; this timing is synchronized with the internal clock. Figure 16.12 shows the IRIC set timing and SCL control.

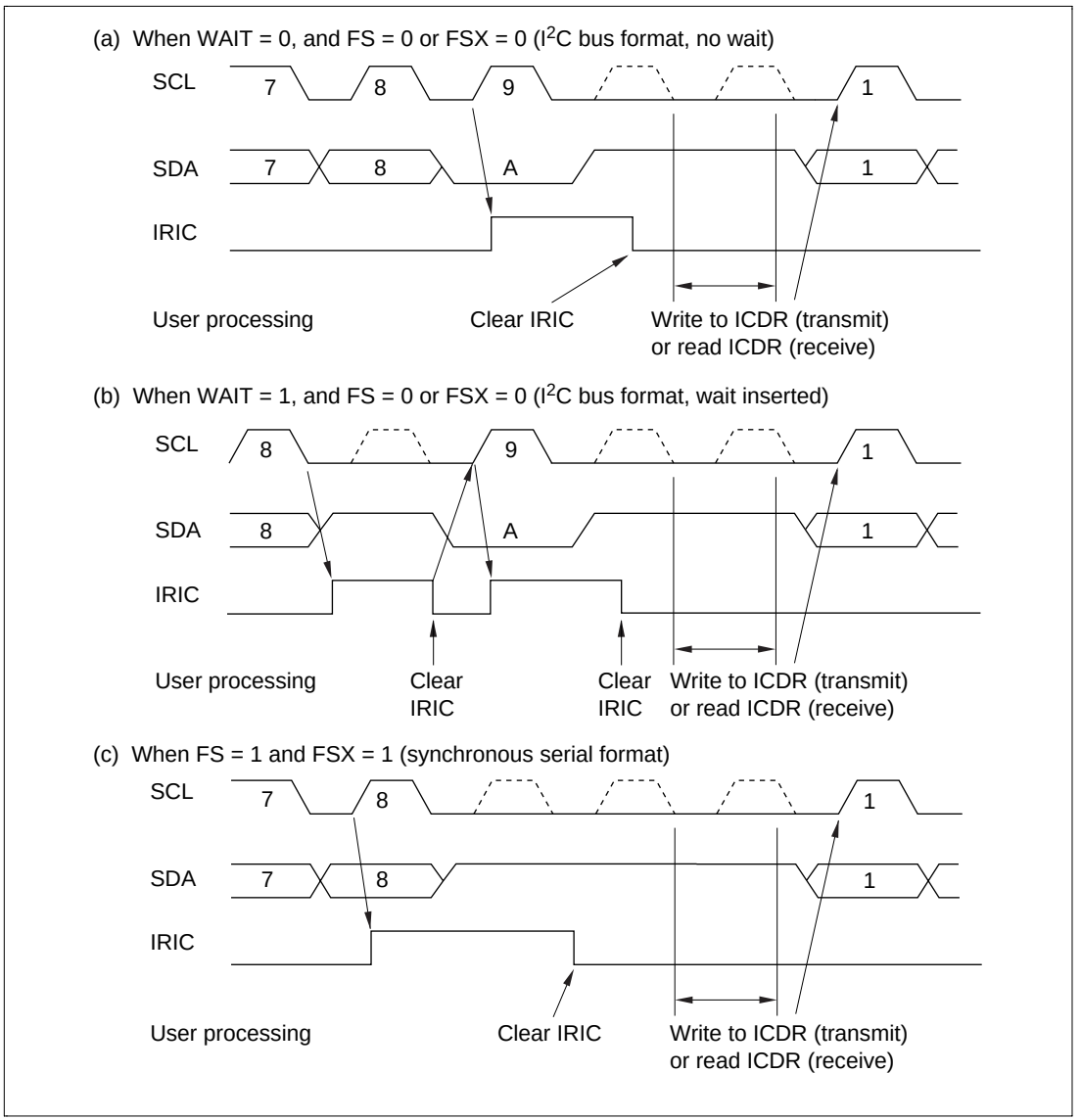



**Figure 16.12 IRIC Setting Timing and SCL Control**

### 16.3.7 Automatic Switching from Formatless Mode to I²C Bus Format

Setting the SW bit to 1 in DDCSWR enables formatless mode to be selected as the IIC0 operating mode. Switching from formatless mode to the I²C bus format (slave mode) is performed automatically when a falling edge is detected on the SCL pin.

The following four preconditions are necessary for this operation:

- A common data pin (SDA) for formatless and I²C bus format operation
- Separate clock pins for formatless operation (VSYNCI) and I²C bus format operation (SCL)
- A fixed 1 level for the SCL pin during formatless operation (the SCL pin does not output a low level)
- Settings of bits other than TRS in ICCR that allow I²C bus format operation

Automatic switching is performed from formatless mode to the I²C bus format when the SW bit in DDCSWR is automatically cleared to 0 on detection of a falling edge on the SCL pin. Switching from the I²C bus format to formatless mode is achieved by having software set the SW bit in DDCSWR to 1.

In formatless mode, bits (such as MSL and TRS) that control the I²C bus interface operating mode must not be modified. When switching from the I²C bus format to formatless mode, set the TRS bit to 1 or clear it to 0 according to the transmit data (transmission or reception) in formatless mode, then set the SW bit to 1. After automatic switching from formatless mode to the I²C bus format (slave mode), in order to wait for slave address reception, the TRS bit is automatically cleared to 0.

If a falling edge is detected on the SCL pin during formatless operation, the I²C bus interface operating mode is switched to the I²C bus format without waiting for a stop condition to be detected.

### 16.3.8 Operation Using the DTC

The $I^2C$ bus format provides for selection of the slave device and transfer direction by means of the slave address and the R/$\overline{W}$ bit, confirmation of reception with the acknowledge bit, indication of the last frame, and so on. Therefore, continuous data transfer using the DTC must be carried out in conjunction with CPU processing by means of interrupts.

Table 16.5 shows some examples of processing using the DTC. These examples assume that the number of transfer data bytes is known in slave mode.

**Table 16.5 Examples of Operation Using the DTC**

| Item | Master Transmit Mode | Master Receive Mode | Slave Transmit Mode | Slave Receive Mode |
|---|---|---|---|---|
| Slave address + R/$\overline{W}$ bit transmission/ reception | Transmission by DTC (ICDR write) | Transmission by CPU (ICDR write) | Reception by CPU (ICDR read) | Reception by CPU (ICDR read) |
| Dummy data read | — | Processing by CPU (ICDR read) | — | — |
| Actual data transmission/ reception | Transmission by DTC (ICDR write) | Reception by DTC (ICDR read) | Transmission by DTC (ICDR write) | Reception by DTC (ICDR read) |
| Dummy data (H'FF) write | — | — | Processing by DTC (ICDR write) | — |
| Last frame processing | Not necessary | Reception by CPU (ICDR read) | Not necessary | Reception by CPU (ICDR read) |
| Transfer request processing after last frame processing | 1st time: Clearing by CPU<br>2nd time: End condition issuance by CPU | Not necessary | Automatic clearing on detection of end condition during transmission of dummy data (H'FF) | Not necessary |
| Setting of number of DTC transfer data frames | Transmission: Actual data count + 1 (+1 equivalent to slave address + R/$\overline{W}$ bits) | Reception: Actual data count | Transmission: Actual data count + 1 (+1 equivalent to dummy data (H'FF)) | Reception: Actual data count |

### 16.3.9 Noise Canceler

The logic levels at the SCL and SDA pins are routed through noise cancelers before being latched internally. Figure 16.13 shows a block diagram of the noise canceler circuit.

The noise canceler consists of two cascaded latches and a match detector. The SCL (or SDA) input signal is sampled on the system clock, but is not passed forward to the next circuit unless the outputs of both latches agree. If they do not agree, the previous value is held.

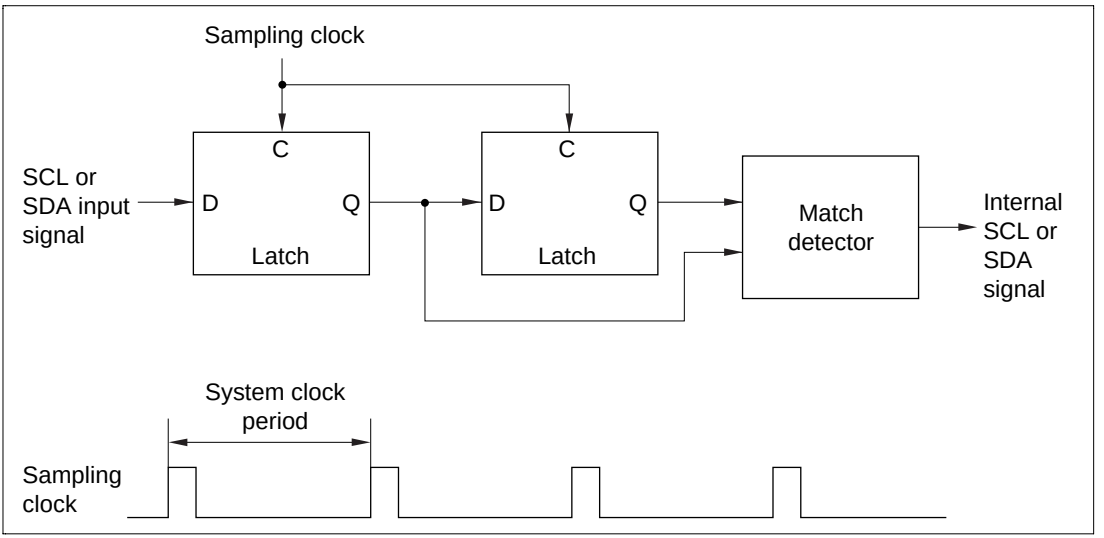



**Figure 16.13 Block Diagram of Noise Canceler**

### 16.3.10 Sample Flowcharts

Figures 16.14 to 16.17 show sample flowcharts for using the $I^2C$ bus interface in each mode.

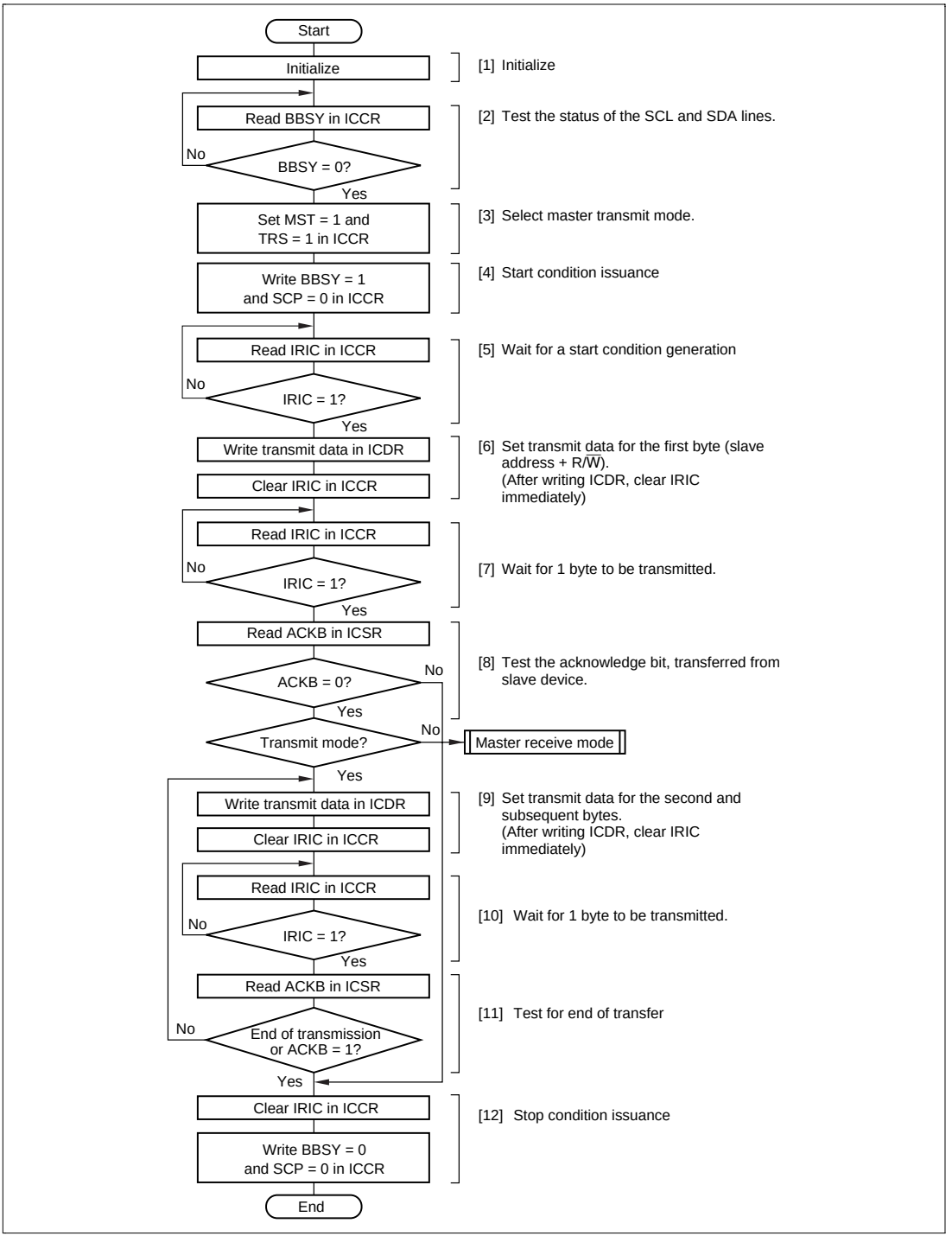



**Figure 16.14 Flowchart for Master Transmit Mode (Example)**

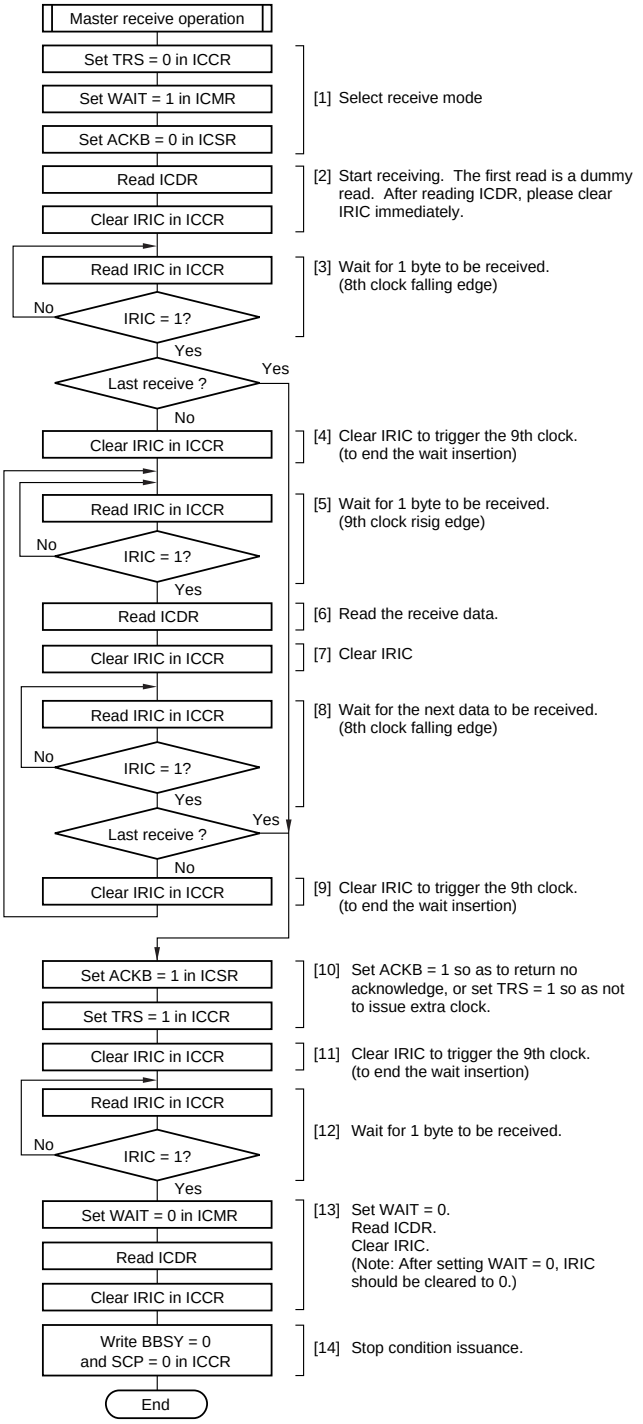



**Figure 16.15 Flowchart for Master Receive Mode (Example)**

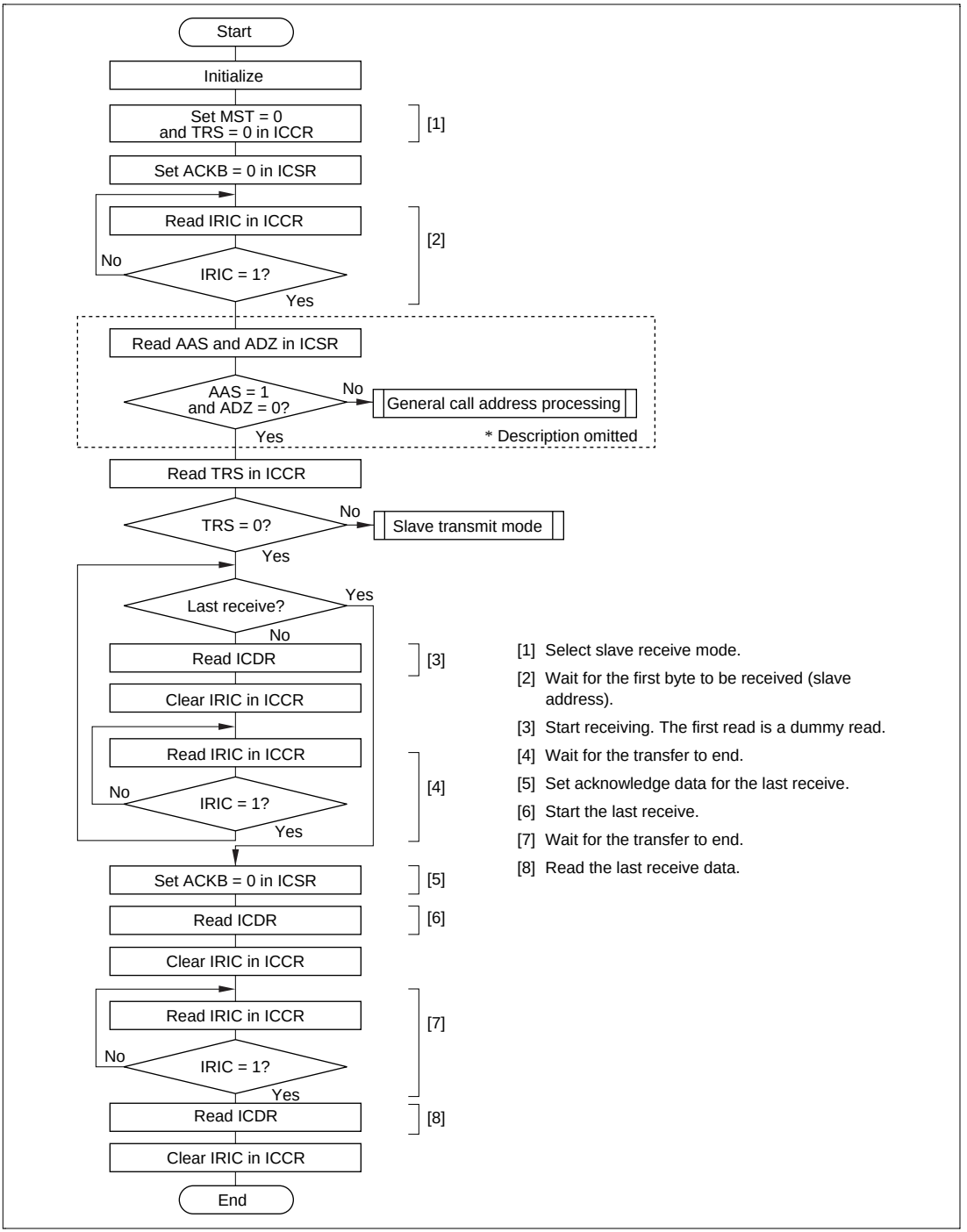



**Figure 16.16 Flowchart for Slave Receive Mode (Example)**

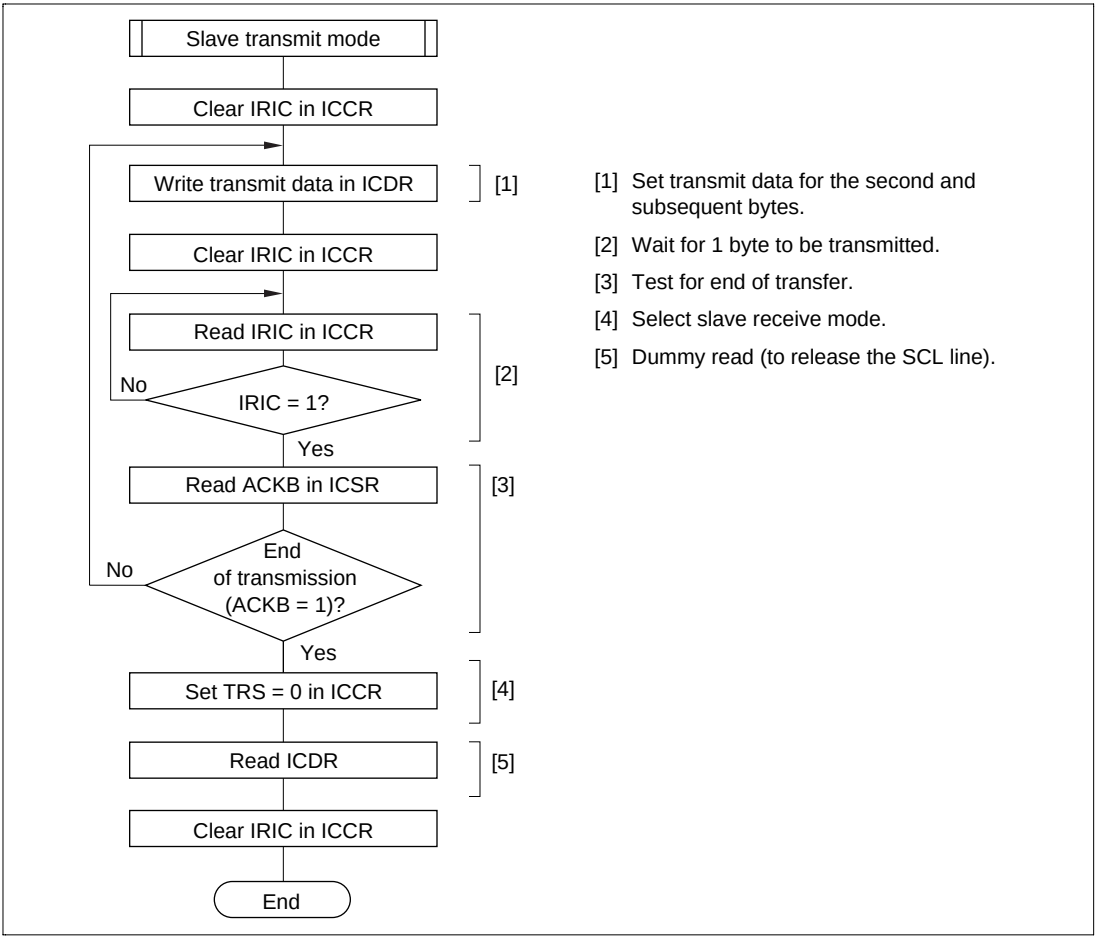



**Figure 16.17 Flowchart for Slave Transmit Mode (Example)**

### 16.3.11 Initialization of Internal State

The IIC has a function for forcible initialization of its internal state if a deadlock occurs during communication.

Initialization is executed by (1) setting bits CLR3 to CLR0 in the DDCSWR register or (2) clearing the ICE bit. For details of settings for bits CLR3 to CLR0, see section 16.2.8, DDC Switch Register (DDCSWR).

**Scope of Initialization:** The initialization executed by this function covers the following items:

- TDRE and RDRF internal flags
- Transmit/receive sequencer and internal operating clock counter

- Internal latches for retaining the output state of the SCL and SDA pins (wait, clock, data output, etc.)

The following items are not initialized:

- Actual register values (ICDR, SAR, SARX, ICMR, ICCR, ICSR, DDCSWR, STCR)
- Internal latches used to retain register read information for setting/clearing flags in the ICMR, ICCR, ICSR, and DDCSWR registers
- The value of the ICMR register bit counter (BC2 to BC0)
- Generated interrupt sources (interrupt sources transferred to the interrupt controller)

**Notes on Initialization:**

- Interrupt flags and interrupt sources are not cleared, and so flag clearing measures must be taken as necessary.
- Basically, other register flags are not cleared either, and so flag clearing measures must be taken as necessary.
- When initialization is performed by means of the DDCSWR register, the write data for bits CLR3 to CLR0 is not retained. To perform IIC clearance, bits CLR3 to CLR0 must be written to simultaneously using an MOV instruction. Do not use a bit manipulation instruction such as BCLR. Similarly, when clearing is required again, all the bits must be written to simultaneously in accordance with the setting.
- If a flag clearing setting is made during transmission/reception, the IIC module will stop transmitting/receiving at that point and the SCL and SDA pins will be released. When transmission/reception is started again, register initialization, etc., must be carried out as necessary to enable correct communication as a system.

The value of the BBSY bit cannot be modified directly by this module clear function, but since the stop condition pin waveform is generated according to the state and release timing of the SCL and SDA pins, the BBSY bit may be cleared as a result. Similarly, state switching of other bits and flags may also have an effect.

To prevent problems caused by these factors, the following procedure should be used when initializing the IIC state.

1. Execute initialization of the internal state by setting of bit CLR3 to CLR0 or by clearing ICE bit.
2. Execute a stop condition issuance instruction (write 0 to BBSY and SCP) to clear the BBSY bit to 0, and wait for two transfer rate clock cycles.
3. Re-execute initialization of the internal state by setting of bit CLR3 to CLR0 or by clearing ICE bit.
4. Initialize (re-set) the IIC registers.

## 16.4 Usage Notes

- In master mode, if an instruction to generate a start condition is immediately followed by an instruction to generate a stop condition, neither condition will be output correctly. To output consecutive start and stop conditions, after issuing the instruction that generates the start condition, read the relevant ports, check that SCL and SDA are both low, then issue the instruction that generates the stop condition. Note that SCL may not yet have gone low when BBSY is cleared to 0.

- Either of the following two conditions will start the next transfer. Pay attention to these conditions when reading or writing to ICDR.
  - Write access to ICDR when ICE = 1 and TRS = 1 (including automatic transfer from ICDRT to ICDRS)
  - Read access to ICDR when ICE = 1 and TRS = 0 (including automatic transfer from ICDRS to ICDRR)

- Table 16.6 shows the timing of SCL and SDA output in synchronization with the internal clock. Timings on the bus are determined by the rise and fall times of signals affected by the bus load capacitance, series resistance, and parallel resistance.

**Table 16.6 $I^2C$ Bus Timing (SCL and SDA Output)**

| Item | Symbol | Output Timing | Unit | Notes |
|---|---|---|---|---|
| SCL output cycle time | $t_{SCLO}$ | $28t_{cyc}$ to $256t_{cyc}$ | ns | Figure 22.24 (reference) |
| SCL output high pulse width | $t_{SCLHO}$ | $0.5t_{SCLO}$ | ns | |
| SCL output low pulse width | $t_{SCLLO}$ | $0.5t_{SCLO}$ | ns | |
| SDA output bus free time | $t_{BUFO}$ | $0.5t_{SCLO} – 1t_{cyc}$ | ns | |
| Start condition output hold time | $t_{STAHO}$ | $0.5t_{SCLO} – 1t_{cyc}$ | ns | |
| Retransmission start condition output setup time | $t_{STASO}$ | $1t_{SCLO}$ | ns | |
| Stop condition output setup time | $t_{STOSO}$ | $0.5t_{SCLO} + 2t_{cyc}$ | ns | |
| Data output setup time (master) | $t_{SDASO}$ | $1t_{SCLLO} – 3t_{cyc}$ | ns | |
| Data output setup time (slave) | | $1t_{SCLL} – (6t_{cyc}$ or $12t_{cyc}$*) | | |
| Data output hold time | $t_{SDAHO}$ | $3t_{cyc}$ | ns | |

Note: * $6t_{cyc}$ when IICX is 0, $12t_{cyc}$ when 1.

- SCL and SDA input is sampled in synchronization with the internal clock. The AC timing therefore depends on the system clock cycle $t_{cyc}$, as shown in $I^2C$ Bus Timing in section 22, Electrical Characteristics. Note that the $I^2C$ bus interface AC timing specifications will not be met with a system clock frequency of less than 5 MHz.

- The $I^2C$ bus interface specification for the SCL rise time $t_{sr}$ is under 1000 ns (300 ns for high-speed mode). In master mode, the $I^2C$ bus interface monitors the SCL line and synchronizes one bit at a time during communication. If $t_{sr}$ (the time for SCL to go from low to $V_{IH}$) exceeds the time determined by the input clock of the $I^2C$ bus interface, the high period of SCL is extended. The SCL rise time is determined by the pull-up resistance and load capacitance of the SCL line. To insure proper operation at the set transfer rate, adjust the pull-up resistance and load capacitance so that the SCL rise time does not exceed the values given in the table below.

**Table 16.7 Permissible SCL Rise Time ($t_{Sr}$) Values**

| | | | Time Indication | | | | | |
|---|---|---|---|---|---|---|---|---|
| IICX | $t_{cyc}$ Indication | | $I^2C$ Bus Specification (Max.) | ø = 5 MHz | ø = 8 MHz | ø = 10 MHz | ø = 16 MHz | ø = 20 MHz |
| 0 | $7.5t_{cyc}$ | Standard mode | 1000 ns | 1000 ns | 937 ns | 750 ns | 468 ns | 375 ns |
| | | High-speed mode | 300 ns | 300 ns | 300 ns | 300 ns | 300 ns | 300 ns |
| 1 | $17.5t_{cyc}$ | Standard mode | 1000 ns | 1000 ns | 1000 ns | 1000 ns | 1000 ns | 875 ns |
| | | High-speed mode | 300 ns | 300 ns | 300 ns | 300 ns | 300 ns | 300 ns |

- The $I^2C$ bus interface specifications for the SCL and SDA rise and fall times are under 1000 ns and 300 ns. The $I^2C$ bus interface SCL and SDA output timing is prescribed by $t_{cyc}$, as shown in table 16.6. However, because of the rise and fall times, the $I^2C$ bus interface specifications may not be satisfied at the maximum transfer rate. Table 16.8 shows output timing calculations for different operating frequencies, including the worst-case influence of rise and fall times.

  $t_{BUFO}$ fails to meet the $I^2C$ bus interface specifications at any frequency. The solution is either (a) to provide coding to secure the necessary interval (approximately 1 µs) between issuance of a stop condition and issuance of a start condition, or (b) to select devices whose input timing permits this output timing for use as slave devices connected to the $I^2C$ bus.

  $t_{SCLLO}$ in high-speed mode and $t_{STASO}$ in standard mode fail to satisfy the $I^2C$ bus interface specifications for worst-case calculations of $t_{Sr}/t_{Sf}$. Possible solutions that should be investigated include (a) adjusting the rise and fall times by means of a pull-up resistor and capacitive load, (b) reducing the transfer rate to meet the specifications, or (c) selecting devices whose input timing permits this output timing for use as slave devices connected to the $I^2C$ bus.

**Table 16.8 I²C Bus Timing (with Maximum Influence of $t_{Sr}/t_{Sf}$)**

| | | | Time Indication (at Maximum Transfer Rate) [ns] | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Item** | **$t_{cyc}$ Indication** | | **$t_{Sr}/t_{Sf}$ Influence (Max.)** | **I²C Bus Specification (Min.)** | **ø = 5 MHz** | **ø = 8 MHz** | **ø = 10 MHz** | **ø = 16 MHz** | **ø = 20 MHz** |
| $t_{SCLHO}$ | $0.5t_{SCLO}$ ($-t_{Sr}$) | Standard mode | –1000 | 4000 | 4000 | 4000 | 4000 | 4000 | 4000 |
| | | High-speed mode | –300 | 600 | 950 | 950 | 950 | 950 | 950 |
| $t_{SCLLO}$ | $0.5t_{SCLO}$ ($-t_{Sr}$) | Standard mode | –250 | 4700 | 4750 | 4750 | 4750 | 4750 | 4750 |
| | | High-speed mode | –250 | 1300 | 1000*1 | 1000*1 | 1000*1 | 1000*1 | 1000*1 |
| $t_{BUFO}$ | $0.5t_{SCLO} - 1t_{cyc}$ ($-t_{Sr}$) | Standard mode | –1000 | 4700 | 3800*1 | 3875*1 | 3900*1 | 3938*1 | 3950*1 |
| | | High-speed mode | –300 | 1300 | 750*1 | 825*1 | 850*1 | 888*1 | 900*1 |
| $t_{STAHO}$ | $0.5t_{SCLO} - 1t_{cyc}$ ($-t_{Sf}$) | Standard mode | –250 | 4000 | 4550 | 4625 | 4650 | 4688 | 4700 |
| | | High-speed mode | –250 | 600 | 800 | 875 | 900 | 938 | 950 |
| $t_{STASO}$ | $1t_{SCLO}$ ($-t_{Sr}$) | Standard mode | –1000 | 4700 | 9000 | 9000 | 9000 | 9000 | 9000 |
| | | High-speed mode | –300 | 600 | 2200 | 2200 | 2200 | 2200 | 2200 |
| $t_{STOSO}$ | $0.5t_{SCLO} + 2t_{cyc}$ ($-t_{Sr}$) | Standard mode | –1000 | 4000 | 4400 | 4250 | 4200 | 4125 | 4100 |
| | | High-speed mode | –300 | 600 | 1350 | 1200 | 1150 | 1075 | 1050 |
| $t_{SDASO}$ (master) | $1t_{SCLLO}$*3 – $3t_{cyc}$ ($-t_{Sr}$) | Standard mode | –1000 | 250 | 3100 | 3325 | 3400 | 3513 | 3550 |
| | | High-speed mode | –300 | 100 | 400 | 625 | 700 | 813 | 850 |
| $t_{SDASO}$ (slave) | $1t_{SCLL}$*3 – $12t_{cyc}$*2 ($-t_{Sr}$) | Standard mode | –1000 | 250 | 1300 | 2200 | 2500 | 2950 | 3100 |
| | | High-speed mode | –300 | 100 | –1400*1 | –500*1 | –200*1 | 250 | 400 |

| Item | $t_{cyc}$ Indication | | Time Indication (at Maximum Transfer Rate) [ns] $t_{Sr}/t_{Sf}$ Influence (Max.) | $I^2C$ Bus Specification (Min.) | ø = 5 MHz | ø = 8 MHz | ø = 10 MHz | ø = 16 MHz | ø = 20 MHz |
|---|---|---|---|---|---|---|---|---|---|
| $t_{SDAHO}$ | $3t_{cyc}$ | Standard mode | 0 | 0 | 600 | 375 | 300 | 188 | 150 |
| | | High-speed mode | 0 | 0 | 600 | 375 | 300 | 188 | 150 |

Notes: *1 Does not meet the $I^2C$ bus interface specification. Remedial action such as the following is necessary: (a) secure a start/stop condition issuance interval; (b) adjust the rise and fall times by means of a pull-up resistor and capacitive load; (c) reduce the transfer rate; (d) select slave devices whose input timing permits this output timing.

The values in the above table will vary depending on the settings of the IICX bit and bits CKS0 to CKS2. Depending on the frequency it may not be possible to achieve the maximum transfer rate; therefore whether or not the $I^2C$ bus interface specifications are met must be determined in accordance with the actual setting conditions.

*2 Value when the IICX bit is set to 1. When the IICX bit is cleared to 0, the value is ($t_{SCLL} - 6t_{cyc}$).

*3 Calculated using the $I^2C$ bus specification values (standard mode: 4700 ns min.; high-speed mode: 1300 ns min.).

- Note on ICDR Read at End of Master Reception

  To halt reception at the end of a receive operation in master receive mode, set the TRS bit to 1 and write 0 to BBSY and SCP in ICCR. This changes SDA from low to high when SCL is high, and generates the stop condition. After this, receive data can be read by means of an ICDR read, but if data remains in the buffer the ICDRS receive data will not be transferred to ICDR, and so it will not be possible to read the second byte of data.

  If it is necessary to read the second byte of data, issue the stop condition in master receive mode (i.e. with the TRS bit cleared to 0). When reading the receive data, first confirm that the BBSY bit in the ICCR register is cleared to 0, the stop condition has been generated, and the bus has been released, then read the ICDR register with TRS cleared to 0.

  Note that if the receive data (ICDR data) is read in the interval between execution of the instruction for issuance of the stop condition (writing of 0 to BBSY and SCP in ICCR) and the actual generation of the stop condition, the clock may not be output correctly in subsequent master transmission.

  Clearing of the MST bit after completion of master transmission/reception, or other modifications of IIC control bits to change the transmit/receive operating mode or settings, must be carried out during interval (a) in figure 16.18 (after confirming that the BBSY bit has been cleared to 0 in the ICCR register).

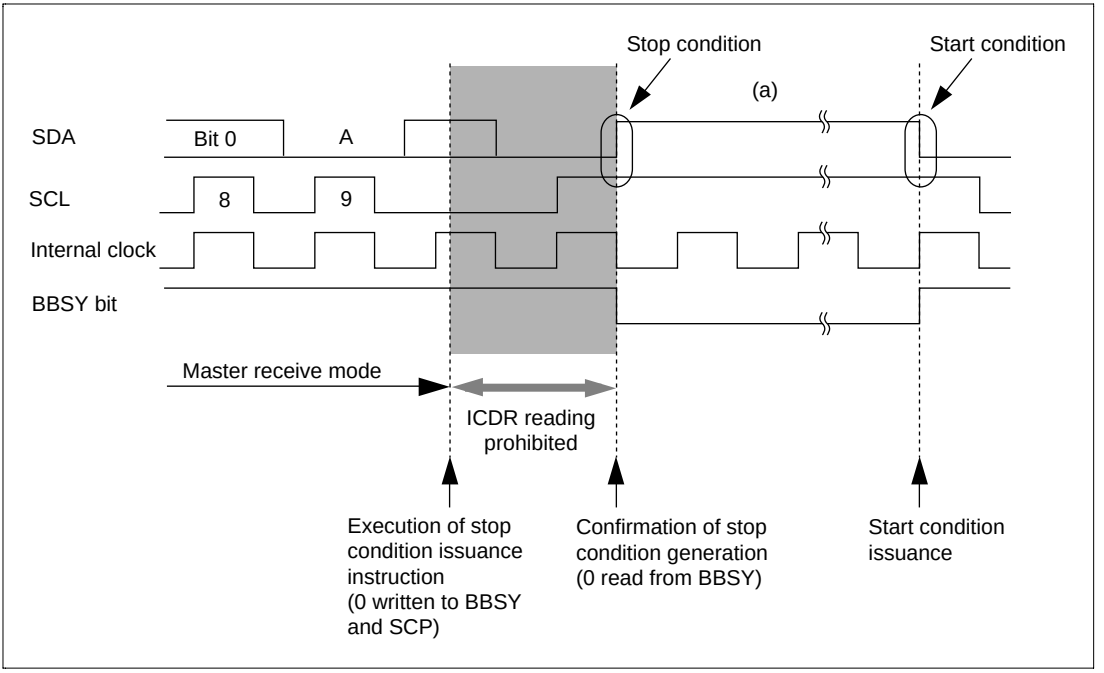
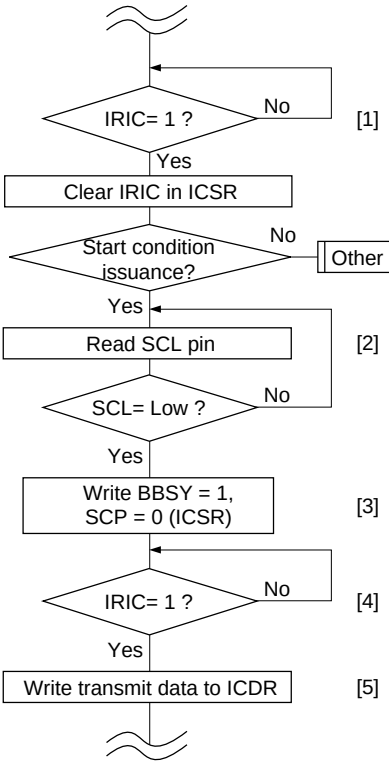



**Figure 16.18 Points for Attention Concerning Reading of Master Receive Data**

- Notes on Start Condition Issuance for Retransmission

  Figure 16-19 shows the timing of start condition issuance for retransmission, and the timing for subsequently writing data to ICDR, together with the corresponding flowchart. After start condition issuance is done and determined the start condition, write the transmit data to ICDR, as shown below.




[1] Wait for end of 1-byte transfer.

[2] Determine whether SCL is low.

[3] Issue restart condition instruction for retransmission.

[4] Determine whether start condition is generated or not.

[5] Set transmit data (slave address + R/$\overline{W}$).

Note: Program so that processing from [3] to [5] is executed continuously.

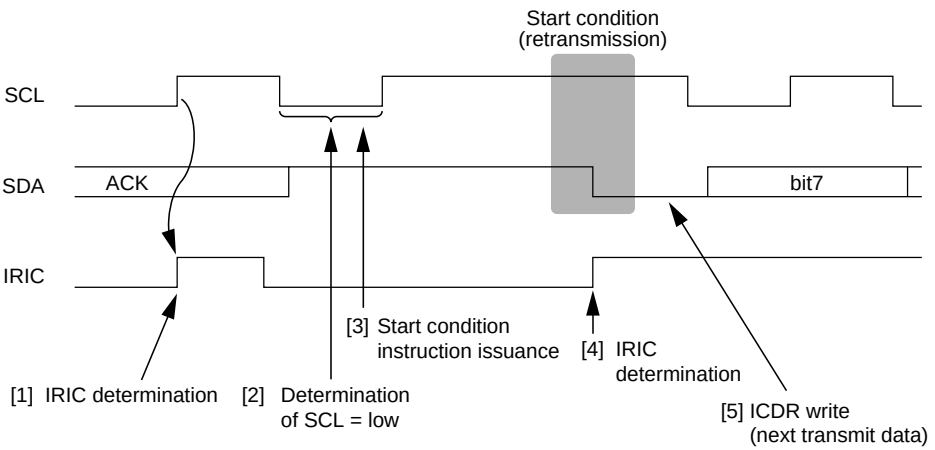



**Figure 16.19 Flowchart and Timing of Start Condition Instruction Issuance for Retransmission**

- Notes on $I^2C$ Bus Interface Stop Condition Instruction Issuance

  If the rise time of the 9th SCL clock exceeds the specification because the bus load capacitance is large, or if there is a slave device of the type that drives SCL low to effect a wait, after rising of the 9th SCL clock, issue the stop condition instruction after reading SCL and determining it to be low, as shown below.

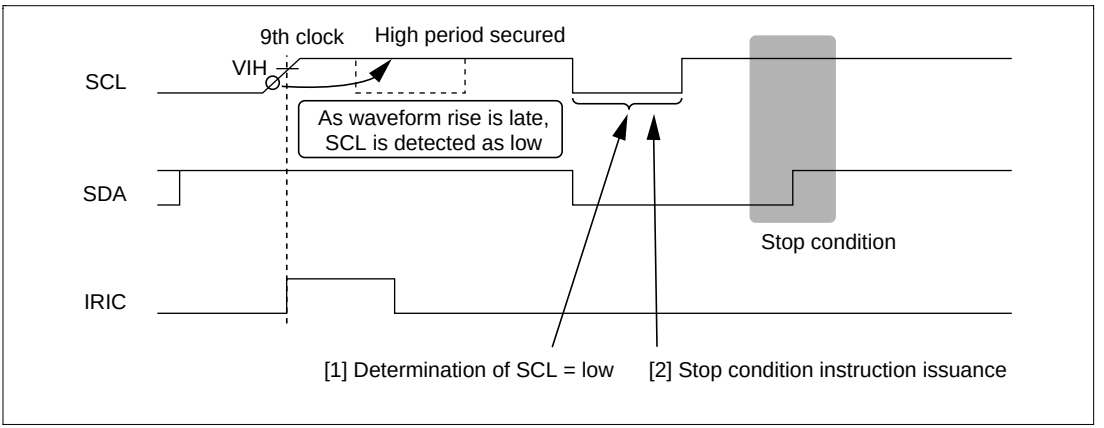



**Figure 16.20 Timing of Stop Condition Issuance**

## 22.1 Voltage of Power Supply and Operating Range

The power supply voltage and operating range (shaded part) for each product are shown in table 22.1.

**Table 22.1 Power Supply Voltage and Operating Range (1) (F-ZTAT Products)**

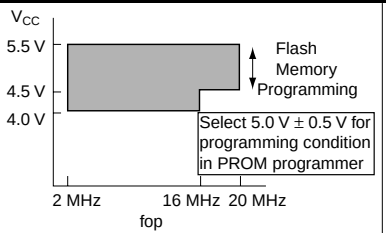
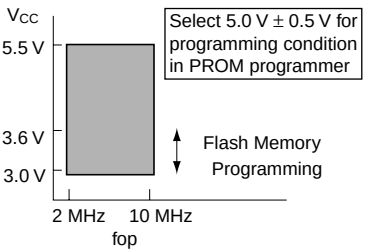
| Product/ Power supply | 5 V version | Product/ Power supply | 3 V version |
|---|---|---|---|
| HD64F2128 |  | HD64F2128V |  |
| VCC1 pin<br>VCC2 pin | $V_{CC}$ = 5.0 V ± 10% (fop = 2 to 20 MHz)<br>$V_{CC}$ = 4.0 V to 5.5 V (fop = 2 to 16 MHz) | VCC1 pin<br>VCC2 pin | $V_{CC}$ = 3.0 V to 5.5 V (fop = 2 to 10 MHz) |
| AVCC pin | $AV_{CC}$ = 5.0 V ± 10% (fop = 2 to 20 MHz)<br>$AV_{CC}$ = 4.0 V to 5.5 V (fop = 2 to 16 MHz) | AVCC pin | $AV_{CC}$ = 3.0 V to 5.5 V (fop = 2 to 10 MHz) |

**Table 22.1 Power Supply Voltage and Operating Range (2) (Mask ROM Products)**

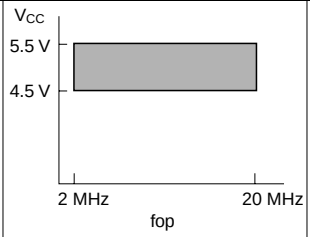
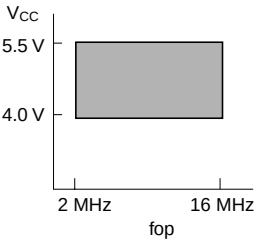
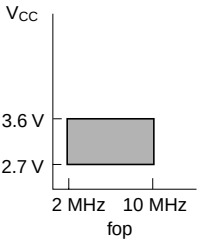
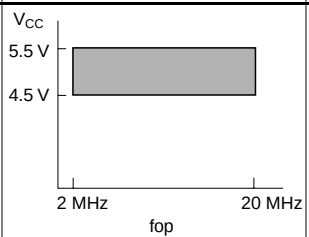
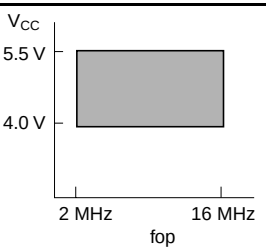
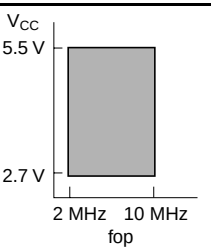
| Product/ Power supply | 5 V version | 4 V version | 3 V version |
|---|---|---|---|
| HD6432128S<br>HD6432128SW<br>HD6432127S<br>HD6432127SW |  |  |  |
| VCC1 pin | $V_{CC}$ = 5.0 V ± 10% | $V_{CC}$ = 4.0 V to 5.5 V | $V_{CC}$ = 2.7 V to 3.6 V<br>(When using CIN input, $V_{CC}$ = 3.0 V to 3.6 V) |
| VCL pin<br>(VCC2) | $V_{CL}$ = C connection | $V_{CL}$ = C connection | $V_{CL}$ = $V_{CC}$ connection |
| AVCC pin | $AV_{CC}$ = 5.0 V ± 10% | $AV_{CC}$ = 4.0 V to 5.5 V | $AV_{CC}$ = 2.7 V to 3.6 V<br>(When using CIN input, $AV_{CC}$ = 3.0 V to 3.6 V) |

**Table 22.1 Power Supply Voltage and Operating Range (3) (Mask ROM Products)**

| Product/ Power supply | 5 V version | 4 V version | 3 V version |
|---|---|---|---|
| HD6432127R<br>HD6432127RW<br>HD6432126R<br>HD6432126RW<br>HD6432122<br>HD6432120 |  |  |  |
| VCC1 pin<br>VCC2 pin | $V_{CC}$ = 5.0 V ± 10% | $V_{CC}$ = 4.0 V to 5.5 V | $V_{CC}$ = 2.7 V to 5.5 V |
| AVCC pin | $AV_{CC}$ = 5.0 V ± 10% | $AV_{CC}$ = 4.0 V to 5.5 V | $AV_{CC}$ = 2.7 V to 5.5 V |

## 22.2 Electrical Characteristics [H8S/2128 Series, H8S/2128 F-ZTAT]

### 22.2.1 Absolute Maximum Ratings

Table 22.2 lists the absolute maximum ratings.

**Table 22.2 Absolute Maximum Ratings**

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | –0.3 to +7.0 | V |
| Input voltage (except ports 6, and 7) | $V_{in}$ | –0.3 to $V_{CC}$ +0.3 | V |
| Input voltage (CIN input not selected for port 6) | $V_{in}$ | –0.3 to $V_{CC}$ +0.3 | V |
| Input voltage (CIN input selected for port 6) | $V_{in}$ | Lower voltage of –0.3 to $V_{CC}$ +0.3 and $AV_{CC}$ +0.3 | V |
| Input voltage (port 7) | $V_{in}$ | –0.3 to $AV_{CC}$ + 0.3 | V |
| Analog power supply voltage | $AV_{CC}$ | –0.3 to +7.0 | V |
| Analog input voltage | $V_{AN}$ | –0.3 to $AV_{CC}$ +0.3 | V |
| Operating temperature | $T_{opr}$ | Regular specifications: –20 to +75 | °C |
| | | Wide-range specifications: –40 to +85 | °C |
| Operating temperature (Flash memory programming/ erasing) | $T_{opr}$ | Regular specifications: 0 to +75 | °C |
| | | Wide-range specifications: 0 to +85 | |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C |

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

### 22.2.2 DC Characteristics

Table 22.3 lists the DC characteristics. Table 22.4 lists the permissible output currents.

**Table 22.3 DC Characteristics (1)**

Conditions: $V_{CC}$ = 5.0 V ± 10%, $AV_{CC}$*1 = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$*1 = 0 V,
$T_a$ = –20 to +75°C*8 (regular specifications),
$T_a$ = –40 to +85°C*8 (wide-range specifications)

| Item | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60*2 *5, $\overline{IRQ2}$ to $\overline{IRQ0}$*3 | (1) | $V_T^-$ | 1.0 | — | — | V | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | 0.4 | — | — | V | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0 | (2) | $V_{IH}$ | $V_{CC}$ – 0.7 | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | Port 7 | | | 2.0 | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | | 2.0 | — | $V_{CC}$ +0.3 | V | |
| Input low voltage | $\overline{RES}$, $\overline{STBY}$, MD1, MD0 | (3) | $V_{IL}$ | –0.3 | — | 0.5 | V | |
| | NMI, EXTAL, input pins except (1) and (3) above | | | –0.3 | — | 0.8 | V | |
| Output high voltage | All output pins (except P47, and P52*4) | | $V_{OH}$ | $V_{CC}$ – 0.5 | — | — | V | $I_{OH}$ = –200 µA |
| | | | | 3.5 | — | — | V | $I_{OH}$ = –1 mA |
| | P47, P52*4 | | | 2.5 | — | — | V | $I_{OH}$ = –1 mA |
| Output low voltage | All output pins | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | Ports 1 to 3 | | | — | — | 1.0 | V | $I_{OL}$ = 10 mA |
| Input leakage current | $\overline{RES}$ | | $\lvert I_{in} \rvert$ | — | — | 10.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| | $\overline{STBY}$, NMI, MD1, MD0 | | | — | — | 1.0 | µA | |
| | Port 7 | | | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $AV_{CC}$ – 0.5 V |

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Three-state leakage current (off state) | Ports 1 to 6 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| Input pull-up MOS current | Ports 1 to 3 | $-I_P$ | 50 | — | 300 | µA | $V_{in}$ = 0 V |
| Input capacitance | $\overline{RES}$ (4) | $C_{in}$ | — | — | 80 | pF | $V_{in}$ = 0 V<br>f = 1 MHz<br>$T_a$ = 25°C |
| | NMI | | — | — | 50 | pF | |
| | P52, P47, P24, P23 | | — | — | 20 | pF | |
| | Input pins except (4) above | | — | — | 15 | pF | |
| Current dissipation*6 | Normal operation | $I_{CC}$ | — | 70 | 90 | mA | f = 20 MHz |
| | Sleep mode | | — | 55 | 75 | mA | f = 20 MHz |
| | Standby mode*7 | | — | 0.01 | 5.0 | µA | $T_a \leq 50°C$ |
| | | | — | — | 20.0 | µA | 50°C < $T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 1.5 | 3.0 | mA | |
| | Idle | | — | 0.01 | 5.0 | µA | $AV_{CC}$ = 2.0 V to 5.5 V |
| Analog power supply voltage*1 | | $AV_{CC}$ | 4.5 | — | 5.5 | V | Operating |
| | | | 2.0 | — | 5.5 | V | Idle/not used |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: *1 Do not leave the $AV_{CC}$, and $AV_{SS}$ pins open even if the A/D converter is not used.
Even if the A/D converter is not used, apply a value in the range 2.0 V to 5.5 V to $AV_{CC}$ by connection to the power supply ($V_{CC}$), or some other method.

*2 P67 to P60 include supporting module inputs multiplexed on those pins.

*3 $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

*4 In the H8S/2128 Series, P52/SCK0/SCL0 and P47/SDA0 are NMOS push-pull outputs.
An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).
In the H8S/2128 Series, P52/SCK0 and P47 (ICE = 0) high levels are driven by NMOS.

*5 The upper limit of the port 6 applied voltage is $V_{CC}$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}$ + 0.3 V and $AV_{CC}$ + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

*6 Current dissipation values are for $V_{IH}$ min = $V_{CC}$ – 0.5 V and $V_{IL}$ max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

*7 The values are for $V_{RAM} \leq V_{CC} < 4.5$ V, $V_{IH}$ min = $V_{CC} \times 0.9$, and $V_{IL}$ max = 0.3 V.

*8 For flash memory program/erase operations, the applicable range is $T_a$ = 0 to +75°C (regular specifications) or $T_a$ = 0 to +85°C (wide-range specifications).

**Table 22.3 DC Characteristics (2)**

Conditions: $V_{CC}$ = 4.0 V to 5.5 V*[8], $AV_{CC}$*[1] = 4.0 V to 5.5 V, $V_{SS}$ = $AV_{SS}$*[1] = 0 V,
$T_a$ = –20 to +75°C*[8] (regular specifications),
$T_a$ = –40 to +85°C*[8] (wide-range specifications)

| Item | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60*[2] *[5], $\overline{IRQ2}$ to $\overline{IRQ0}$*[3] | (1) | $V_T^-$ | 1.0 | — | — | V | $V_{CC}$ = 4.5 V to 5.5 V |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | 0.4 | — | — | V | |
| | | | $V_T^-$ | 0.8 | — | — | V | $V_{CC}$ < 4.5 V |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | 0.3 | — | — | V | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0 | (2) | $V_{IH}$ | $V_{CC}$ – 0.7 | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | Port 7 | | | 2.0 | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | | 2.0 | — | $V_{CC}$ +0.3 | V | |
| Input low voltage | $\overline{RES}$, $\overline{STBY}$, MD1, MD0 | (3) | $V_{IL}$ | –0.3 | — | 0.5 | V | |
| | NMI, EXTAL, input pins except (1) and (3) above | | | –0.3 | — | 0.8 | V | |
| Output high voltage | All output pins (except P47, and P52*[4]) | | $V_{OH}$ | $V_{CC}$ – 0.5 | — | — | V | $I_{OH}$ = –200 µA |
| | | | | 3.5 | — | — | V | $I_{OH}$ = –1 mA, $V_{CC}$= 4.5 V to 5.5 V |
| | | | | 3.0 | — | — | V | $I_{OH}$ = –1 mA, $V_{CC}$ < 4.5 V |
| | P47, P52*[4] | | | 2.0 | — | — | V | $I_{OH}$ = –1 mA |
| Output low voltage | All output pins | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | Ports 1 to 3 | | | — | — | 1.0 | V | $I_{OL}$ = 10 mA |
| Input leakage current | $\overline{RES}$ | | $\lvert I_{in} \rvert$ | — | — | 10.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| | $\overline{STBY}$, NMI, MD1, MD0 | | | — | — | 1.0 | µA | |
| | Port 7 | | | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $AV_{CC}$ – 0.5 V |

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Three-state leakage current (off state) | Ports 1 to 6 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| Input pull-up MOS current | Ports 1 to 3 | $-I_P$ | 50 | — | 300 | µA | $V_{in}$ = 0 V, $V_{CC}$ = 4.5 V to 5.5 V |
| | | | 30 | — | 200 | µA | $V_{in}$ = 0 V, $V_{CC}$ < 4.5 V |
| Input capacitance | $\overline{RES}$ (4) | $C_{in}$ | — | — | 80 | pF | $V_{in}$ = 0 V, f = 1 MHz, $T_a$ = 25°C |
| | NMI | | — | — | 50 | pF | |
| | P52, P47, P24, P23 | | — | — | 20 | pF | |
| | Input pins except (4) above | | — | — | 15 | pF | |
| Current dissipation*6 | Normal operation | $I_{CC}$ | — | 55 | 75 | mA | f = 16 MHz |
| | Sleep mode | | — | 42 | 62 | mA | f = 16 MHz |
| | Standby mode*7 | | — | 0.01 | 5.0 | µA | $T_a \leq$ 50°C |
| | | | — | — | 20.0 | µA | 50°C < $T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 1.5 | 3.0 | mA | |
| | Idle | | — | 0.01 | 5.0 | µA | $AV_{CC}$ = 2.0 V to 5.5 V |
| Analog power supply voltage*1 | | $AV_{CC}$ | 4.0 | — | 5.5 | V | Operating |
| | | | 2.0 | — | 5.5 | V | Idle/not used |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: *1 Do not leave the $AV_{CC}$, and $AV_{SS}$ pins open even if the A/D converter is not used.
Even if the A/D converter is not used, apply a value in the range 2.0 V to 5.5 V to $AV_{CC}$ by connection to the power supply ($V_{CC}$), or some other method.

*2 P67 to P60 include supporting module inputs multiplexed on those pins.

*3 $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

*4 In the H8S/2128 Series, P52/SCK0/SCL0 and P47/SDA0 are NMOS push-pull outputs.
An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).
In the H8S/2128 Series, P52/SCK0 and P47 (ICE = 0) high levels are driven by NMOS.

*5 The upper limit of the port 6 applied voltage is $V_{CC}$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}$ + 0.3 V and $AV_{CC}$ + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

*6 Current dissipation values are for $V_{IH}$ min = $V_{CC}$ – 0.5 V and $V_{IL}$ max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

*7 The values are for $V_{RAM} \leq V_{CC} < 4.0$ V, $V_{IH}$ min = $V_{CC} \times 0.9$, and $V_{IL}$ max = 0.3 V.

*8 For flash memory program/erase operations, the applicable ranges are $V_{CC}$ = 4.5 V to 5.5 V and $T_a$ = 0 to +75°C (regular specifications) or $T_a$ = 0 to +85°C (wide-range specifications).

**Table 22.3 DC Characteristics (3)**

Conditions (Mask ROM version): $V_{CC}$ = 2.7 V to 5.5 V, $AV_{CC}$*1 = 2.7 V to 5.5 V, $V_{SS}$ = $AV_{SS}$*1 = 0 V, $T_a$ = –20 to +75°C

(Flash memory version): $V_{CC}$ = 3.0 V to 5.5 V, $AV_{CC}$*1 = 3.0 V to 5.5 V, $V_{SS}$ = $AV_{SS}$*1 = 0 V, $T_a$ = –20 to +75°C*8

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60*2 *5, (1) $\overline{IRQ2}$ to $\overline{IRQ0}$*3 | $V_T^-$ | $V_{CC} \times 0.2$ | — | — | V | |
| | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | $V_T^+ - V_T^-$ | $V_{CC} \times 0.05$ | — | — | V | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, (2) NMI, MD1, MD0 | $V_{IH}$ | $V_{CC} \times 0.9$ | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | Port 7 | | $V_{CC} \times 0.7$ | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| Input low voltage | $\overline{RES}$, $\overline{STBY}$, (3) MD1, MD0 | $V_{IL}$ | –0.3 | — | $V_{CC} \times 0.1$ | V | |
| | NMI, EXTAL, input pins except (1) and (3) above | | –0.3 | — | $V_{CC} \times 0.2$ | V | $V_{CC}$ < 4.0 V |
| | | | | | 0.8 | V | $V_{CC}$ = 4.0 V to 5.5 V |
| Output high voltage | All output pins (except P47, and P52*4) | $V_{OH}$ | $V_{CC}$ – 0.5 | — | — | V | $I_{OH}$ = –200 µA |
| | | | $V_{CC}$ – 1.0 | — | — | V | $I_{OH}$ = –1 mA ($V_{CC}$ < 4.0 V) |
| | P47, P52*4 | | 1.0 | — | — | V | $I_{OH}$ = –1 mA |
| Output low voltage | All output pins | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | Ports 1 to 3 | | — | — | 1.0 | V | $I_{OL}$ = 5 mA ($V_{CC}$ < 4.0 V), $I_{OL}$ = 10 mA (4.0 V ≤ $V_{CC}$ ≤ 5.5 V) |
| Input leakage current | $\overline{RES}$ | $\lvert I_{in} \rvert$ | — | — | 10.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| | $\overline{STBY}$, NMI, MD1, MD0 | | — | — | 1.0 | µA | |
| | Port 7 | | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $AV_{CC}$ – 0.5 V |

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Three-state leakage current (off state) | Ports 1 to 6 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| Input pull-up MOS current | Ports 1 to 3 | $-I_P$ | 10 | — | 150 | µA | $V_{in}$ = 0 V, $V_{CC}$ = 2.7 V to 3.6 V |
| Input capacitance | $\overline{RES}$ (4) | $C_{in}$ | — | — | 80 | pF | $V_{in}$ = 0 V, f = 1 MHz, Ta = 25°C |
| | NMI | | — | — | 50 | pF | |
| | P52, P47, P24, P23 | | — | — | 20 | pF | |
| | Input pins except (4) above | | — | — | 15 | pF | |
| Current dissipation*6 | Normal operation | $I_{CC}$ | — | 40 | 52 | mA | f = 10 MHz |
| | Sleep mode | | — | 30 | 42 | mA | f = 10 MHz |
| | Standby mode*7 | | — | 0.01 | 5.0 | µA | $T_a \leq 50°C$ |
| | | | — | — | 20.0 | µA | $50°C < T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 1.5 | 3.0 | mA | |
| | Idle | | — | 0.01 | 5.0 | µA | $AV_{CC}$ = 2.0 V to 5.5 V |
| Analog power supply voltage*1 | | $AV_{CC}$ | 2.7 | — | 5.5 | V | Operating |
| | | | 2.0 | — | 5.5 | V | Idle/not used |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: *1 Do not leave the $AV_{CC}$, and $AV_{SS}$ pins open even if the A/D converter is not used.
Even if the A/D converter is not used, apply a value in the range 2.0 V to 5.5 V to $AV_{CC}$ by connection to the power supply ($V_{CC}$), or some other method.

*2 P67 to P60 include supporting module inputs multiplexed on those pins.

*3 $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

*4 In the H8S/2128 Series, P52/SCK0/SCL0 and P47/SDA0 are NMOS push-pull outputs.
An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).
In the H8S/2128 Series, P52/SCK0 and P47 (ICE = 0) high levels are driven by NMOS.

*5 The upper limit of the port 6 applied voltage is $V_{CC}$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}$ + 0.3 V and $AV_{CC}$ + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

*6 Current dissipation values are for $V_{IH}$ min = $V_{CC}$ – 0.5 V and $V_{IL}$ max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

*7 The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, $V_{IH}$ min = $V_{CC} \times 0.9$, and $V_{IL}$ max = 0.3 V.

*8 For flash memory program/erase operations, the applicable range is $V_{CC}$ = 3.0 V to 3.6 V and $T_a$ = 0 to +75°C.

**Table 22.4 Permissible Output Currents**

Conditions: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, Ta = –20 to +75°C (regular specifications), Ta = –40 to +85°C (wide-range specifications)

| Item | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Permissible output low current (per pin) | SCL1, SCL0, SDA1, SDA0 | $I_{OL}$ | — | — | 20 | mA |
| | Ports 1, 2, 3 | | — | — | 10 | mA |
| | Other output pins | | — | — | 2 | mA |
| Permissible output low current (total) | Total of ports 1, 2, and 3 | $\Sigma I_{OL}$ | — | — | 80 | mA |
| | Total of all output pins, including the above | | — | — | 120 | mA |
| Permissible output high current (per pin) | All output pins | $-I_{OH}$ | — | — | 2 | mA |
| Permissible output high current (total) | Total of all output pins | $\Sigma -I_{OH}$ | — | — | 40 | mA |

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22.4.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 22.1 and 22.2.

**Table 22.4 Permissible Output Currents (cont)**

Conditions: $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V, Ta = –20 to +75°C

| Item | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Permissible output low current (per pin) | SCL1, SCL0, SDA1, SDA0 | $I_{OL}$ | — | — | 10 | mA |
| | Ports 1, 2, 3 | | — | — | 2 | mA |
| | Other output pins | | — | — | 1 | mA |
| Permissible output low current (total) | Total of ports 1, 2, and 3 | $\Sigma I_{OL}$ | — | — | 40 | mA |
| | Total of all output pins, including the above | | — | — | 60 | mA |
| Permissible output high current (per pin) | All output pins | $-I_{OH}$ | — | — | 2 | mA |
| Permissible output high current (total) | Total of all output pins | $\Sigma -I_{OH}$ | — | — | 30 | mA |

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22.4.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 22.1 and 22.2.

**Table 22.5 Bus Drive Characteristics**

Conditions: $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V

Applicable Pins: SCL1, SCL0, SDA1, SDA0 (bus drive function selected)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | $V_T^-$ | $V_{CC} \times 0.3$ | — | — | V | $V_{CC}$ = 2.7 V to 5.5 V |
| | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | | $V_{CC}$ = 2.7 V to 5.5 V |
| | $V_T^+ - V_T^-$ | $V_{CC} \times 0.05$ | — | — | | $V_{CC}$ = 2.7 V to 5.5 V |
| Input high voltage | $V_{IH}$ | $V_{CC} \times 0.7$ | — | $V_{CC}$ + 0.5 | V | $V_{CC}$ = 2.7 V to 5.5 V |
| Input low voltage | $V_{IL}$ | –0.5 | — | $V_{CC} \times 0.3$ | | $V_{CC}$ = 2.7 V to 5.5 V |
| Output low voltage | $V_{OL}$ | — | — | 0.8 | V | $I_{OL}$ = 16 mA, $V_{CC}$ = 4.5 V to 5.5 V |
| | | — | — | 0.5 | | $I_{OL}$ = 8 mA |
| | | — | — | 0.4 | | $I_{OL}$ = 3 mA |
| Input capacitance | $C_{in}$ | — | — | 20 | pF | $V_{in}$ = 0 V, f = 1 MHz, $T_a$ = 25°C |
| Three-state leakage current (off state) | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| SCL, SDA output fall time | $t_{Of}$ | 20 + 0.1Cb | — | 250 | ns | $V_{CC}$ = 2.7 V to 5.5 V |

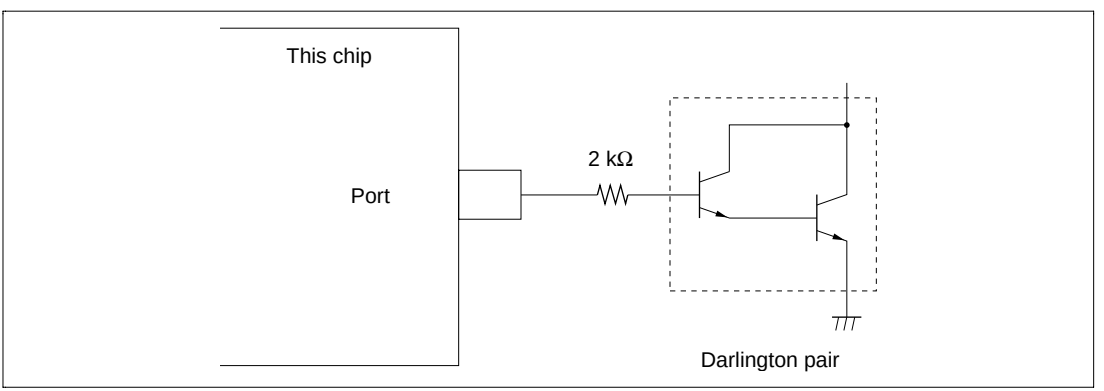



**Figure 22.1 Darlington Pair Drive Circuit (Example)**

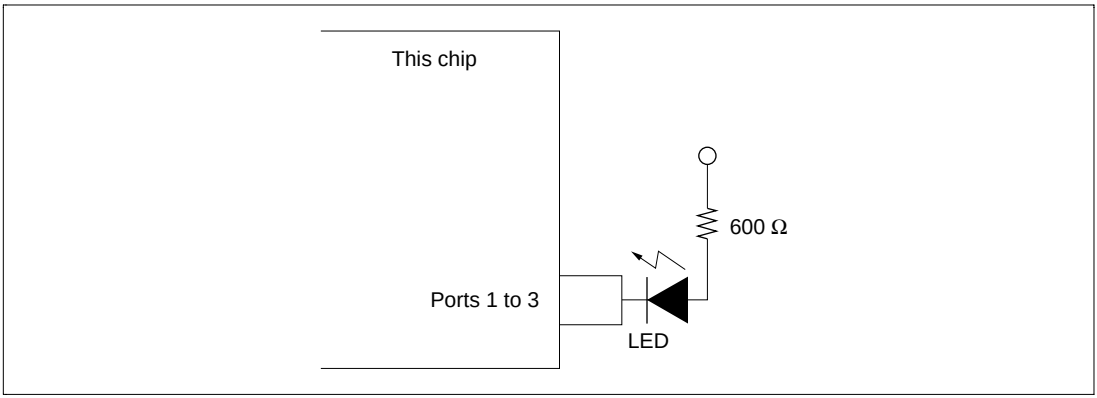



**Figure 22.2 LED Drive Circuit (Example)**

### 22.2.3 AC Characteristics

Figure 22.3 shows the test conditions for the AC characteristics.

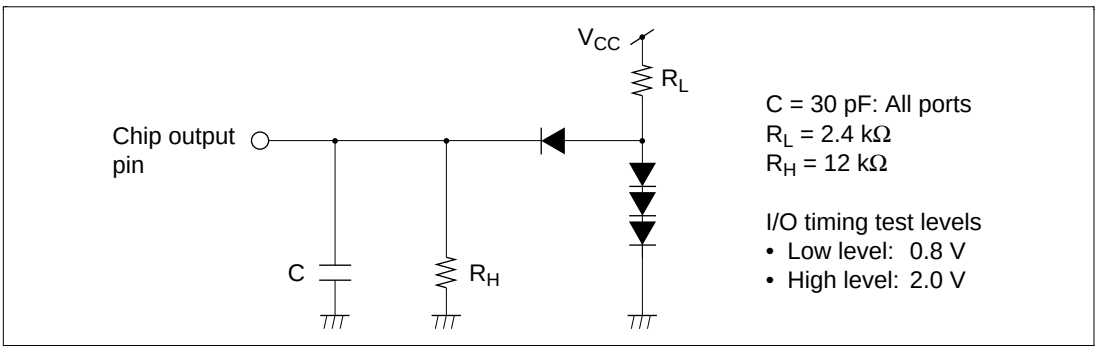



**Figure 22.3 Output Load Circuit**

### (1) Clock Timing

Table 22.6 shows the clock timing. The clock timing specified here covers clock (ø) output and clock pulse generator (crystal) and external clock input (EXTAL pin) oscillation settling times. For details of external clock input (EXTAL pin and EXCL pin) timing, see section 20, Clock Pulse Generator.

**Table 22.6 Clock Timing**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V*, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | Test |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Conditions |
| Clock cycle time | $t_{cyc}$ | 50 | 500 | 62.5 | 500 | 100 | 500 | ns | Figure 22.4 |
| Clock high pulse width | $t_{CH}$ | 17 | — | 20 | — | 30 | — | ns | Figure 22.4 |
| Clock low pulse width | $t_{CL}$ | 17 | — | 20 | — | 30 | — | ns | |
| Clock rise time | $t_{Cr}$ | — | 8 | — | 10 | — | 20 | ns | |
| Clock fall time | $t_{Cf}$ | — | 8 | — | 10 | — | 20 | ns | |
| Oscillation settling time at reset (crystal) | $t_{OSC1}$ | 10 | — | 10 | — | 20 | — | ms | Figure 22.5<br>Figure 22.6 |
| Oscillation settling time in software standby (crystal) | $t_{OSC2}$ | 8 | — | 8 | — | 8 | — | ms | |
| External clock output stabilization delay time | $t_{DEXT}$ | 500 | — | 500 | — | 500 | — | µs | |

Note: * For the low-voltage F-ZTAT version, $V_{CC}$ = 3.0 V to 5.5 V.

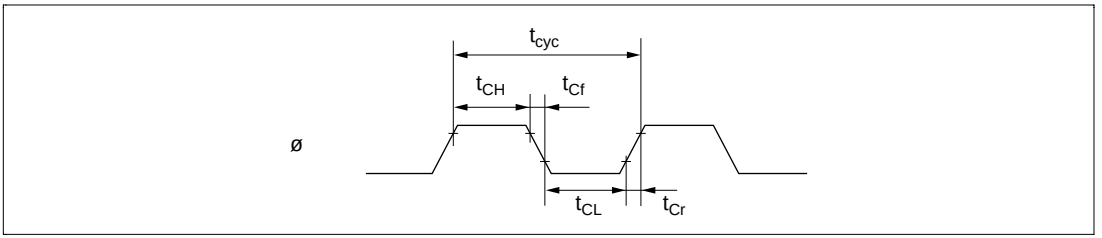



**Figure 22.4 System Clock Timing**

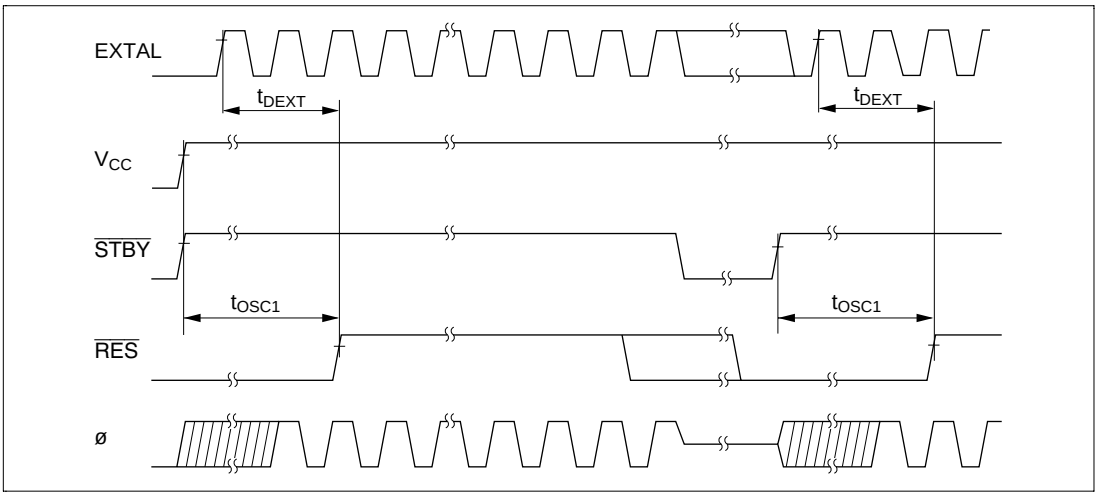



**Figure 22.5 Oscillation Settling Timing**

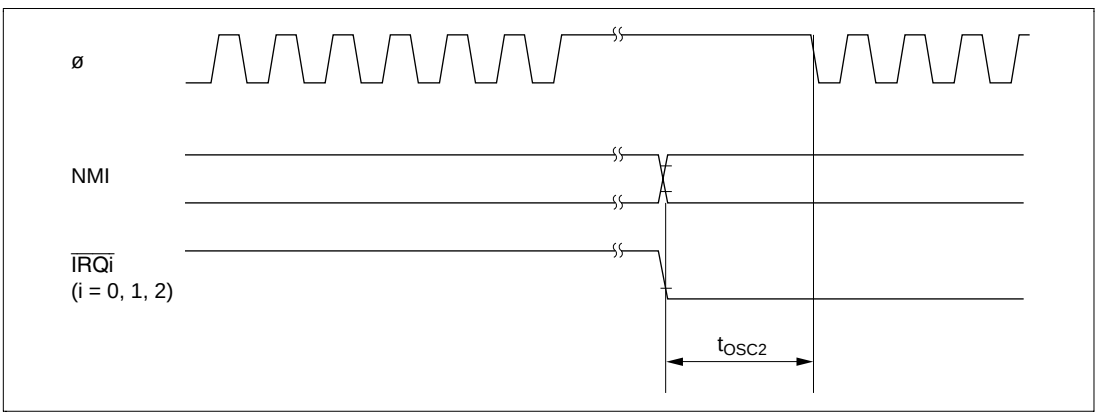



**Figure 22.6 Oscillation Setting Timing (Exiting Software Standby Mode)**

### (2) Control Signal Timing

Table 22.7 shows the control signal timing. The only external interrupts that can operate on the subclock (ø = 32.768 kHz) are NMI and IRQ0, 1, and IRQ2.

**Table 22.7 Control Signal Timing**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V*, $V_{SS}$ = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C

| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | Test |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Conditions |
| $\overline{RES}$ setup time | $t_{RESS}$ | 200 | — | 200 | — | 300 | — | ns | Figure 22.7 |
| $\overline{RES}$ pulse width | $t_{RESW}$ | 20 | — | 20 | — | 20 | — | $t_{cyc}$ | |
| NMI setup time (NMI) | $t_{NMIS}$ | 150 | — | 150 | — | 250 | — | ns | Figure 22.8 |
| NMI hold time (NMI) | $t_{NMIH}$ | 10 | — | 10 | — | 10 | — | ns | |
| NMI pulse width (exiting software standby mode) | $t_{NMIW}$ | 200 | — | 200 | — | 200 | — | ns | |
| IRQ setup time ($\overline{IRQ2}$ to $\overline{IRQ0}$) | $t_{IRQS}$ | 150 | — | 150 | — | 250 | — | ns | |
| IRQ hold time ($\overline{IRQ2}$ to $\overline{IRQ0}$) | $t_{IRQH}$ | 10 | — | 10 | — | 10 | — | ns | |
| IRQ pulse width ($\overline{IRQ2}$ to $\overline{IRQ0}$) (exiting software standby mode) | $t_{IRQW}$ | 200 | — | 200 | — | 200 | — | ns | |

Note: * For the low-voltage F-ZTAT version, $V_{CC}$ = 3.0 V to 5.5 V.

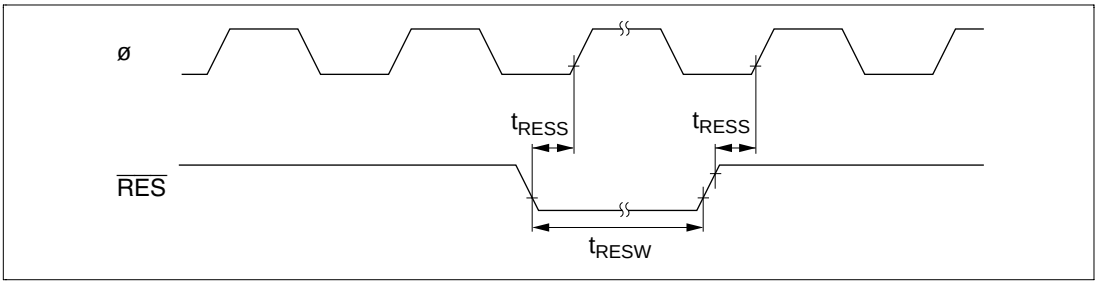



**Figure 22.7 Reset Input Timing**

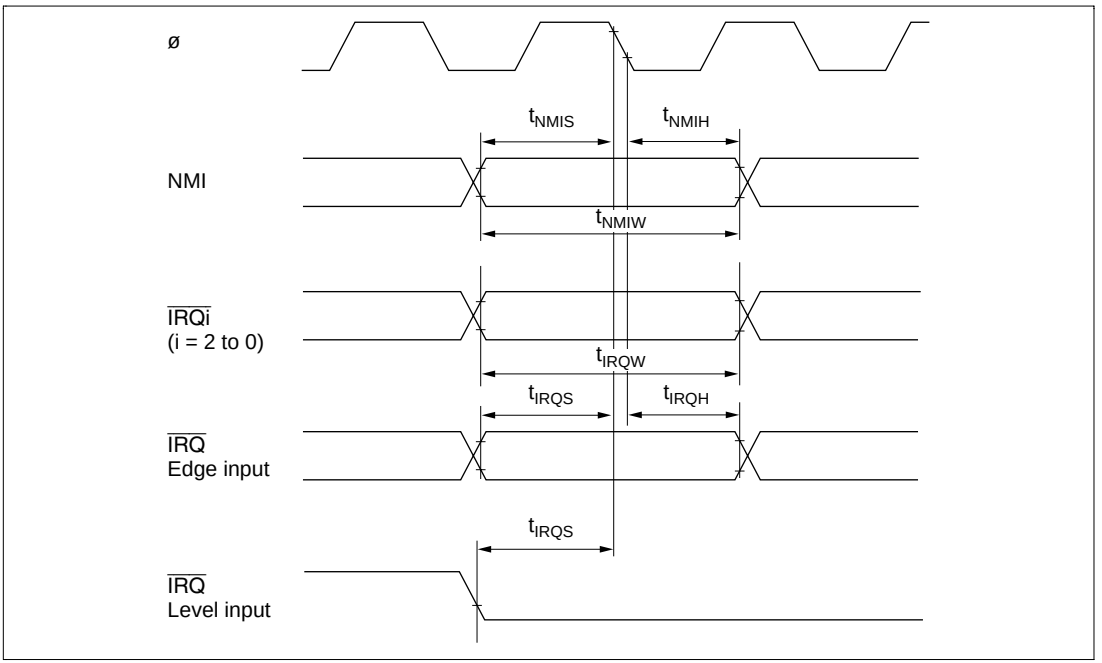



**Figure 22.8 Interrupt Input Timing**

### (3) Bus Timing

Table 22.8 shows the bus timing. Operation in external expansion mode is not guaranteed when operating on the subclock (ø = 32.768 kHz).

**Table 22.8 Bus Timing**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

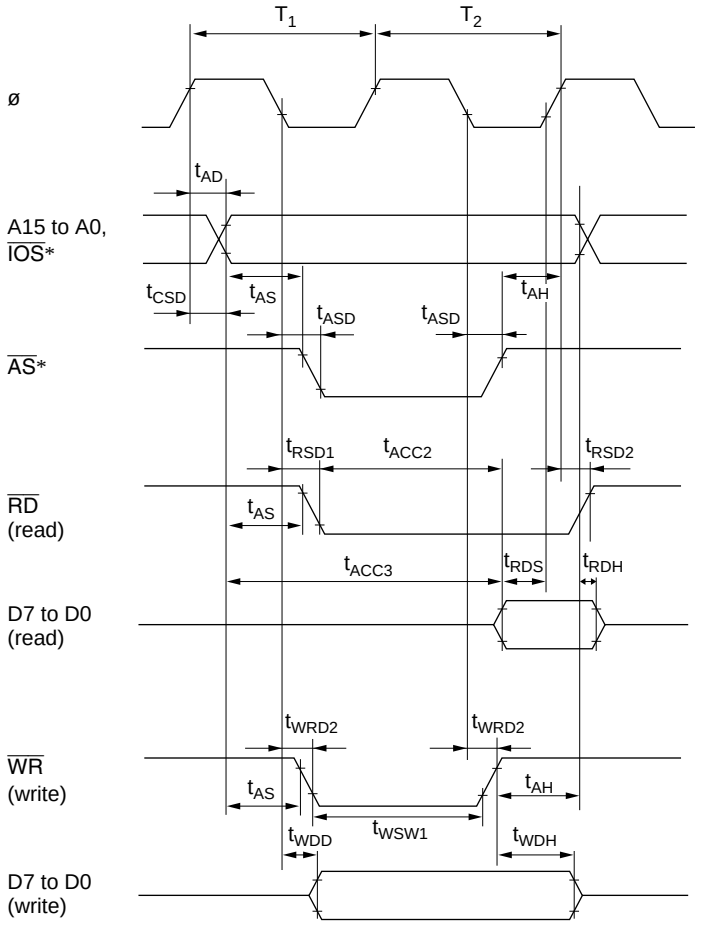
Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V*, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | Test |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Conditions |
| Address delay time | $t_{AD}$ | — | 20 | — | 30 | — | 40 | ns | Figure 22.9 to figure 22.13 |
| Address setup time | $t_{AS}$ | 0.5 × $t_{cyc}$ – 15 | — | 0.5 × $t_{cyc}$ – 20 | — | 0.5 × $t_{cyc}$ – 30 | — | ns | |
| Address hold time | $t_{AH}$ | 0.5 × $t_{cyc}$ – 10 | — | 0.5 × $t_{cyc}$ – 15 | — | 0.5 × $t_{cyc}$ – 20 | — | ns | |
| $\overline{CS}$ delay time ($\overline{IOS}$) | $t_{CSD}$ | — | 20 | — | 30 | — | 40 | ns | |
| $\overline{AS}$ delay time | $t_{ASD}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{RD}$ delay time 1 | $t_{RSD1}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{RD}$ delay time 2 | $t_{RSD2}$ | — | 30 | — | 45 | — | 60 | ns | |
| Read data setup time | $t_{RDS}$ | 15 | — | 20 | — | 35 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read data access time 1 | $t_{ACC1}$ | — | 1.0 × $t_{cyc}$ – 30 | — | 1.0 × $t_{cyc}$ – 40 | — | 1.0 × $t_{cyc}$ – 60 | ns | |
| Read data access time 2 | $t_{ACC2}$ | — | 1.5 × $t_{cyc}$ – 25 | — | 1.5 × $t_{cyc}$ – 35 | — | 1.5 × $t_{cyc}$ – 50 | ns | |

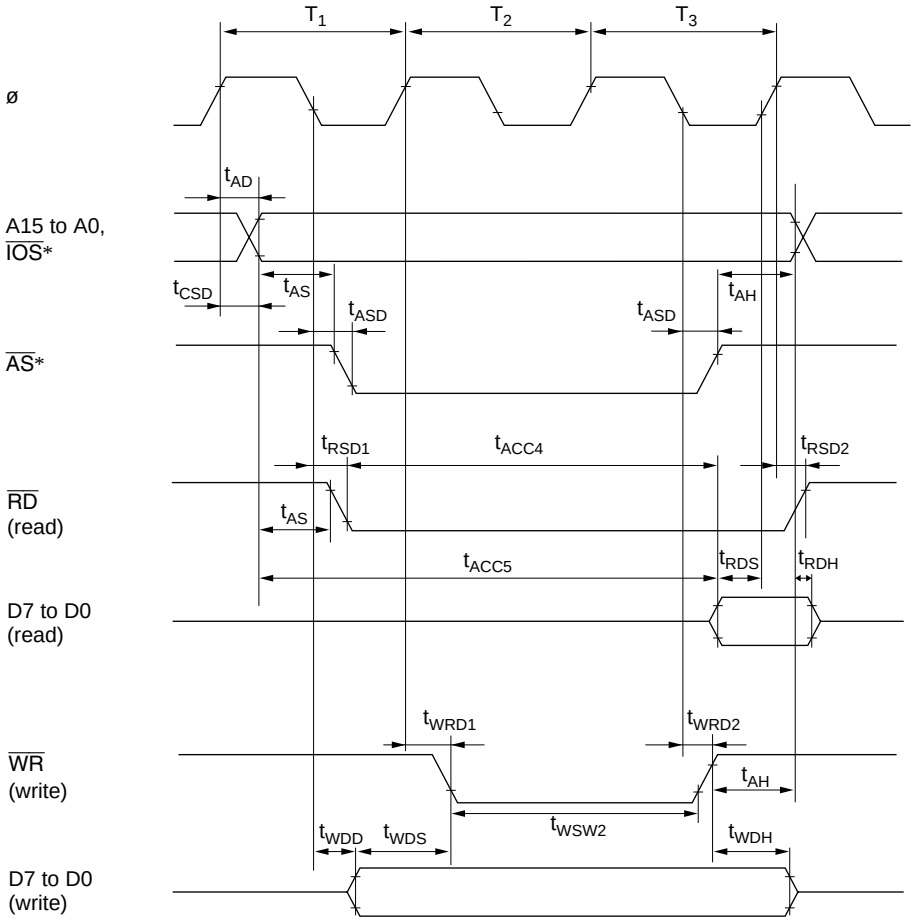
| Item | Symbol | Condition A 20 MHz Min | Condition A 20 MHz Max | Condition B 16 MHz Min | Condition B 16 MHz Max | Condition C 10 MHz Min | Condition C 10 MHz Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Read data access time 3 | $t_{ACC3}$ | — | $2.0 \times t_{cyc} - 30$ | — | $2.0 \times t_{cyc} - 40$ | — | $2.0 \times t_{cyc} - 60$ | ns | Figure 22.9 to figure 22.13 |
| Read data access time 4 | $t_{ACC4}$ | — | $2.5 \times t_{cyc} - 25$ | — | $2.5 \times t_{cyc} - 35$ | — | $2.5 \times t_{cyc} - 50$ | ns | |
| Read data access time 5 | $t_{ACC5}$ | — | $3.0 \times t_{cyc} - 30$ | — | $3.0 \times t_{cyc} - 40$ | — | $3.0 \times t_{cyc} - 60$ | ns | |
| $\overline{WR}$ delay time 1 | $t_{WRD1}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{WR}$ delay time 2 | $t_{WRD2}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{WR}$ pulse width 1 | $t_{WSW1}$ | $1.0 \times t_{cyc} - 20$ | — | $1.0 \times t_{cyc} - 30$ | — | $1.0 \times t_{cyc} - 40$ | — | ns | |
| $\overline{WR}$ pulse width 2 | $t_{WSW2}$ | $1.5 \times t_{cyc} - 20$ | — | $1.5 \times t_{cyc} - 30$ | — | $1.5 \times t_{cyc} - 40$ | — | ns | |
| Write data delay time | $t_{WDD}$ | — | 30 | — | 45 | — | 60 | ns | |
| Write data setup time | $t_{WDS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Write data hold time | $t_{WDH}$ | 10 | — | 15 | — | 20 | — | ns | |
| $\overline{WAIT}$ setup time | $t_{WTS}$ | 30 | — | 45 | — | 60 | — | ns | |
| $\overline{WAIT}$ hold time | $t_{WTH}$ | 5 | — | 5 | — | 10 | — | ns | |

Note: * For the low-voltage F-ZTAT version, $V_{CC}$ = 3.0 V to 5.5 V.



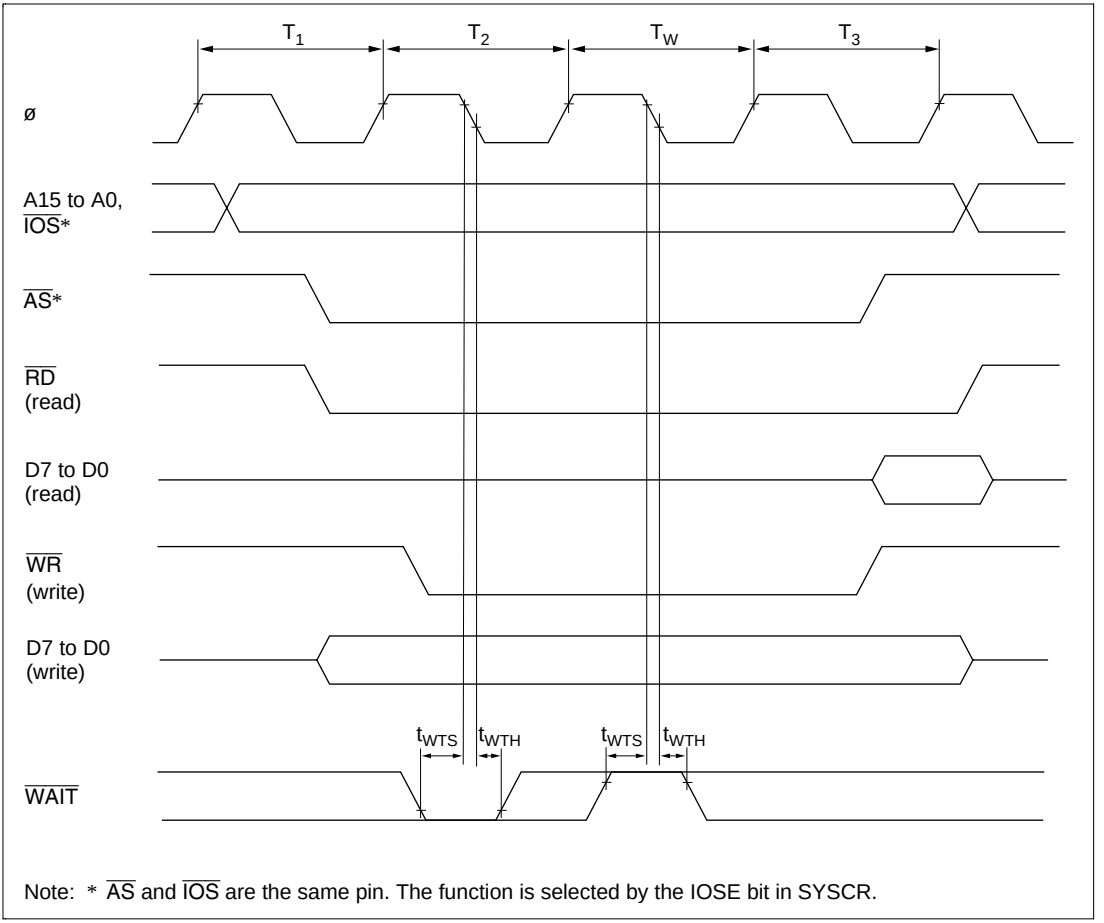

Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.9 Basic Bus Timing (Two-State Access)**




Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.10 Basic Bus Timing (Three-State Access)**




Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.11 Basic Bus Timing (Three-State Access with One Wait State)**

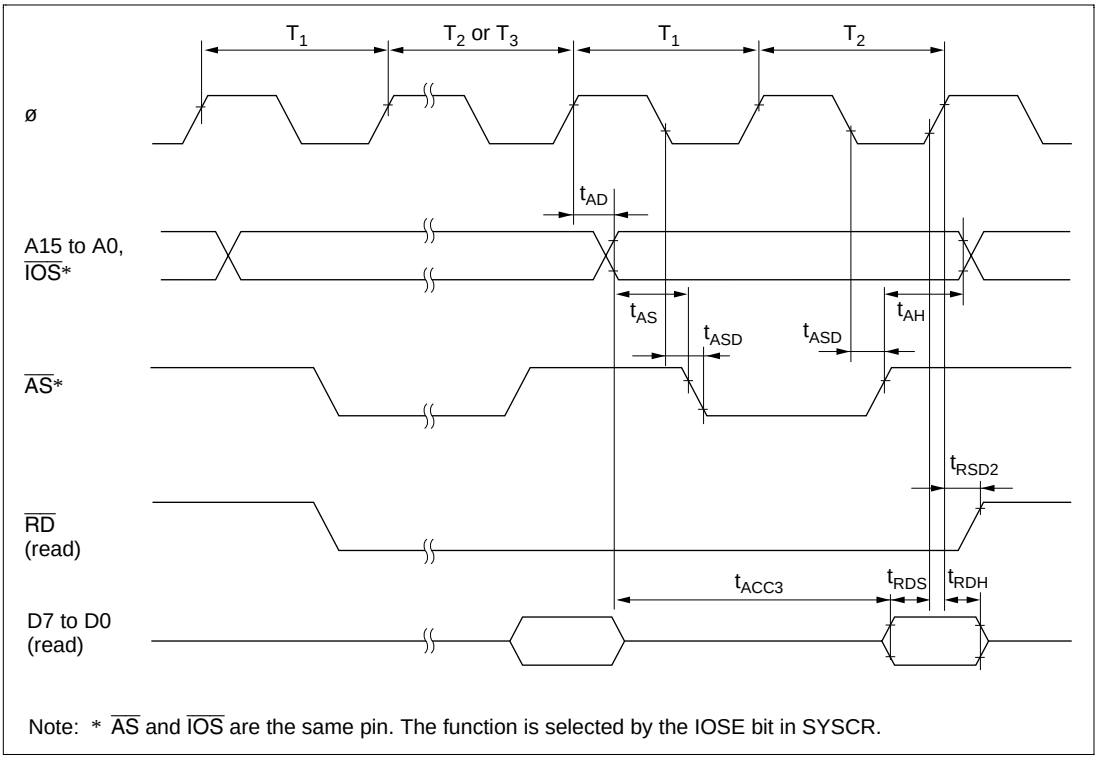
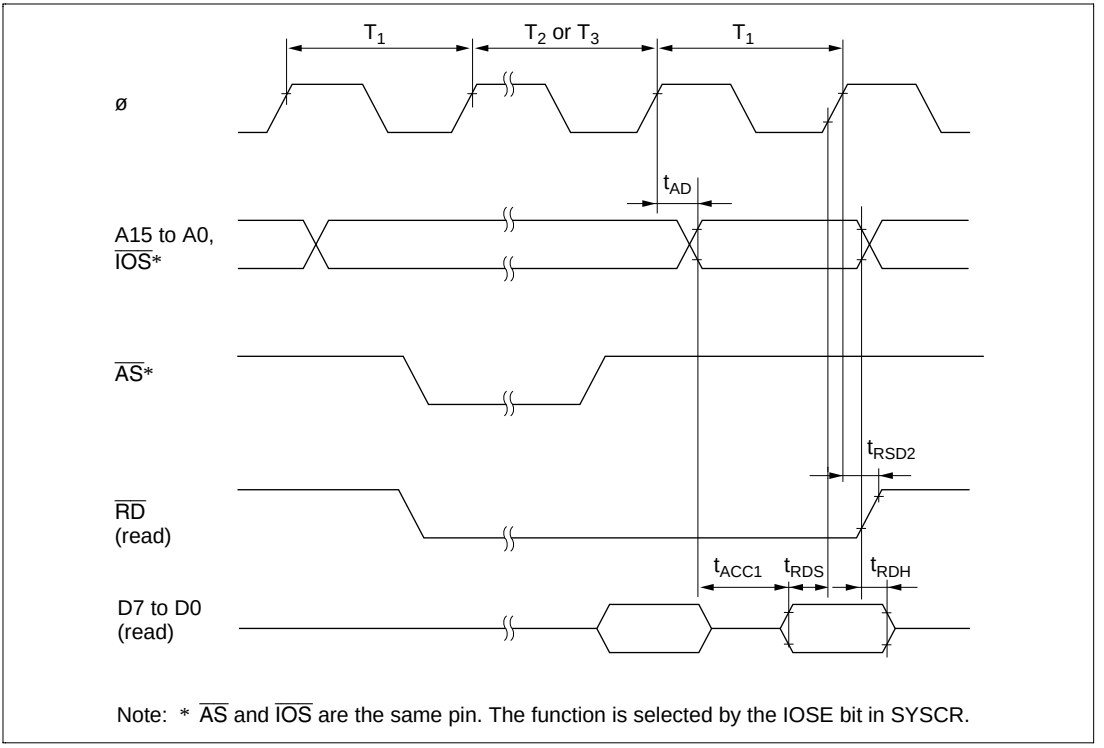



**Figure 22.12 Burst ROM Access Timing (Two-State Access)**




Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.13 Burst ROM Access Timing (One-State Access)**

### (4) Timing of On-Chip Supporting Modules

Tables 22.9 and 22.10 show the on-chip supporting module timing. The only on-chip supporting modules that can operate in subclock operation (ø = 32.768 kHz) are the I/O ports, external interrupts (NMI and IRQ0, 1, and IRQ2), the watchdog timer, and the 8-bit timer (channels 0 and 1).

**Table 22.9 Timing of On-Chip Supporting Modules**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 32.768 kHz*[1], 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 32.768 kHz*[1], 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V*[2], $V_{SS}$ = 0 V, ø = 32.768 kHz*[1], 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C

| | | | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 20 MHz | | 16 MHz | | 10 MHz | | | |
| Item | | | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test Conditions |
| I/O ports | Output data delay time | | $t_{PWD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.14 |
| | Input data setup time | | $t_{PRS}$ | 30 | — | 30 | — | 50 | — | | |
| | Input data hold time | | $t_{PRH}$ | 30 | — | 30 | — | 50 | — | | |
| FRT | Timer output delay time | | $t_{FTOD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.15 |
| | Timer input setup time | | $t_{FTIS}$ | 30 | — | 30 | — | 50 | — | | |
| | Timer clock input setup time | | $t_{FTCS}$ | 30 | — | 30 | — | 50 | — | | Figure 22.16 |
| | Timer clock pulse width | Single edge | $t_{FTCWH}$ | 1.5 | — | 1.5 | — | 1.5 | — | $t_{cyc}$ | |
| | | Both edges | $t_{FTCWL}$ | 2.5 | — | 2.5 | — | 2.5 | — | | |

| Item | | | Symbol | Condition A 20 MHz Min | Condition A 20 MHz Max | Condition B 16 MHz Min | Condition B 16 MHz Max | Condition C 10 MHz Min | Condition C 10 MHz Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMR | Timer output delay time | | $t_{TMOD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.17 |
| | Timer reset input setup time | | $t_{TMRS}$ | 30 | — | 30 | — | 50 | — | | Figure 22.19 |
| | Timer clock input setup time | | $t_{TMCS}$ | 30 | — | 30 | — | 50 | — | | Figure 22.18 |
| | Timer clock pulse width | Single edge | $t_{TMCWH}$ | 1.5 | — | 1.5 | — | 1.5 | — | $t_{cyc}$ | |
| | | Both edges | $t_{TMCWL}$ | 2.5 | — | 2.5 | — | 2.5 | — | | |
| PWM, PWMX | Pulse output delay time | | $t_{PWOD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.20 |
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | 4 | — | 4 | — | $t_{cyc}$ | Figure 22.21 |
| | | Synchronous | | 6 | — | 6 | — | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 1.5 | — | 1.5 | — | 1.5 | $t_{cyc}$ | |
| | Input clock fall time | | $t_{SCKf}$ | — | 1.5 | — | 1.5 | — | 1.5 | | |
| | Transmit data delay time (synchronous) | | $t_{TXD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.22 |
| | Receive data setup time (synchronous) | | $t_{RXS}$ | 50 | — | 50 | — | 100 | — | ns | |
| | Receive data hold time (synchronous) | | $t_{RXH}$ | 50 | — | 50 | — | 100 | — | ns | |
| A/D converter | Trigger input setup time | | $t_{TRGS}$ | 30 | — | 30 | — | 50 | — | ns | Figure 22.23 |

Notes: 1. Only supporting modules that can be used in subclock operation

2. For the low-voltage F-ZTAT version, $V_{CC}$ = 3.0 V to 5.5 V

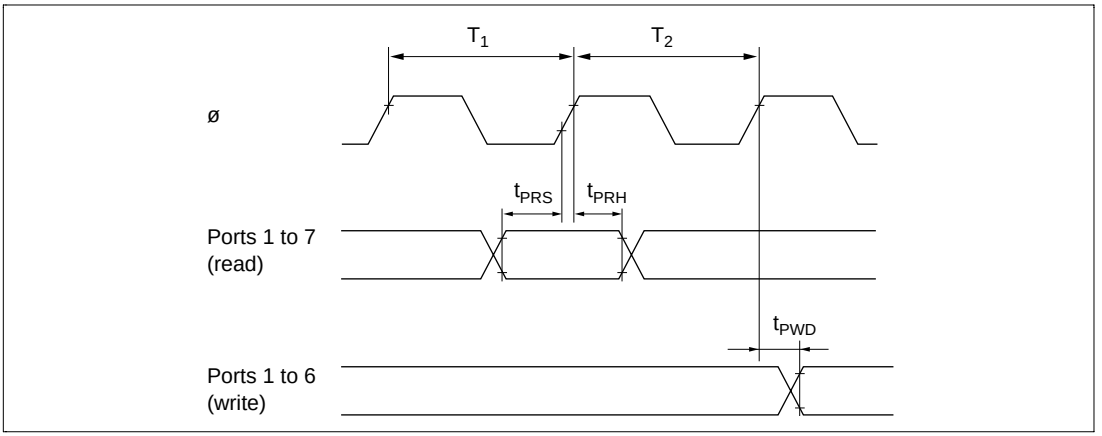



**Figure 22.14 I/O Port Input/Output Timing**

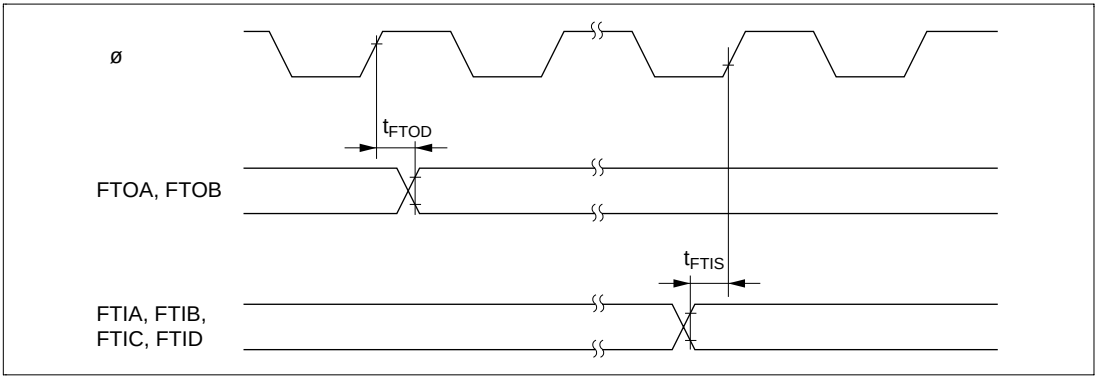



**Figure 22.15 FRT Input/Output Timing**

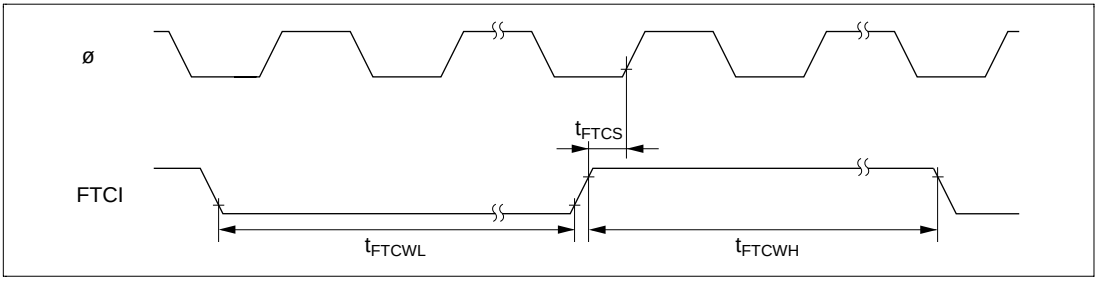



**Figure 22.16 FRT Clock Input Timing**

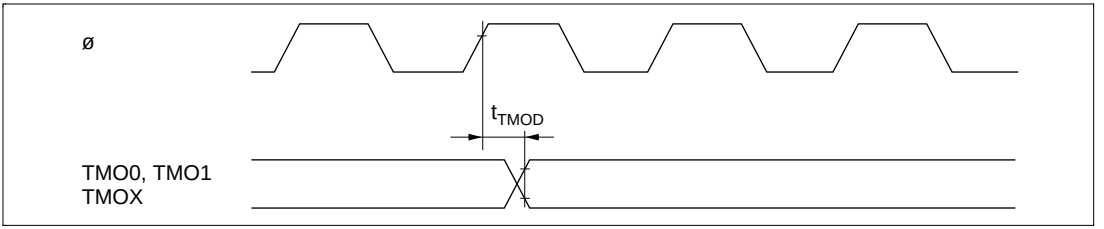



**Figure 22.17 8-Bit Timer Output Timing**

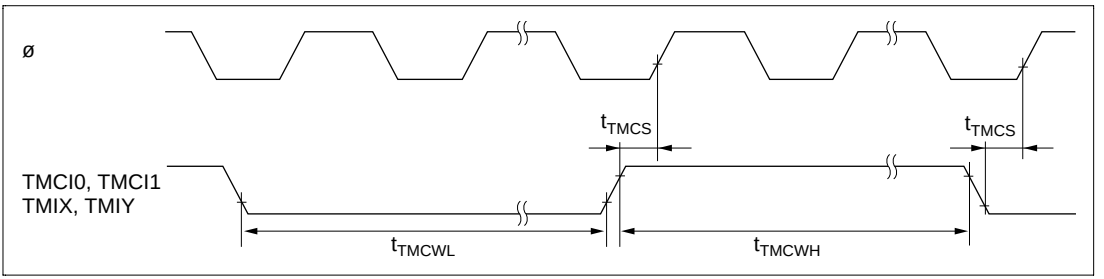



**Figure 22.18 8-Bit Timer Clock Input Timing**

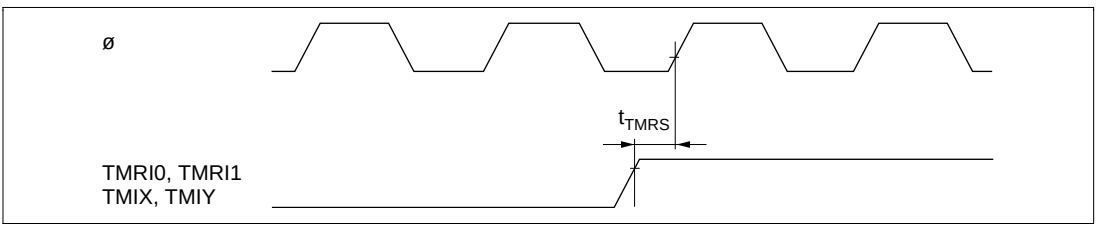



**Figure 22.19 8-Bit Timer Reset Input Timing**

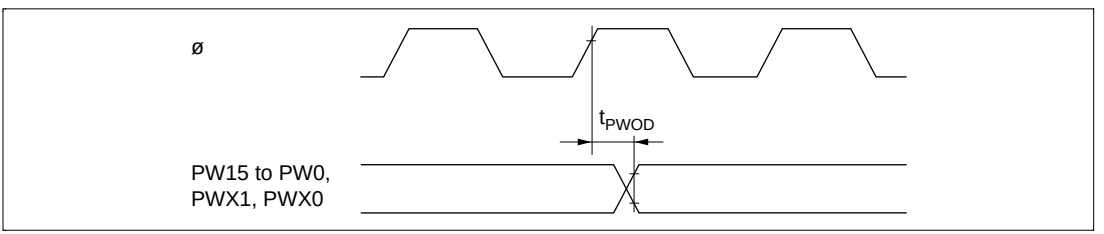



**Figure 22.20 PWM, PWMX Output Timing**

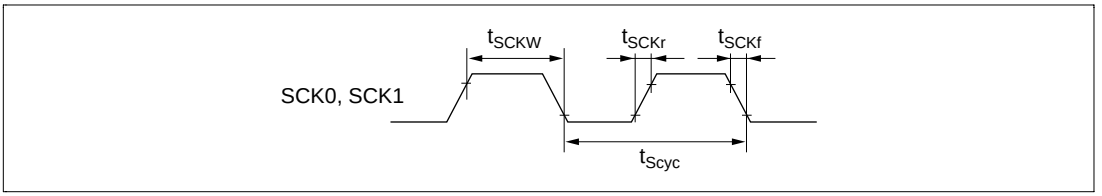



**Figure 22.21 SCK Clock Input Timing**

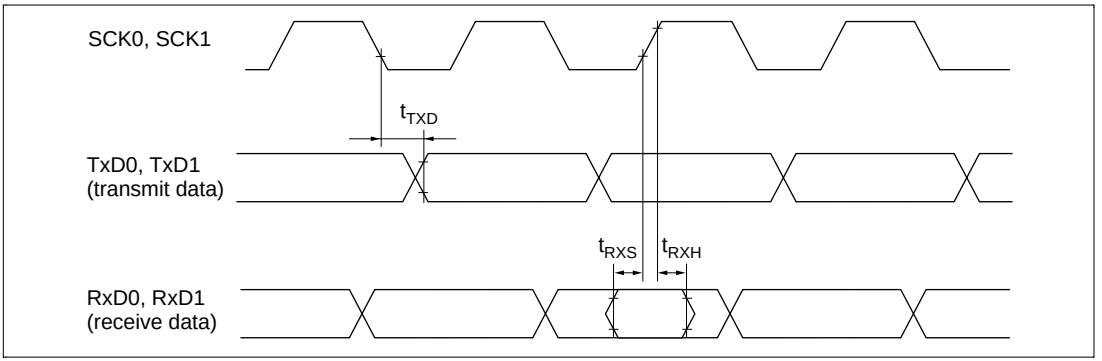



**Figure 22.22 SCI Input/Output Timing (Synchronous Mode)**

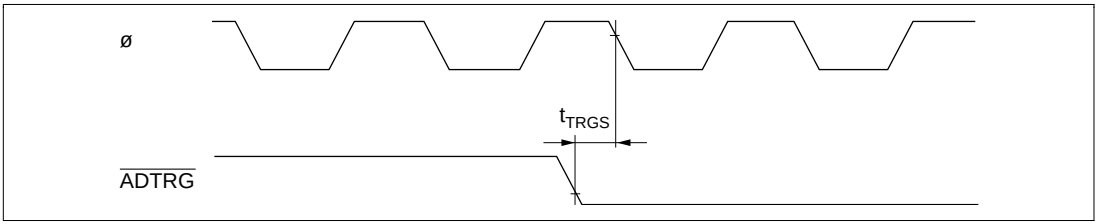


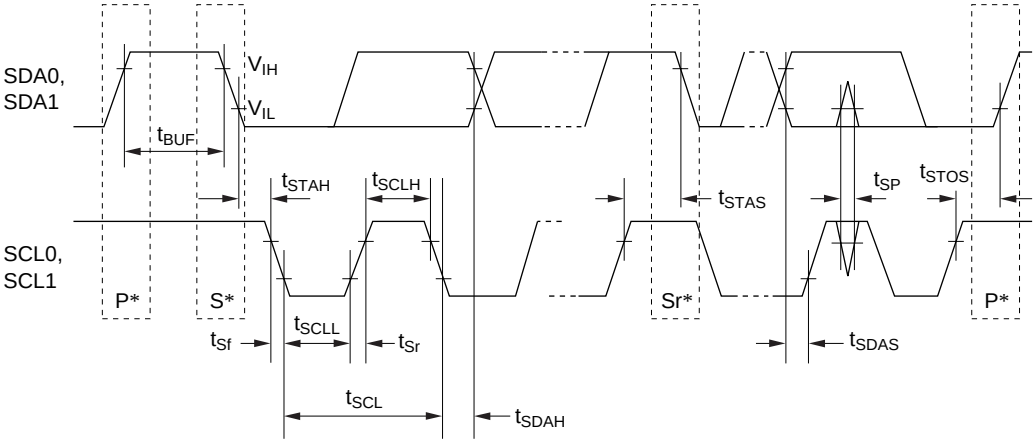

**Figure 22.23 A/D Converter External Trigger Input Timing**

**Table 22.10 $I^2C$ Bus Timing**

Conditions: $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V, ø = 5 MHz to maximum operating frequency, $T_a$ = –20 to +75°C

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| SCL clock cycle time | $t_{SCL}$ | 12 | — | — | $t_{cyc}$ | | Figure 22.24 |
| SCL clock high pulse width | $t_{SCLH}$ | 3 | — | — | $t_{cyc}$ | | |
| SCL clock low pulse width | $t_{SCLL}$ | 5 | — | — | $t_{cyc}$ | | |
| SCL, SDA input rise time | $t_{Sr}$ | — | — | 7.5* | $t_{cyc}$ | | |
| SCL, SDA input fall time | $t_{Sf}$ | — | — | 300 | ns | | |
| SCL, SDA input spike pulse elimination time | $t_{SP}$ | — | — | 1 | $t_{cyc}$ | | |
| SDA input bus free time | $t_{BUF}$ | 5 | — | — | $t_{cyc}$ | | |
| Start condition input hold time | $t_{STAH}$ | 3 | — | — | $t_{cyc}$ | | |
| Retransmission start condition input setup time | $t_{STAS}$ | 3 | — | — | $t_{cyc}$ | | |
| Stop condition input setup time | $t_{STOS}$ | 3 | — | — | $t_{cyc}$ | | |
| Data input setup time | $t_{SDAS}$ | 0.5 | — | — | $t_{cyc}$ | | |
| Data input hold time | $t_{SDAH}$ | 0 | — | — | ns | | |
| SCL, SDA capacitive load | $C_b$ | — | — | 400 | pF | | |

Note: * $17.5t_{cyc}$ can be set according to the clock selected for use by the $I^2C$ module. For details, see section 16.4, Usage Notes.




Note: * S, P, and Sr indicate the following conditions.

S: Start condition
P: Stop condition
Sr: Retransmission start condition

**Figure 22.24 I²C Bus Interface Input/Output Timing (Option)**

### 22.2.4 A/D Conversion Characteristics

Tables 22.11 and 22.12 list the A/D conversion characteristics.

**Table 22.11 A/D Conversion Characteristics (AN7 to AN0 Input: 134/266-State Conversion)**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $AV_{CC}$ = 5.0 V ± 10%
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$ = 4.0 V to 5.5 V
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V*5, $AV_{CC}$ = 2.7 V to 5.5 V*5
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

| | Condition A | | | Condition B | | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 20 MHz | | | 16 MHz | | | 10 MHz | | | |
| **Item** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Resolution | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | Bits |
| Conversion time*6 | — | — | 6.7 | — | — | 8.4 | — | — | 13.4 | µs |
| Analog input capacitance | — | — | 20 | — | — | 20 | — | — | 20 | pF |
| Permissible signal-source impedance | — | — | 10*3 | — | — | 10*3 | — | — | 10*1 | kΩ |
| | | | 5*4 | | | 5*4 | | | 5*2 | |
| Nonlinearity error | — | — | ±3.0 | — | — | ±3.0 | — | — | ±7.0 | LSB |
| Offset error | — | — | ±3.5 | — | — | ±3.5 | — | — | ±7.5 | LSB |
| Full-scale error | — | — | ±3.5 | — | — | ±3.5 | — | — | ±7.5 | LSB |
| Quantization error | — | — | ±0.5 | — | — | ±0.5 | — | — | ±0.5 | LSB |
| Absolute accuracy | — | — | ±4.0 | — | — | ±4.0 | — | — | ±8.0 | LSB |

Notes: *1 When 4.0 V ≤ $AV_{CC}$ ≤ 5.5 V
*2 When 2.7 V ≤ $AV_{CC}$ < 4.0 V
*3 When conversion time ≥ 11. 17 µs (CKS = 1 and ø ≤ 12 MHz, or CKS = 0)
*4 When conversion time < 11. 17 µs (CKS = 1 and ø > 12 MHz)
*5 For the low-voltage F-ZTAT version, $V_{CC}$ = 3.0 V to 5.5 V and $AV_{CC}$ = 3.0 V to 5.5 V.
*6 At the maximum operating frequency in single mode

**Table 22.12 A/D Conversion Characteristics**
**(CIN7 to CIN0 Input: 134/266-State Conversion)**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $AV_{CC}$ = 5.0 V ± 10%
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$ = 4.0 V to 5.5 V
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V*5, $AV_{CC}$ = 2.7 V to 5.5 V*5
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

| | Condition A | | | Condition B | | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 20 MHz | | | 16 MHz | | | 10 MHz | | | |
| **Item** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Resolution | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | Bits |
| Conversion time*6 | — | — | 6.7 | — | — | 8.4 | — | — | 13.4 | µs |
| Analog input capacitance | — | — | 20 | — | — | 20 | — | — | 20 | pF |
| Permissible signal-source impedance | — | — | 10*3 | — | — | 10*3 | — | — | 10*1 | kΩ |
| | | | 5*4 | | | 5*4 | | | 5*2 | |
| Nonlinearity error | — | — | ±5.0 | — | — | ±5.0 | — | — | ±11.0 | LSB |
| Offset error | — | — | ±5.5 | — | — | ±5.5 | — | — | ±11.5 | LSB |
| Full-scale error | — | — | ±5.5 | — | — | ±5.5 | — | — | ±11.5 | LSB |
| Quantization error | — | — | ±0.5 | — | — | ±0.5 | — | — | ±0.5 | LSB |
| Absolute accuracy | — | — | ±6.0 | — | — | ±6.0 | — | — | ±12.0 | LSB |

Notes: *1 When 4.0 V ≤ $AV_{CC}$ ≤ 5.5 V
*2 When 2.7 V ≤ $AV_{CC}$ < 4.0 V
*3 When conversion time ≥ 11. 17 µs (CKS = 1 and ø ≤ 12 MHz, or CKS = 0)
*4 When conversion time < 11. 17 µs (CKS = 1 and ø > 12 MHz)
*5 For the low-voltage F-ZTAT version, $V_{CC}$ = 3.0 V to 5.5 V and $AV_{CC}$ = 3.0 V to 5.5 V.
*6 At the maximum operating frequency in single mode

### 22.2.5 Flash Memory Characteristics

Table 22.13 shows the flash memory characteristics.

**Table 22.13 Flash Memory Characteristics**

Conditions (5 V version): $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, $T_a$ = 0 to +75°C (regular specifications), $T_a$ = 0 to +85°C (wide-range specifications)

Conditions for low-voltage version: $V_{CC}$ = 3.0 V to 3.6 V, $V_{SS}$ = 0 V, $T_a$ = 0 to +75°C (Programming/erasing operating temperature)

| Item | | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| Programming time*1 *2 *4 | | tP | — | 10 | 200 | ms/ 32 bytes | |
| Erase time*1 *3 *5 | | tE | — | 100 | 1200 | ms/ block | |
| Reprogramming count | | $N_{WEC}$ | — | — | 100 | Times | |
| Programming | Wait time after SWE-bit setting*1 | x | 10 | — | — | µs | |
| | Wait time after PSU-bit setting*1 | y | 50 | — | — | µs | |
| | Wait time after P-bit setting*1 *4 | z | 150 | — | 200 | µs | |
| | Wait time after P-bit clear*1 | α | 10 | — | — | µs | |
| | Wait time after PSU-bit clear*1 | β | 10 | — | — | µs | |
| | Wait time after PV-bit setting*1 | γ | 4 | — | — | µs | |
| | Wait time after dummy write*1 | ε | 2 | — | — | µs | |
| | Wait time after PV-bit clear*1 | η | 4 | — | — | µs | |
| | Maximum programming count*1 *4 *5 | N | — | — | 1000 | Times | z = 200 µs |

| Item | | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| Erase | Wait time after SWE-bit setting*1 | x | 10 | — | — | µs | |
| | Wait time after ESU-bit setting*1 | y | 200 | — | — | µs | |
| | Wait time after E-bit setting*1 *6 | z | 5 | — | 10 | ms | |
| | Wait time after E-bit clear*1 | α | 10 | — | — | µs | |
| | Wait time after ESU-bit clear*1 | β | 10 | — | — | µs | |
| | Wait time after EV-bit setting*1 | γ | 20 | — | — | µs | |
| | Wait time after dummy write*1 | ε | 2 | — | — | µs | |
| | Wait time after EV-bit clear*1 | η | 5 | — | — | µs | |
| | Maximum erase count*1 *6 *7 | N | — | — | 120 | Times | z = 10 ms |

Notes: *1 Set the times according to the program/erase algorithms.

*2 Programming time per 32 bytes (Shows the total period for which the P-bit in the flash memory control register (FLMCR1) is set. It does not include the programming verification time.)

*3 Block erase time (Shows the total period for which the E-bit in FLMCR1 is set. It does not include the erase verification time.)

*4 Maximum programming time (tP (max) = wait time after P-bit setting (z) × maximum programming count (N))

*5 Number of times when the wait time after P-bit setting (z) = 200 µs.

The number of writes should be set according to the actual set value of z to allow programming within the maximum programming time (tP).

*6 Maximum erase time (tE (max) = Wait time after E-bit setting (z) × maximum erase count (N))

*7 Number of times when the wait time after E-bit setting (z) = 10 ms.

The number of erases should be set according to the actual set value of z to allow erasing within the maximum erase time (tE).

### 22.2.6 Usage Note

The F-ZTAT and mask ROM versions have been confirmed as fully meeting the reference values for electrical characteristics shown in this manual. However, actual performance figures, operating margins, noise margins, and other properties may vary due to differences in the manufacturing process, on-chip ROM, layout patterns, etc.

When system evaluation testing is carried out using the F-ZTAT version, the same evaluation tests should also be conducted for the mask ROM version when changing over to that version.

## 22.3 Electrical Characteristics [H8S/2128S Series]

### 22.3.1 Absolute Maximum Ratings

Table 22.14 lists the absolute maximum ratings.

**Table 22.14 Absolute Maximum Ratings**

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage*1 | $V_{CC}$ | –0.3 to +7.0 | V |
| Power supply voltage*1 (3 V version) | $V_{CC}$ | –0.3 to +4.3 | V |
| Power supply voltage*2 ($V_{CL}$ version) | $V_{CL}$ | –0.3 to +4.3 | V |
| Input voltage (except ports 6, 7) | $V_{in}$ | –0.3 to $V_{CC}$ +0.3 | V |
| Input voltage (CIN input not selected for port 6) | $V_{in}$ | –0.3 to $V_{CC}$ +0.3 | V |
| Input voltage (CIN input selected for port 6) | $V_{in}$ | –0.3 V to lower of voltages $V_{CC}$ +0.3 and $AV_{CC}$ +0.3 | V |
| Input voltage (port 7) | $V_{in}$ | –0.3 to $AV_{CC}$ +0.3 | V |
| Analog power supply voltage | $AV_{CC}$ | –0.3 to +7.0 | V |
| Analog power supply voltage (3 V version) | $AV_{CC}$ | –0.3 to +4.3 | V |
| Analog input voltage | $V_{AN}$ | –0.3 to $AV_{CC}$ +0.3 | V |
| Operating temperature | $T_{opr}$ | Regular specifications: –20 to +75 | °C |
| | | Wide-range specifications: –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C |

Cautions: 1. Permanent damage to the chip may result if absolute maximum ratings are exceeded.

2. Never apply more than 7.0 V to any of the pins of the 5 V or 4 V version or 4.3 V to any of the pins of the 3 V version.

Notes: *1 Power supply voltage for $V_{CC1}$ pin

Never exceed the maximum rating of $V_{CL}$ in the low-power version (3 V version) because both the $V_{CC1}$ and $V_{CL}$ pins are connected to the $V_{CC}$ power supply.

*2 It is an operating power supply voltage pin on the chip.

Never apply power supply voltage to the $V_{CL}$ pin in the 5 V or 4 V version.

Always connect an external capacitor between the $V_{CL}$ pin and ground for internal voltage stabilization.

### 22.3.2 DC Characteristics

Table 22.15 lists the DC characteristics. Table 22.16 lists the permissible output currents.

**Table 22.15 DC Characteristics (1)**

Conditions: $V_{CC}$ = 5.0 V ± 10%, $AV_{CC}$*1 = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$*1 = 0 V,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

| Item | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60*2*5, $\overline{IRQ2}$ to $\overline{IRQ0}$*3*8 | (1) | $V_T^-$ | 1.0 | — | — | V | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | 0.4 | — | — | V | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0 | (2) | $V_{IH}$ | $V_{CC} - 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | Port 7 | | | $V_{CC} \times 0.7$ | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| Input low voltage | $\overline{RES}$, $\overline{STBY}$, MD1, MD0 | (3) | $V_{IL}$ | –0.3 | — | 0.5 | V | |
| | NMI, EXTAL | | | –0.3 | — | 0.8 | V | |
| | Input pins except (1) and (3) above | | | –0.3 | — | $V_{CC} \times 0.2$ | V | |
| Output high voltage | All output pins (except P47, and P52*4) | | $V_{OH}$ | $V_{CC} - 0.5$ | — | — | V | $I_{OH}$ = –200 µA |
| | | | | 3.5 | — | — | V | $I_{OH}$ = –1 mA |
| | P47, P52*4 | | | 2.0 | — | — | V | $I_{OH}$ = –200 µA |
| Output low voltage | All output pins | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | Ports 1 to 3 | | | — | — | 1.0 | V | $I_{OL}$ = 10 mA |
| Input leakage current | $\overline{RES}$ | | $\lvert I_{in} \rvert$ | — | — | 10.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| | $\overline{STBY}$, NMI, MD1, MD0 | | | — | — | 1.0 | µA | |
| | Port 7 | | | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $AV_{CC}$ – 0.5 V |

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Three-state leakage current (off state) | Ports 1 to 6 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| Input pull-up MOS current | Ports 1 to 3 | $-I_P$ | 30 | — | 300 | µA | $V_{in}$ = 0 V |
| Input capacitance | $\overline{RES}$ (4) | $C_{in}$ | — | — | 80 | pF | $V_{in}$ = 0 V<br>f = 1 MHz<br>$T_a$ = 25°C |
| | NMI | | — | — | 50 | pF | |
| | P52, P47, P24, P23 | | — | — | 20 | pF | |
| | Input pins except (4) above | | — | — | 15 | pF | |
| Current dissipation*6 | Normal operation | $I_{CC}$ | — | 45 | 55 | mA | f = 20 MHz |
| | Sleep mode | | — | 30 | 41 | mA | f = 20 MHz |
| | Standby mode*7 | | — | 1.0 | 5.0 | µA | $T_a \leq 50°C$ |
| | | | — | — | 20.0 | µA | 50°C < $T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 1.5 | 3.0 | mA | |
| | Idle | | — | 0.01 | 5.0 | µA | $AV_{CC}$ = 2.0 V to 5.5 V |
| Analog power supply voltage*1 | | $AV_{CC}$ | 4.5 | — | 5.5 | V | Operating |
| | | | 2.0 | — | 5.5 | V | Idle/not used |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: *1 Do not leave the $AV_{CC}$, and $AV_{SS}$ pins open even if the A/D converter is not used.
Even if the A/D converter is not used, apply a value in the range 2.0 V to 5.5 V to $AV_{CC}$ by connection to the power supply ($V_{CC}$), or some other method.

*2 P67 to P60 include supporting module inputs multiplexed on those pins.

*3 $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

*4 In the H8S/2128S Series, P52/SCK0/SCL0 and P47/SDA0 are NMOS push-pull outputs.
An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).
In the H8S/2128S Series, P52/SCK0 and P47 (ICE = 0) high levels are driven by NMOS.

*5 The upper limit of the port 6 applied voltage is $V_{CC}$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}$ + 0.3 V and $AV_{CC}$ + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

*6 Current dissipation values are for $V_{IH}$ min = $V_{CC}$ – 0.2 V and $V_{IL}$ max = 0.2 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

*7 The values are for $V_{RAM} \leq V_{CC} < 4.5$ V, $V_{IH}$ min = $V_{CC}$ – 0.2 V, and $V_{IL}$ max = 0.2 V.

*8 The $V_T^+$ to $V_T^-$ specification does not apply to $\overline{IRQ2}$ ($\overline{ADTRG}$) to $\overline{IRQ0}$.

**Table 22.15 DC Characteristics (2)**

Conditions: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$*1 = 4.0 V to 5.5 V, $V_{SS}$ = $AV_{SS}$*1 = 0 V,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

| Item | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60*2*5, $\overline{IRQ2}$ to $\overline{IRQ0}$*3*8 | (1) | $V_T^-$ | 1.0 | — | — | V | $V_{CC}$ = 4.5 V to 5.5 V |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | 0.4 | — | — | V | |
| | | | $V_T^-$ | 0.8 | — | — | V | $V_{CC}$ < 4.5 V |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | 0.3 | — | — | V | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0 | (2) | $V_{IH}$ | $V_{CC}$ – 0.7 | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | Port 7 | | | $V_{CC} \times 0.7$ | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| Input low voltage | $\overline{RES}$, $\overline{STBY}$, MD1, MD0 | (3) | $V_{IL}$ | –0.3 | — | 0.5 | V | |
| | NMI, EXTAL | | | –0.3 | — | 0.8 | V | |
| | Input pins except (1) and (3) above | | | –0.3 | — | $V_{CC} \times 0.2$ | V | |
| Output high voltage | All output pins (except P47, and P52*4) | | $V_{OH}$ | $V_{CC}$ – 0.5 | — | — | V | $I_{OH}$ = –200 µA |
| | | | | 3.5 | — | — | V | $I_{OH}$ = –1 mA, $V_{CC}$= 4.5 V to 5.5 V |
| | | | | 3.0 | — | — | V | $I_{OH}$ = –1 mA, $V_{CC}$ < 4.5 V |
| | P47, P52*4 | | | 1.5 | — | — | V | $I_{OH}$ = –200 µA |
| Output low voltage | All output pins | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | Ports 1 to 3 | | | — | — | 1.0 | V | $I_{OL}$ = 10 mA |

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Input leakage current | $\overline{RES}$ | $\lvert I_{in} \rvert$ | — | — | 10.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| | $\overline{STBY}$, NMI, MD1, MD0 | | — | — | 1.0 | µA | |
| | Port 7 | | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $AV_{CC}$ – 0.5 V |
| Three-state leakage current (off state) | Ports 1 to 6 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| Input pull-up MOS current | Ports 1 to 3 | $-I_P$ | 30 | — | 300 | µA | $V_{in}$ = 0 V, $V_{CC}$ = 4.5 V to 5.5 V |
| | | | 20 | — | 200 | µA | $V_{in}$ = 0 V, $V_{CC}$ < 4.5 V |
| Input capacitance | $\overline{RES}$ (4) | $C_{in}$ | — | — | 80 | pF | $V_{in}$ = 0 V, f = 1 MHz, $T_a$ = 25°C |
| | NMI | | — | — | 50 | pF | |
| | P52, P47, P24, P23 | | — | — | 20 | pF | |
| | Input pins except (4) above | | — | — | 15 | pF | |
| Current dissipation*6 | Normal operation | $I_{CC}$ | — | 35 | 44 | mA | f = 16 MHz |
| | Sleep mode | | — | 25 | 34 | mA | f = 16 MHz |
| | Standby mode*7 | | — | 1.0 | 5.0 | µA | $T_a \leq$ 50°C |
| | | | — | — | 20.0 | µA | 50°C < $T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 1.5 | 3.0 | mA | |
| | Idle | | — | 0.01 | 5.0 | µA | $AV_{CC}$ = 2.0 V to 5.5 V |
| Analog power supply voltage*1 | | $AV_{CC}$ | 4.0 | — | 5.5 | V | Operating |
| | | | 2.0 | — | 5.5 | V | Idle/not used |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: *1 Do not leave the $AV_{CC}$, and $AV_{SS}$ pins open even if the A/D converter is not used. Even if the A/D converter is not used, apply a value in the range 2.0 V to 5.5 V to $AV_{CC}$ by connection to the power supply ($V_{CC}$), or some other method.

*2 P67 to P60 include supporting module inputs multiplexed on those pins.

*3 $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

*4 In the H8S/2128S Series, P52/SCK0/SCL0 and P47/SDA0 are NMOS push-pull outputs.

An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).

In the H8S/2128S Series, P52/SCK0 and P47 (ICE = 0) high levels are driven by NMOS.

*5 The upper limit of the port 6 applied voltage is $V_{CC}$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}$ + 0.3 V and $AV_{CC}$ + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

*6 Current dissipation values are for $V_{IH}$ min = $V_{CC}$ – 0.2 V and $V_{IL}$ max = 0.2 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

*7 The values are for $V_{RAM} \leq V_{CC} < 4.0$ V, $V_{IH}$ min = $V_{CC}$ – 0.2 V, and $V_{IL}$ max = 0.2 V.

*8 The $V_T^+$ to $V_T^-$ specification does not apply to $\overline{IRQ2}$ ($\overline{ADTRG}$) to $\overline{IRQ0}$.

**Table 22.15 DC Characteristics (3)**

Conditions (Mask ROM version): $V_{CC}$ = 2.7 V to 3.6 V, $AV_{CC}$*1 = 2.7 V to 3.6 V,
$V_{SS}$ = $AV_{SS}$*1 = 0 V, $T_a$ = –20 to +75°C

| Item | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60*2*5, $\overline{IRQ2}$ to $\overline{IRQ0}$*3*8 | (1) | $V_T^-$ | $V_{CC} \times 0.2$ | — | — | V | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | $V_{CC} \times 0.05$ | — | — | V | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0 | (2) | $V_{IH}$ | $V_{CC} \times 0.9$ | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | Port 7 | | | $V_{CC} \times 0.7$ | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| Input low voltage | $\overline{RES}$, $\overline{STBY}$, MD1, MD0 | (3) | $V_{IL}$ | –0.3 | — | $V_{CC} \times 0.1$ | V | |
| | NMI, EXTAL, input pins except (1) and (3) above | | | –0.3 | — | $V_{CC} \times 0.2$ | V | |
| Output high voltage | All output pins (except P47, and P52*4) | | $V_{OH}$ | $V_{CC}$ – 0.5 | — | — | V | $I_{OH}$ = –200 µA |
| | | | | $V_{CC}$ – 1.0 | — | — | V | $I_{OH}$ = –1 mA |
| | P47, P52*4 | | | 0.5 | — | — | V | $I_{OH}$ = –200 µA |
| Output low voltage | All output pins | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | Ports 1 to 3 | | | — | — | 1.0 | V | $I_{OL}$ = 5 mA |
| Input leakage current | $\overline{RES}$ | | $\lvert I_{in} \rvert$ | — | — | 10.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| | $\overline{STBY}$, NMI, MD1, MD0 | | | — | — | 1.0 | µA | |
| | Port 7 | | | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $AV_{CC}$ – 0.5 V |

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Three-state leakage current (off state) | Ports 1 to 6 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| Input pull-up MOS current | Ports 1 to 3 | $-I_P$ | 5 | — | 150 | µA | $V_{in}$ = 0 V, $V_{CC}$ = 2.7 V to 3.6 V |
| Input capacitance | $\overline{RES}$ (4) | $C_{in}$ | — | — | 80 | pF | $V_{in}$ = 0 V, f = 1 MHz, Ta = 25°C |
| | NMI | | — | — | 50 | pF | |
| | P52, P47, P24, P23 | | — | — | 20 | pF | |
| | Input pins except (4) above | | — | — | 15 | pF | |
| Current dissipation*6 | Normal operation | $I_{CC}$ | — | 24 | 30 | mA | f = 10 MHz |
| | Sleep mode | | — | 15 | 23 | mA | f = 10 MHz |
| | Standby mode*7 | | — | 1.0 | 5.0 | µA | $T_a \leq 50°C$ |
| | | | — | — | 20.0 | µA | $50°C < T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 1.5 | 3.0 | mA | |
| | Idle | | — | 0.01 | 5.0 | µA | $AV_{CC}$ = 2.0 V to 3.6 V |
| Analog power supply voltage*1 | | $AV_{CC}$ | 2.7 | — | 3.6 | V | Operating |
| | | | 2.0 | — | 3.6 | V | Idle/not used |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: *1 Do not leave the $AV_{CC}$, and $AV_{SS}$ pins open even if the A/D converter is not used.
Even if the A/D converter is not used, apply a value in the range 2.0 V to 3.6 V to $AV_{CC}$ by connection to the power supply ($V_{CC}$), or some other method.

*2 P67 to P60 include supporting module inputs multiplexed on those pins.

*3 $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

*4 In the H8S/2128S Series, P52/SCK0/SCL0 and P47/SDA0 are NMOS push-pull outputs.
An external pull-up resistor is necessary to provide high-level output from SCL0 and SDA0 (ICE = 1).
In the H8S/2128S Series, P52/SCK0 and P47 (ICE = 0) high levels are driven by NMOS.

*5 The upper limit of the port 6 applied voltage is $V_{CC}$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}$ + 0.3 V and $AV_{CC}$ + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

*6 Current dissipation values are for $V_{IH}$ min = $V_{CC}$ – 0.2 V and $V_{IL}$ max = 0.2 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

*7 The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, $V_{IH}$ min = $V_{CC}$ – 0.2 V, and $V_{IL}$ max = 0.2 V.

*8 The $V_T^+$ to $V_T^-$ specification does not apply to $\overline{IRQ2}$ ($\overline{ADTRG}$) to $\overline{IRQ0}$.

**Table 22.16 Permissible Output Currents**

Conditions: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, Ta = –20 to +75°C (regular specifications),
Ta = –40 to +85°C (wide-range specifications)

| Item | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Permissible output low current (per pin) | SCL1, SCL0, SDA1, SDA0 | $I_{OL}$ | — | — | 20 | mA |
| | Ports 1, 2, 3 | | — | — | 10 | mA |
| | Other output pins | | — | — | 2 | mA |
| Permissible output low current (total) | Total of ports 1, 2, and 3 | $\Sigma I_{OL}$ | — | — | 80 | mA |
| | Total of all output pins, including the above | | — | — | 120 | mA |
| Permissible output high current (per pin) | All output pins | $-I_{OH}$ | — | — | 2 | mA |
| Permissible output high current (total) | Total of all output pins | $\Sigma -I_{OH}$ | — | — | 40 | mA |

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22.16.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 22.25 and 22.26.

**Table 22.16 Permissible Output Currents (cont)**

Conditions: $V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0 V, Ta = –20 to +75°C

| Item | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Permissible output low current (per pin) | SCL1, SCL0, SDA1, SDA0 | $I_{OL}$ | — | — | 10 | mA |
| | Ports 1, 2, 3 | | — | — | 2 | mA |
| | Other output pins | | — | — | 1 | mA |
| Permissible output low current (total) | Total of ports 1, 2, and 3 | $\Sigma I_{OL}$ | — | — | 40 | mA |
| | Total of all output pins, including the above | | — | — | 60 | mA |
| Permissible output high current (per pin) | All output pins | $-I_{OH}$ | — | — | 2 | mA |
| Permissible output high current (total) | Total of all output pins | $\Sigma -I_{OH}$ | — | — | 30 | mA |

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22.16.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 22.25 and 22.26.

**Table 22.17 Bus Drive Characteristics**

Conditions: $V_{CC}$ = 4.0 V to 5.5 V, $V_{CC}$ = 2.7 to 3.6 V (3 V version), $V_{SS}$ = 0 V

Applicable Pins: SCL1, SCL0, SDA1, SDA0 (bus drive function selected)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | $V_T^-$ | $V_{CC} \times 0.3$ | — | — | V | |
| | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | | |
| Input high voltage | $V_{IH}$ | $V_{CC} \times 0.7$ | — | $V_{CC}$ + 0.5 | V | |
| Input low voltage | $V_{IL}$ | –0.5 | — | $V_{CC} \times 0.3$ | | |
| Output low voltage | $V_{OL}$ | — | — | 0.8 | V | $I_{OL}$ = 16 mA, $V_{CC}$ = 4.5 V to 5.5 V |
| | | — | — | 0.5 | | $I_{OL}$ = 8 mA |
| | | — | — | 0.4 | | $I_{OL}$ = 3 mA |
| Input capacitance | $C_{in}$ | — | — | 20 | pF | $V_{in}$ = 0 V, f = 1 MHz, $T_a$ = 25°C |
| Three-state leakage current (off state) | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| SCL, SDA output fall time | $t_{Of}$ | 20 + 0.1Cb | — | 250 | ns | |

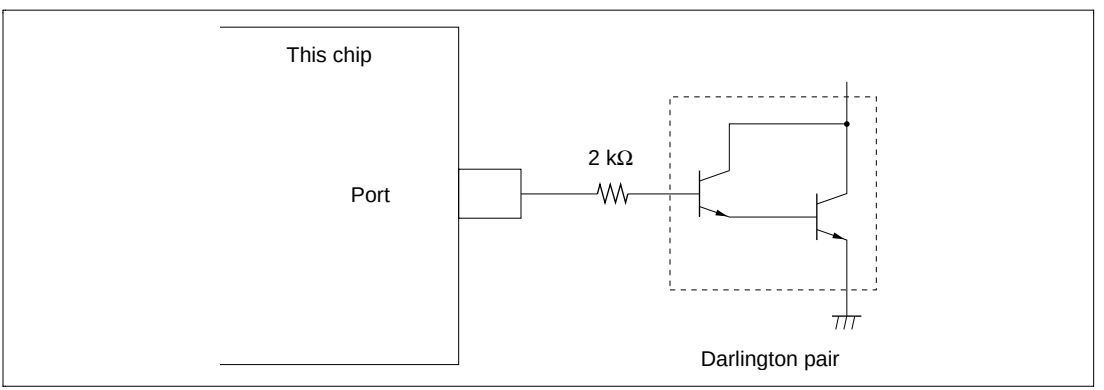



**Figure 22.25 Darlington Pair Drive Circuit (Example)**

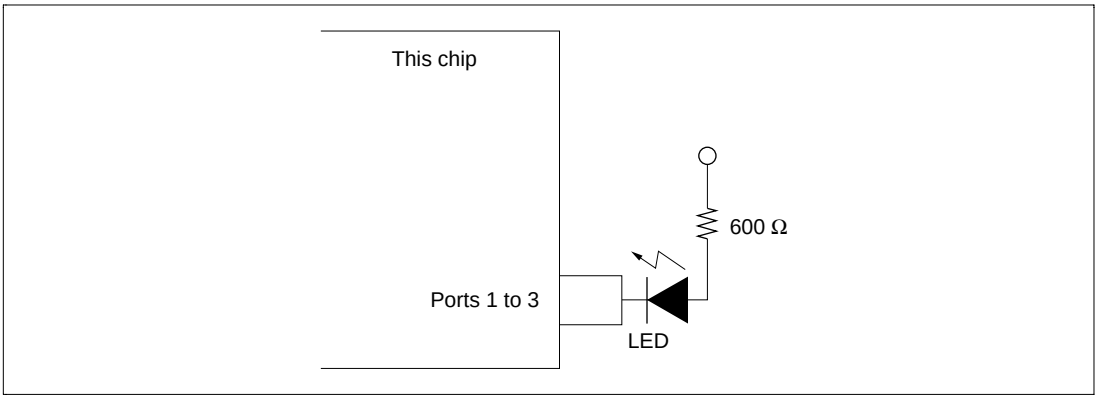



**Figure 22.26 LED Drive Circuit (Example)**

### 22.3.3 AC Characteristics

Figure 22.3 shows the test conditions for the AC characteristics.

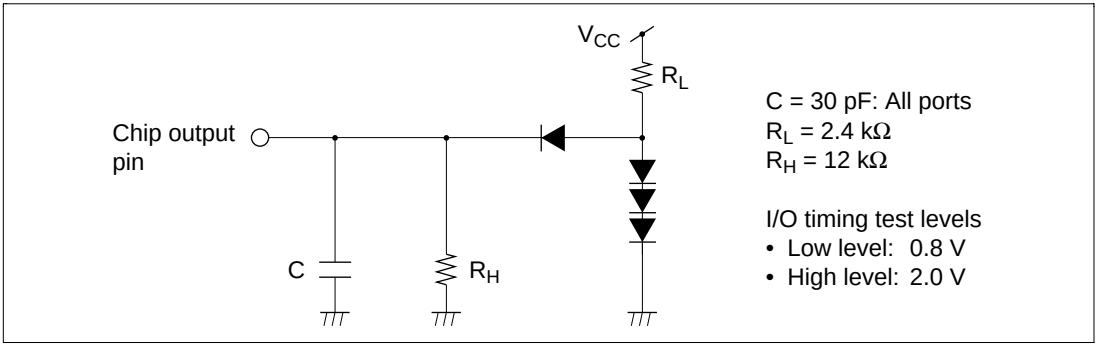



**Figure 22.27 Output Load Circuit**

### (1) Clock Timing

Table 22.18 shows the clock timing. The clock timing specified here covers clock (ø) output and clock pulse generator (crystal) and external clock input (EXTAL pin) oscillation settling times. For details of external clock input (EXTAL pin and EXCL pin) timing, see section 20, Clock Pulse Generator.

**Table 22.18 Clock Timing**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | Test |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Conditions |
| Clock cycle time | $t_{cyc}$ | 50 | 500 | 62.5 | 500 | 100 | 500 | ns | Figure 22.28 |
| Clock high pulse width | $t_{CH}$ | 17 | — | 20 | — | 30 | — | ns | Figure 22.28 |
| Clock low pulse width | $t_{CL}$ | 17 | — | 20 | — | 30 | — | ns | |
| Clock rise time | $t_{Cr}$ | — | 8 | — | 10 | — | 20 | ns | |
| Clock fall time | $t_{Cf}$ | — | 8 | — | 10 | — | 20 | ns | |
| Oscillation settling time at reset (crystal) | $t_{OSC1}$ | 10 | — | 10 | — | 20 | — | ms | Figure 22.29<br>Figure 22.30 |
| Oscillation settling time in software standby (crystal) | $t_{OSC2}$ | 8 | — | 8 | — | 8 | — | ms | |
| External clock output stabilization delay time | $t_{DEXT}$ | 500 | — | 500 | — | 500 | — | µs | |

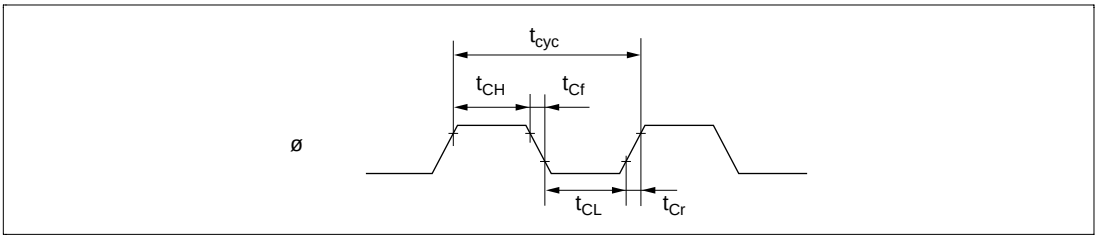



**Figure 22.28 System Clock Timing**

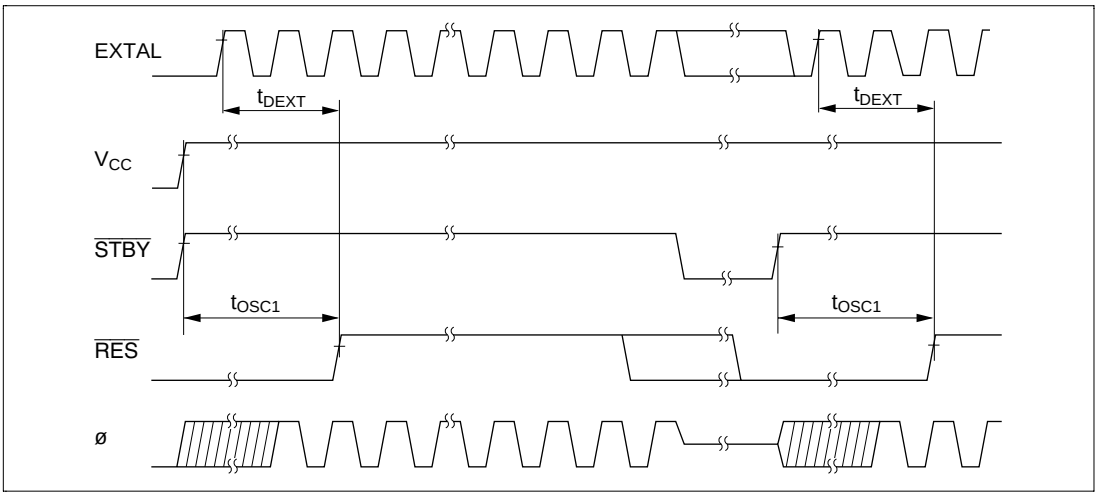



**Figure 22.29 Oscillation Settling Timing**

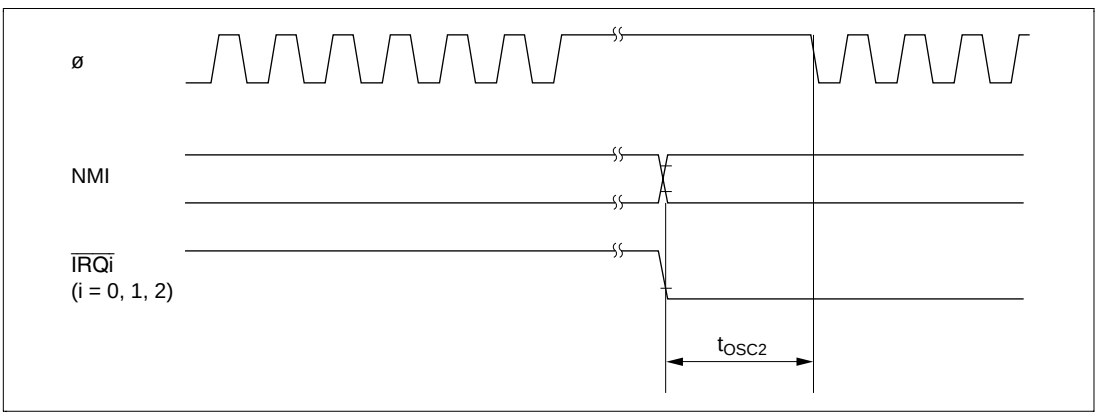



**Figure 22.30 Oscillation Setting Timing (Exiting Software Standby Mode)**

### (2) Control Signal Timing

Table 22.19 shows the control signal timing. The only external interrupts that can operate on the subclock (ø = 32.768 kHz) are NMI and IRQ0, 1, and IRQ2.

**Table 22.19 Control Signal Timing**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C

| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test Conditions |
| $\overline{RES}$ setup time | $t_{RESS}$ | 200 | — | 200 | — | 300 | — | ns | Figure 22.31 |
| $\overline{RES}$ pulse width | $t_{RESW}$ | 20 | — | 20 | — | 20 | — | $t_{cyc}$ | |
| NMI setup time (NMI) | $t_{NMIS}$ | 150 | — | 150 | — | 250 | — | ns | Figure 22.32 |
| NMI hold time (NMI) | $t_{NMIH}$ | 10 | — | 10 | — | 10 | — | ns | |
| NMI pulse width (exiting software standby mode) | $t_{NMIW}$ | 200 | — | 200 | — | 200 | — | ns | |
| IRQ setup time ($\overline{IRQ2}$ to $\overline{IRQ0}$) | $t_{IRQS}$ | 150 | — | 150 | — | 250 | — | ns | |
| IRQ hold time ($\overline{IRQ2}$ to $\overline{IRQ0}$) | $t_{IRQH}$ | 10 | — | 10 | — | 10 | — | ns | |
| IRQ pulse width ($\overline{IRQ2}$ to $\overline{IRQ0}$) (exiting software standby mode) | $t_{IRQW}$ | 200 | — | 200 | — | 200 | — | ns | |

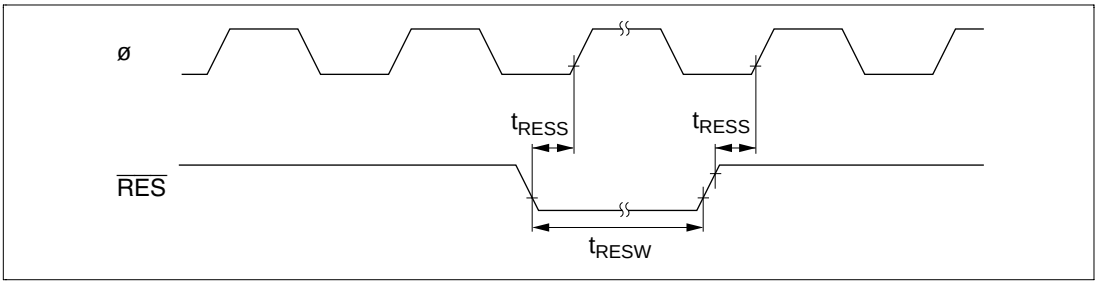



**Figure 22.31 Reset Input Timing**

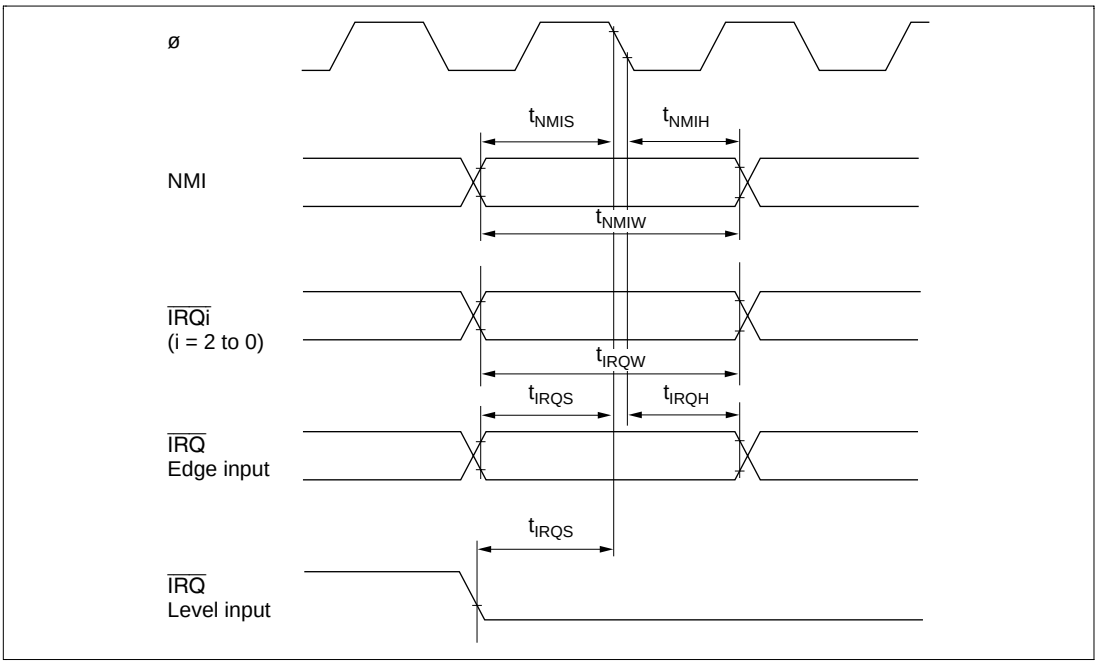



**Figure 22.32 Interrupt Input Timing**

### (3) Bus Timing

Table 22.20 shows the bus timing. Operation in external expansion mode is not guaranteed when operating on the subclock (ø = 32.768 kHz).

**Table 22.20 Bus Timing**

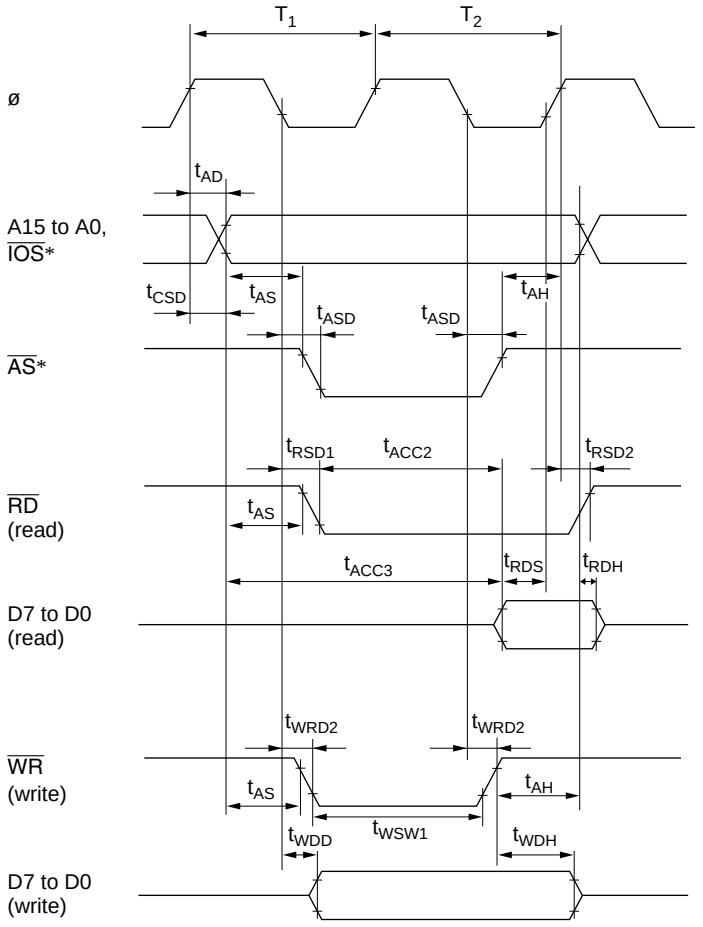
Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

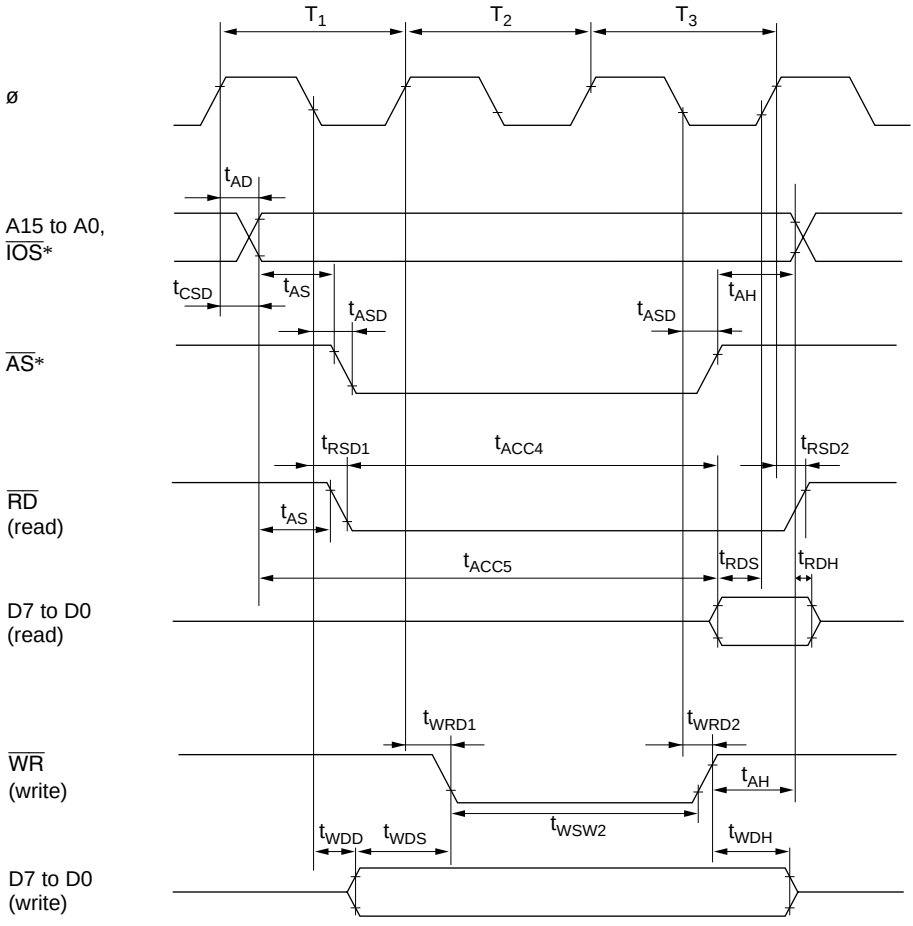
| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test Conditions |
| Address delay time | $t_{AD}$ | — | 20 | — | 30 | — | 40 | ns | Figure 22.33 to figure 22.37 |
| Address setup time | $t_{AS}$ | 0.5 × $t_{cyc}$ – 15 | — | 0.5 × $t_{cyc}$ – 20 | — | 0.5 × $t_{cyc}$ – 30 | — | ns | |
| Address hold time | $t_{AH}$ | 0.5 × $t_{cyc}$ – 10 | — | 0.5 × $t_{cyc}$ – 15 | — | 0.5 × $t_{cyc}$ – 20 | — | ns | |
| $\overline{CS}$ delay time ($\overline{IOS}$) | $t_{CSD}$ | — | 20 | — | 30 | — | 40 | ns | |
| $\overline{AS}$ delay time | $t_{ASD}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{RD}$ delay time 1 | $t_{RSD1}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{RD}$ delay time 2 | $t_{RSD2}$ | — | 30 | — | 45 | — | 60 | ns | |
| Read data setup time | $t_{RDS}$ | 15 | — | 20 | — | 35 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read data access time 1 | $t_{ACC1}$ | — | 1.0 × $t_{cyc}$ – 30 | — | 1.0 × $t_{cyc}$ – 40 | — | 1.0 × $t_{cyc}$ – 60 | ns | |
| Read data access time 2 | $t_{ACC2}$ | — | 1.5 × $t_{cyc}$ – 25 | — | 1.5 × $t_{cyc}$ – 35 | — | 1.5 × $t_{cyc}$ – 50 | ns | |

| Item | Symbol | Condition A 20 MHz Min | Condition A 20 MHz Max | Condition B 16 MHz Min | Condition B 16 MHz Max | Condition C 10 MHz Min | Condition C 10 MHz Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Read data access time 3 | $t_{ACC3}$ | — | $2.0 \times t_{cyc} - 30$ | — | $2.0 \times t_{cyc} - 40$ | — | $2.0 \times t_{cyc} - 60$ | ns | Figure 22.33 to figure 22.37 |
| Read data access time 4 | $t_{ACC4}$ | — | $2.5 \times t_{cyc} - 25$ | — | $2.5 \times t_{cyc} - 35$ | — | $2.5 \times t_{cyc} - 50$ | ns | |
| Read data access time 5 | $t_{ACC5}$ | — | $3.0 \times t_{cyc} - 30$ | — | $3.0 \times t_{cyc} - 40$ | — | $3.0 \times t_{cyc} - 60$ | ns | |
| $\overline{WR}$ delay time 1 | $t_{WRD1}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{WR}$ delay time 2 | $t_{WRD2}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{WR}$ pulse width 1 | $t_{WSW1}$ | $1.0 \times t_{cyc} - 20$ | — | $1.0 \times t_{cyc} - 30$ | — | $1.0 \times t_{cyc} - 40$ | — | ns | |
| $\overline{WR}$ pulse width 2 | $t_{WSW2}$ | $1.5 \times t_{cyc} - 20$ | — | $1.5 \times t_{cyc} - 30$ | — | $1.5 \times t_{cyc} - 40$ | — | ns | |
| Write data delay time | $t_{WDD}$ | — | 30 | — | 45 | — | 60 | ns | |
| Write data setup time | $t_{WDS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Write data hold time | $t_{WDH}$ | 10 | — | 15 | — | 20 | — | ns | |
| $\overline{WAIT}$ setup time | $t_{WTS}$ | 30 | — | 45 | — | 60 | — | ns | |
| $\overline{WAIT}$ hold time | $t_{WTH}$ | 5 | — | 5 | — | 10 | — | ns | |



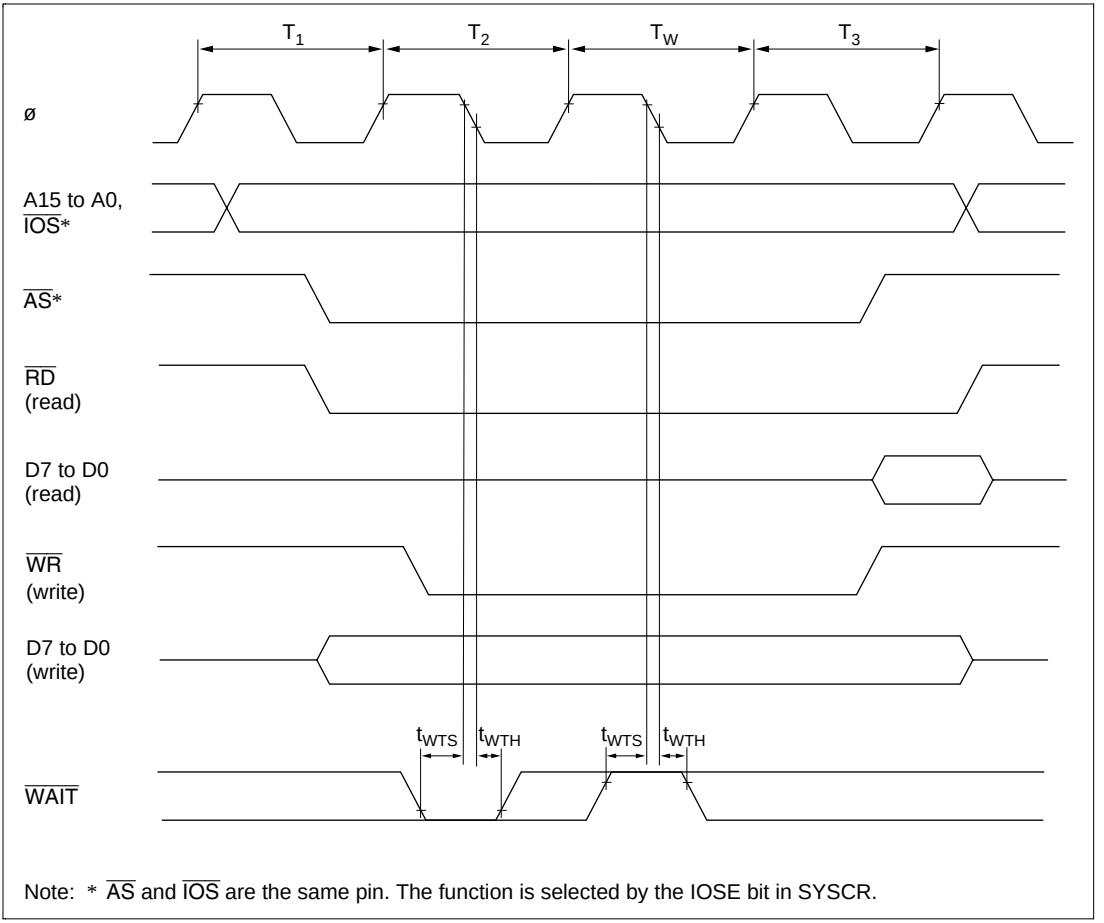

Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.33 Basic Bus Timing (Two-State Access)**




Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.34 Basic Bus Timing (Three-State Access)**




Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.35 Basic Bus Timing (Three-State Access with One Wait State)**

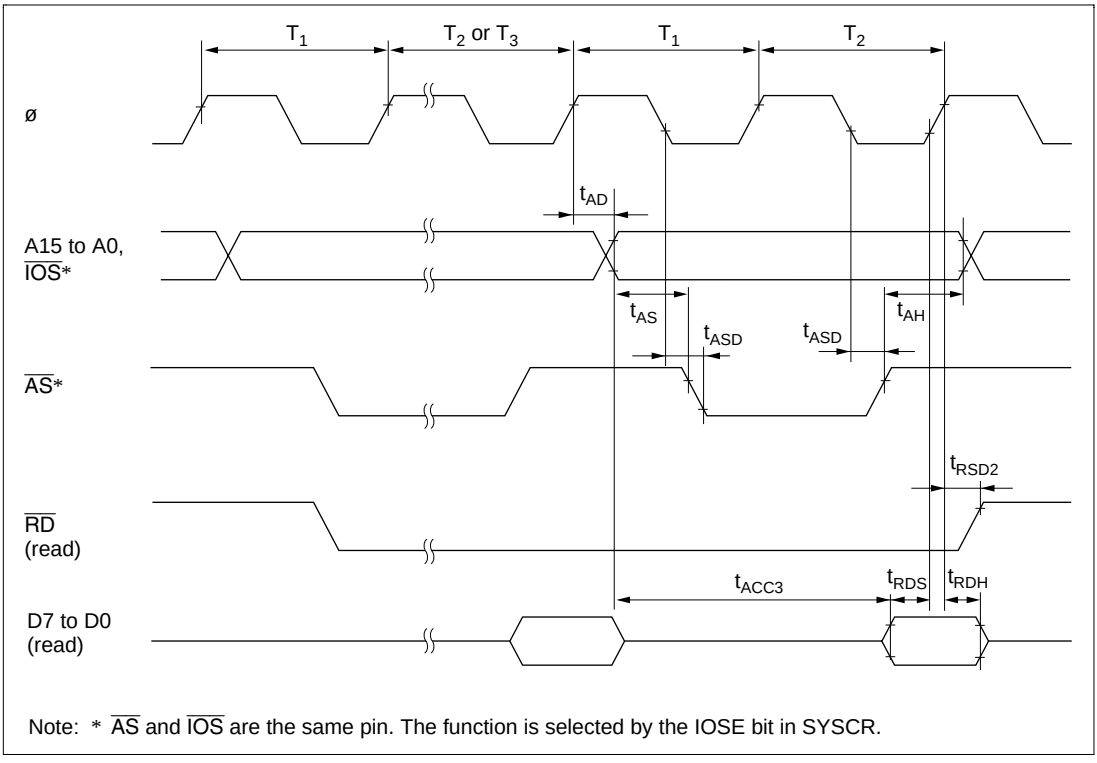
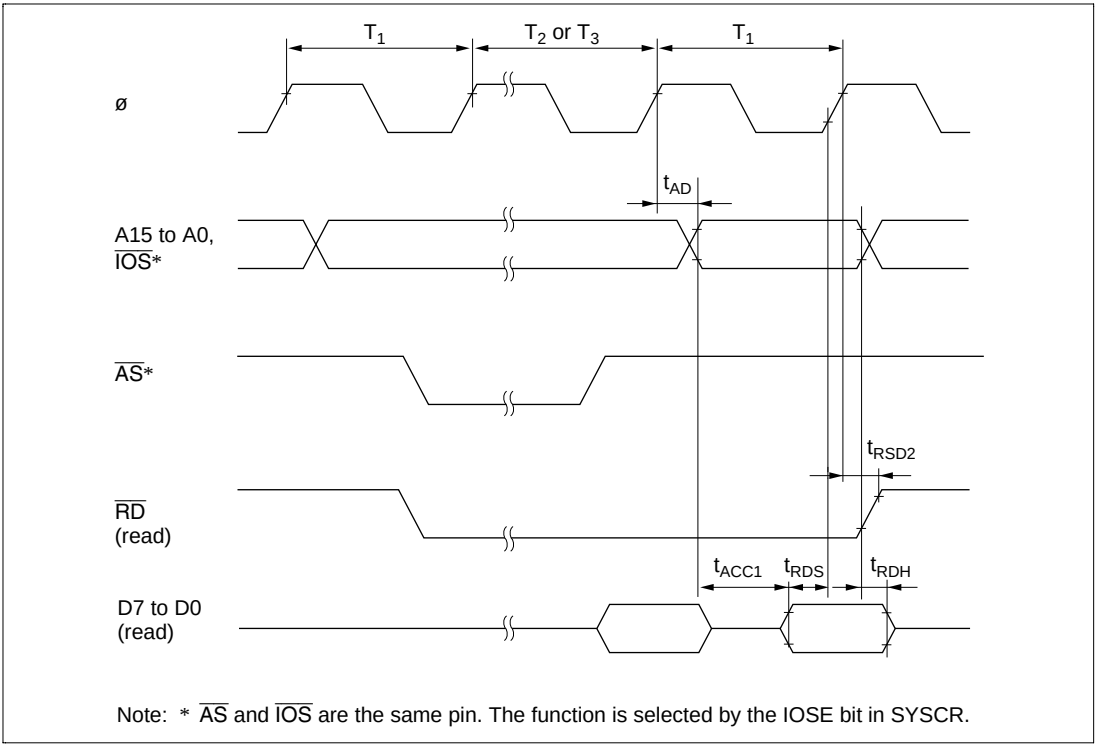



**Figure 22.36 Burst ROM Access Timing (Two-State Access)**




Note: * $\overline{AS}$ and $\overline{IOS}$ are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.37 Burst ROM Access Timing (One-State Access)**

### (4) Timing of On-Chip Supporting Modules

Tables 22.21 and 22.22 show the on-chip supporting module timing. The only on-chip supporting modules that can operate in subclock operation (ø = 32.768 kHz) are the I/O ports, external interrupts (NMI and IRQ0, 1, and IRQ2), the watchdog timer, and the 8-bit timer (channels 0 and 1).

**Table 22.21 Timing of On-Chip Supporting Modules**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 32.768 kHz*, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 32.768 kHz*, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 3.6 V, $V_{SS}$ = 0 V, ø = 32.768 kHz*, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C

| | | | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 20 MHz | | 16 MHz | | 10 MHz | | | |
| Item | | | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test Conditions |
| I/O ports | Output data delay time | | $t_{PWD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.38 |
| | Input data setup time | | $t_{PRS}$ | 30 | — | 30 | — | 50 | — | | |
| | Input data hold time | | $t_{PRH}$ | 30 | — | 30 | — | 50 | — | | |
| FRT | Timer output delay time | | $t_{FTOD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.39 |
| | Timer input setup time | | $t_{FTIS}$ | 30 | — | 30 | — | 50 | — | | |
| | Timer clock input setup time | | $t_{FTCS}$ | 30 | — | 30 | — | 50 | — | | Figure 22.40 |
| | Timer clock pulse width | Single edge | $t_{FTCWH}$ | 1.5 | — | 1.5 | — | 1.5 | — | $t_{cyc}$ | |
| | | Both edges | $t_{FTCWL}$ | 2.5 | — | 2.5 | — | 2.5 | — | | |

| Item | | | Symbol | Condition A 20 MHz Min | Condition A 20 MHz Max | Condition B 16 MHz Min | Condition B 16 MHz Max | Condition C 10 MHz Min | Condition C 10 MHz Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMR | Timer output delay time | | $t_{TMOD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.41 |
| | Timer reset input setup time | | $t_{TMRS}$ | 30 | — | 30 | — | 50 | — | | Figure 22.43 |
| | Timer clock input setup time | | $t_{TMCS}$ | 30 | — | 30 | — | 50 | — | | Figure 22.42 |
| | Timer clock pulse width | Single edge | $t_{TMCWH}$ | 1.5 | — | 1.5 | — | 1.5 | — | $t_{cyc}$ | |
| | | Both edges | $t_{TMCWL}$ | 2.5 | — | 2.5 | — | 2.5 | — | | |
| PWM, PWMX | Pulse output delay time | | $t_{PWOD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.44 |
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | 4 | — | 4 | — | $t_{cyc}$ | Figure 22.45 |
| | | Synchronous | | 6 | — | 6 | — | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 1.5 | — | 1.5 | — | 1.5 | $t_{cyc}$ | |
| | Input clock fall time | | $t_{SCKf}$ | — | 1.5 | — | 1.5 | — | 1.5 | | |
| | Transmit data delay time (synchronous) | | $t_{TXD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.46 |
| | Receive data setup time (synchronous) | | $t_{RXS}$ | 50 | — | 50 | — | 100 | — | ns | |
| | Receive data hold time (synchronous) | | $t_{RXH}$ | 50 | — | 50 | — | 100 | — | ns | |
| A/D converter | Trigger input setup time | | $t_{TRGS}$ | 30 | — | 30 | — | 50 | — | ns | Figure 22.47 |

Note: * Only supporting modules that can be used in subclock operation

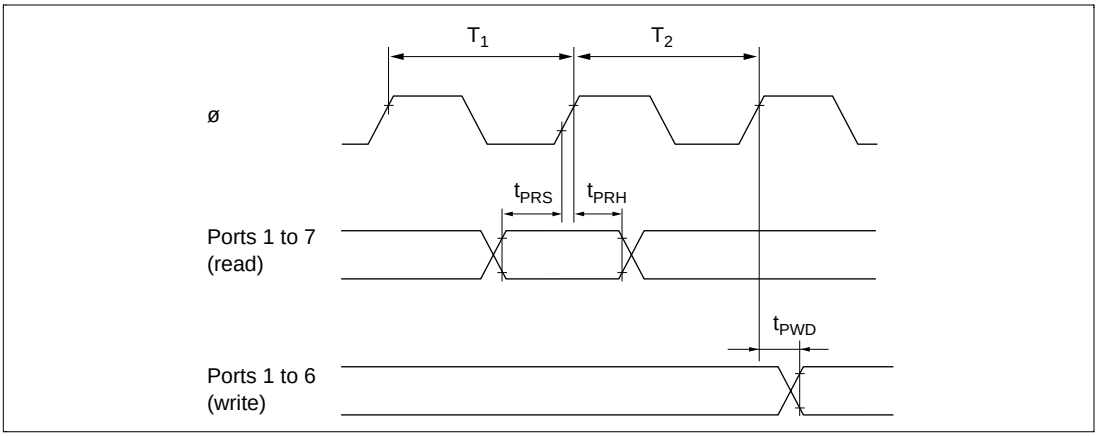



**Figure 22.38 I/O Port Input/Output Timing**

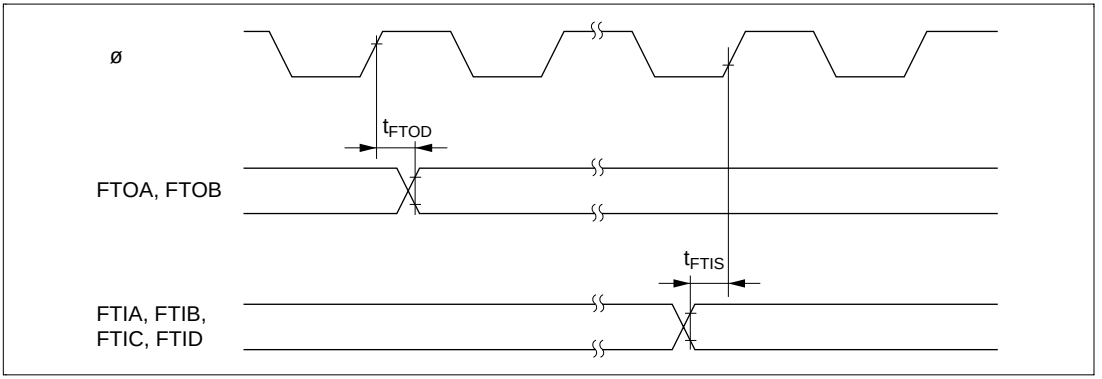



**Figure 22.39 FRT Input/Output Timing**

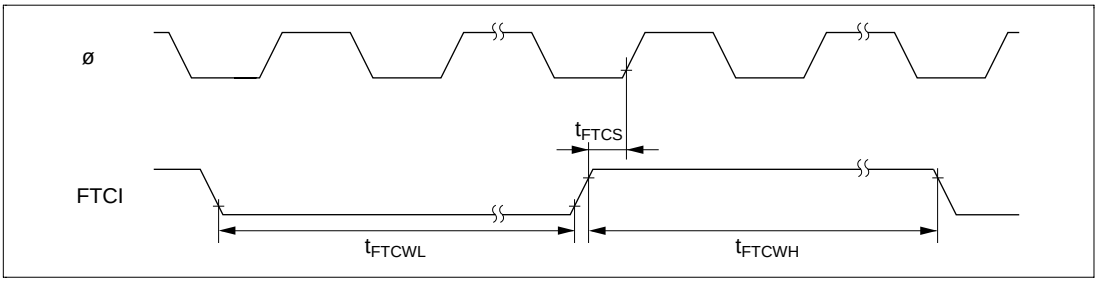



**Figure 22.40 FRT Clock Input Timing**

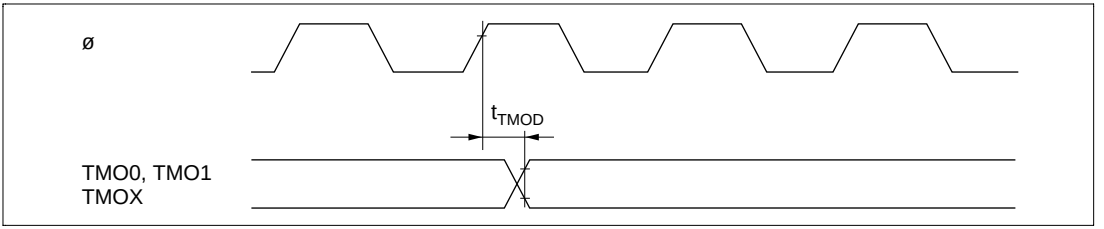



**Figure 22.41 8-Bit Timer Output Timing**

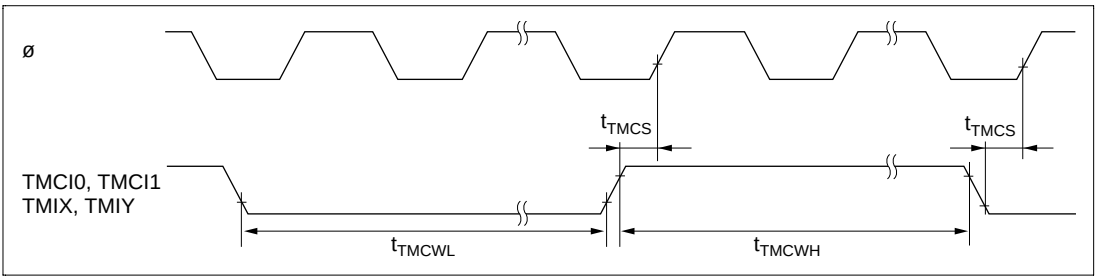



**Figure 22.42 8-Bit Timer Clock Input Timing**

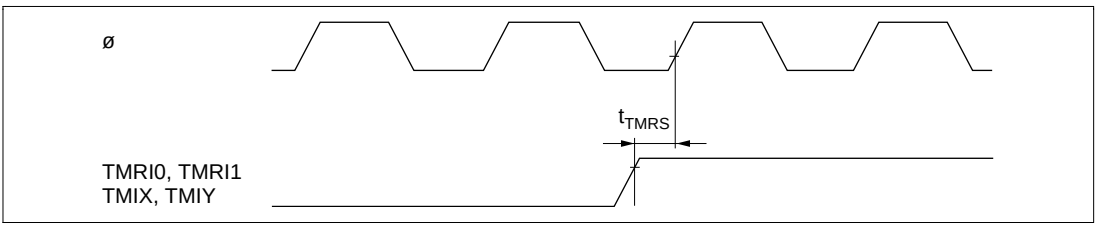



**Figure 22.43 8-Bit Timer Reset Input Timing**

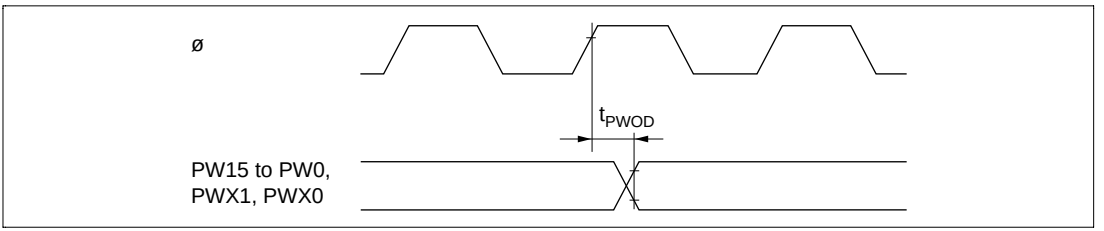



**Figure 22.44 PWM, PWMX Output Timing**

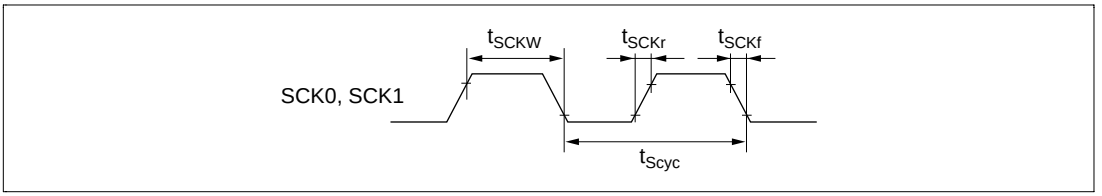



**Figure 22.45 SCK Clock Input Timing**

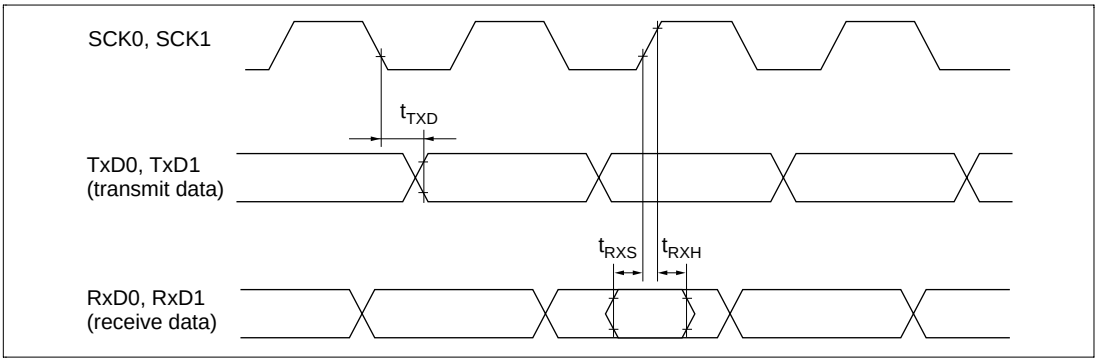



**Figure 22.46 SCI Input/Output Timing (Synchronous Mode)**

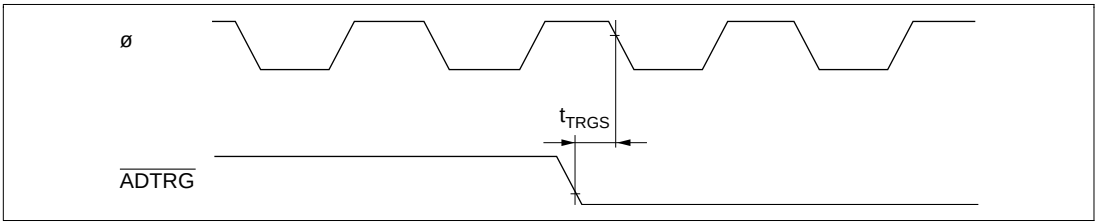


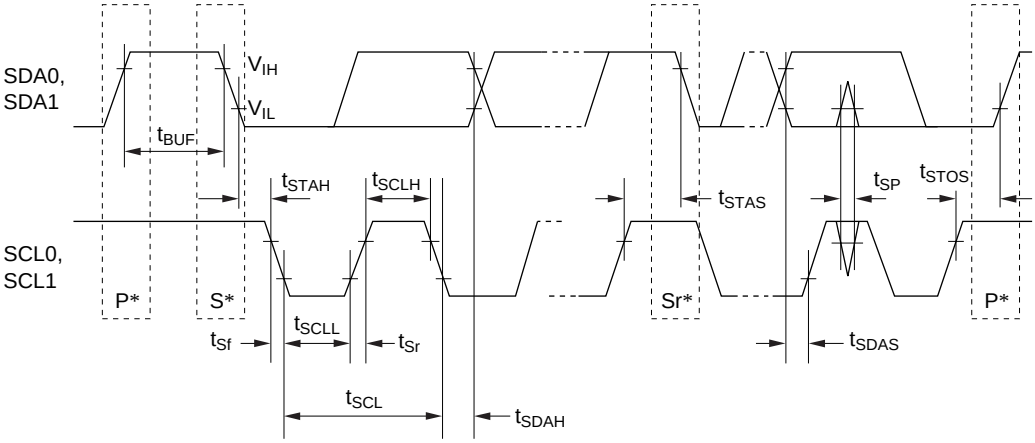

**Figure 22.47 A/D Converter External Trigger Input Timing**

**Table 22.22 $I^2C$ Bus Timing**

Conditions: $V_{CC}$ = 4.0 V to 5.5 V, $V_{CC}$ = 2.7 V to 3.6 V (3 V version), $V_{SS}$ = 0 V, ø = 5 MHz to maximum operating frequency, $T_a$ = –20 to +75°C

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|
| SCL clock cycle time | $t_{SCL}$ | 12 | — | — | $t_{cyc}$ | | Figure 22.48 |
| SCL clock high pulse width | $t_{SCLH}$ | 3 | — | — | $t_{cyc}$ | | |
| SCL clock low pulse width | $t_{SCLL}$ | 5 | — | — | $t_{cyc}$ | | |
| SCL, SDA input rise time | $t_{Sr}$ | — | — | 7.5* | $t_{cyc}$ | | |
| SCL, SDA input fall time | $t_{Sf}$ | — | — | 300 | ns | | |
| SCL, SDA input spike pulse elimination time | $t_{SP}$ | — | — | 1 | $t_{cyc}$ | | |
| SDA input bus free time | $t_{BUF}$ | 5 | — | — | $t_{cyc}$ | | |
| Start condition input hold time | $t_{STAH}$ | 3 | — | — | $t_{cyc}$ | | |
| Retransmission start condition input setup time | $t_{STAS}$ | 3 | — | — | $t_{cyc}$ | | |
| Stop condition input setup time | $t_{STOS}$ | 3 | — | — | $t_{cyc}$ | | |
| Data input setup time | $t_{SDAS}$ | 0.5 | — | — | $t_{cyc}$ | | |
| Data input hold time | $t_{SDAH}$ | 0 | — | — | ns | | |
| SCL, SDA capacitive load | $C_b$ | — | — | 400 | pF | | |

Note: * $17.5t_{cyc}$ can be set according to the clock selected for use by the $I^2C$ module. For details, see section 16.4, Usage Notes.




Note: * S, P, and Sr indicate the following conditions.

S: Start condition
P: Stop condition
Sr: Retransmission start condition

**Figure 22.48 I²C Bus Interface Input/Output Timing (Option)**

### 22.3.4 A/D Conversion Characteristics

Tables 22.23 and 22.24 list the A/D conversion characteristics.

**Table 22.23 A/D Conversion Characteristics (AN7 to AN0 Input: 134/266-State Conversion)**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $AV_{CC}$ = 5.0 V ± 10%
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$ = 4.0 V to 5.5 V
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 3.6 V, $AV_{CC}$ = 2.7 V to 3.6 V
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

| | Condition A | | | Condition B | | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 20 MHz | | | 16 MHz | | | 10 MHz | | | |
| **Item** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Resolution | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | Bits |
| Conversion time*3 | — | — | 6.7 | — | — | 8.4 | — | — | 13.4 | µs |
| Analog input capacitance | — | — | 20 | — | — | 20 | — | — | 20 | pF |
| Permissible signal-source impedance | — | — | 10*1<br>5*2 | — | — | 10*1<br>5*2 | — | — | 5 | kΩ |
| Nonlinearity error | — | — | ±3.0 | — | — | ±3.0 | — | — | ±7.0 | LSB |
| Offset error | — | — | ±3.5 | — | — | ±3.5 | — | — | ±7.5 | LSB |
| Full-scale error | — | — | ±3.5 | — | — | ±3.5 | — | — | ±7.5 | LSB |
| Quantization error | — | — | ±0.5 | — | — | ±0.5 | — | — | ±0.5 | LSB |
| Absolute accuracy | — | — | ±4.0 | — | — | ±4.0 | — | — | ±8.0 | LSB |

Notes: *1 When conversion time ≥ 11. 17 µs (CKS = 1 and ø ≤ 12 MHz, or CKS = 0)
*2 When conversion time < 11. 17 µs (CKS = 1 and ø > 12 MHz)
*3 At the maximum operating frequency in single mode

**Table 22.24 A/D Conversion Characteristics**
**(CIN7 to CIN0 Input: 134/266-State Conversion)**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $AV_{CC}$ = 5.0 V ± 10%
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$ = 4.0 V to 5.5 V
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 3.0 V to 3.6 V*4, $AV_{CC}$ = 3.0 V to 3.6 V*4
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

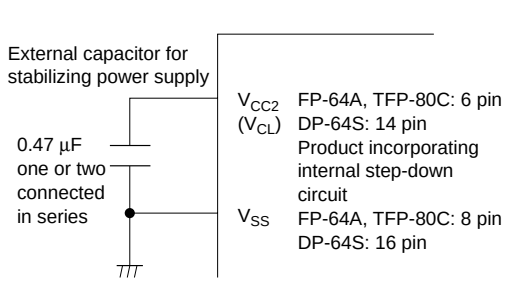
| | Condition A | | | Condition B | | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 20 MHz | | | 16 MHz | | | 10 MHz | | | |
| **Item** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Resolution | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | Bits |
| Conversion time*3 | — | — | 6.7 | — | — | 8.4 | — | — | 13.4 | µs |
| Analog input capacitance | — | — | 20 | — | — | 20 | — | — | 20 | pF |
| Permissible signal-source impedance | — | — | 10*1<br>5*2 | — | — | 10*1<br>5*2 | — | — | 5 | kΩ |
| Nonlinearity error | — | — | ±5.0 | — | — | ±5.0 | — | — | ±11.0 | LSB |
| Offset error | — | — | ±5.5 | — | — | ±5.5 | — | — | ±11.5 | LSB |
| Full-scale error | — | — | ±5.5 | — | — | ±5.5 | — | — | ±11.5 | LSB |
| Quantization error | — | — | ±0.5 | — | — | ±0.5 | — | — | ±0.5 | LSB |
| Absolute accuracy | — | — | ±6.0 | — | — | ±6.0 | — | — | ±12.0 | LSB |

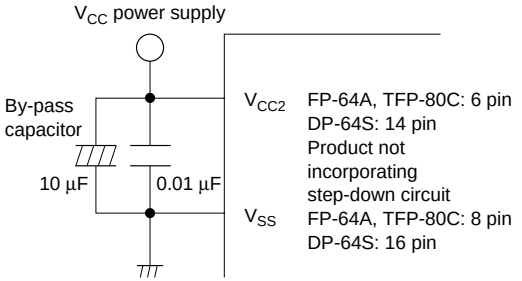
Notes: *1 When conversion time ≥ 11. 17 µs (CKS = 1 and ø ≤ 12 MHz, or CKS = 0)
*2 When conversion time < 11. 17 µs (CKS = 1 and ø > 12 MHz)
*3 At the maximum operating frequency in single mode
*4 When using CIN input, $V_{CC}$ = 3.0 V to 3.6 V and $AV_{CC}$ = 3.0 V to 3.6 V.

### 22.3.5 Usage Note

(1) The F-ZTAT and mask ROM versions have been confirmed as fully meeting the reference values for electrical characteristics shown in this manual. However, actual performance figures, operating margins, noise margins, and other properties may vary due to differences in the manufacturing process, on-chip ROM, layout patterns, etc.
When system evaluation testing is carried out using the F-ZTAT version, the same evaluation tests should also be conducted for the mask ROM version when changing over to that version.

(2) On-chip power supply step-down circuit
The H8S/2128 F-ZTAT does not incorporate an internal power supply step-down circuit. When changing over to F-ZTAT versions or mask ROM versions incorporating an internal step-down circuit, the $V_{CC2}$ pin has the same pin location as the $V_{CL}$ pin in a step-down circuit. Therfore, note that the circuit patterns differ between these two types of products.




For products incorporating an internal step-down circuit, do not connect the $V_{CL}$ pin to the $V_{CC}$ power supply. (The $V_{CC1}$ pin must be connected to the $V_{CC}$ power supply as usual.)

The power supply stabilization capacitor must be connected to the $V_{CL}$ pin. Use a monolithic ceramic capacitor of 0.47 µF(one or two connected in series) and locate it near the pins.

In case the power supply voltage is lower than 3.6 V, connect the capacitor in the same way as the case with no step-down circuit incorporated.

<Products incorporating internal step-down circuit>

HD6432128S, HD6432128SW,
HD6432127S, HD6432127SW

The location of the $V_{CC2}$ ($V_{CC}$ power supply) pin in the product not incorporating an internal step-down circuit, is the same as the $V_{CL}$ pin in a product incorporating an internal step-down circuit.

It is recommended that the by-pass capacitors are connected to the power supply terminal (these are reference values).

<Products not incorporating internal step-down circuit>

HD64F2128, HD64F2128V,
HD6432127R, HD6432127RW,
HD6432126R, HD6432126RW,
HD6432122, HD6432120,
HD6432128SV, HD6432128SVW,
HD6432127SV, HD6432127SVW

**Figure 22.49 Connection of External Capacitor (mask ROM type incorporating step-down circuit and product not incorporating step-down circuit)**

(3) Specification differences in internal I/O registers

Mask ROM version of H8S/2128S, H8S/2127S are different from the H8S/2128 Series and H8S/2124 Series in the specification of control registers for peripheral functions.

A/D converter: A/D Control Register (ADCR)

**H8S/2128 Series, H8S/2124 Series**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | TRGS1 | TRGS0 | — | — | — | — | — | — |
| Initial value | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| Read/Write | R/W | R/W | — | — | — | — | — | — |

Bits 5 to 0—Reserved bits: These bits cannot be modified and are always read as 1.

**H8S/2128S Series Mask ROM Version (internal step-down products)**

Bits 5 to 0—Reserved bits: Should always be written 1.

Power-down state: Standby Control Register (SBYCR)

**H8S/2128 Series, H8S/2124 Series**

| Bit 6 | Bit 5 | Bit 4 | | |
|---|---|---|---|---|
| **STS2** | **STS1** | **STS0** | **Description** | |
| 0 | 0 | 0 | Standby time = 8,192 states | (Initial value) |
| | | 1 | Standby time = 16,384 states | |
| | 1 | 0 | Standby time = 32,768 states | |
| | | 1 | Standby time = 65,536 states | |
| 1 | 0 | 0 | Standby time = 131,072 states | |
| | | 1 | Standby time = 262,144 states | |
| | 1 | 0 | Reserved | |
| | | 1 | Standby time = 16 states* | |

Note: * This setting must not be used in the flash memory versions.

**H8S/2128S Series Mask ROM Version (internal step-down products)**

| Bit 6 | Bit 5 | Bit 4 | | |
|---|---|---|---|---|
| **STS2** | **STS1** | **STS0** | **Description** | |
| 0 | 0 | 0 | Standby time = 8,192 states | (Initial value) |
| | | 1 | Standby time = 16,384 states | |
| | 1 | 0 | Standby time = 32,768 states | |
| | | 1 | Standby time = 65,536 states | |
| 1 | 0 | 0 | Standby time = 131,072 states | |
| | | 1 | Standby time = 262,144 states | |
| | 1 | 0 | Reserved | |
| | | 1 | Standby time = 16 states* | |

Note: * This setting must not be used in the flash memory versions and H8S/2128S Series.

## 22.4 Electrical Characteristics [H8S/2124 Series]

### 22.4.1 Absolute Maximum Ratings

Table 22.25 lists the absolute maximum ratings.

**Table 22.25 Absolute Maximum Ratings**

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | –0.3 to +7.0 | V |
| Input voltage (except ports 6, and 7) | $V_{in}$ | –0.3 to $V_{CC}$ +0.3 | V |
| Input voltage (CIN input not selected for port 6) | $V_{in}$ | –0.3 to $V_{CC}$ +0.3 | V |
| Input voltage (CIN input selected for port 6) | $V_{in}$ | Lower voltage of –0.3 to $V_{CC}$ +0.3 and $AV_{CC}$ +0.3 | V |
| Input voltage (port 7) | $V_{in}$ | –0.3 to $AV_{CC}$ + 0.3 | V |
| Analog power supply voltage | $AV_{CC}$ | –0.3 to +7.0 | V |
| Analog input voltage | $V_{AN}$ | –0.3 to $AV_{CC}$ +0.3 | V |
| Operating temperature | $T_{opr}$ | Regular specifications: –20 to +75 | °C |
| | | Wide-range specifications: –40 to +85 | °C |
| Storage temperature | $T_{stg}$ | –55 to +125 | °C |

Caution: Permanent damage to the chip may result if absolute maximum ratings are exceeded.

### 22.4.2 DC Characteristics

Table 22.26 lists the DC characteristics. Table 22.27 lists the permissible output currents.

**Table 22.26 DC Characteristics (1)**

Conditions: $V_{CC}$ = 5.0 V ± 10%, $AV_{CC}$*1 = 5.0 V ± 10%, $V_{SS}$ = $AV_{SS}$*1 = 0 V,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60*2*4, (1) $\overline{IRQ2}$ to $\overline{IRQ0}$*3 | $V_T^-$ | 1.0 | — | — | V | |
| | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | $V_T^+ - V_T^-$ | 0.4 | — | — | V | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, (2) NMI, MD1, MD0 | $V_{IH}$ | $V_{CC}$ – 0.7 | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | Port 7 | | 2.0 | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | 2.0 | — | $V_{CC}$ +0.3 | V | |
| Input low voltage | $\overline{RES}$, $\overline{STBY}$, (3) MD1, MD0 | $V_{IL}$ | –0.3 | — | 0.5 | V | |
| | NMI, EXTAL, input pins except (1) and (3) above | | –0.3 | — | 0.8 | V | |
| Output high voltage | All output pins | $V_{OH}$ | $V_{CC}$ – 0.5 | — | — | V | $I_{OH}$ = –200 µA |
| | | | 3.5 | — | — | V | $I_{OH}$ = –1 mA |
| Output low voltage | All output pins | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | Ports 1 to 3 | | — | — | 1.0 | V | $I_{OL}$ = 10 mA |
| Input leakage current | $\overline{RES}$ | $\lvert I_{in} \rvert$ | — | — | 10.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| | $\overline{STBY}$, NMI, MD1, MD0 | | — | — | 1.0 | µA | |
| | Port 7 | | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $AV_{CC}$ – 0.5 V |

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Three-state leakage current (off state) | Ports 1 to 6 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| Input pull-up MOS current | Ports 1 to 3 | $-I_P$ | 50 | — | 300 | µA | $V_{in}$ = 0 V |
| Input capacitance | $\overline{RES}$ (4) | $C_{in}$ | — | — | 80 | pF | $V_{in}$ = 0 V, f = 1 MHz, $T_a$ = 25°C |
| | NMI | | — | — | 50 | pF | |
| | P52, P47, P24, P23 | | — | — | 20 | pF | |
| | Input pins except (4) above | | — | — | 15 | pF | |
| Current dissipation*5 | Normal operation | $I_{CC}$ | — | 70 | 90 | mA | f = 20 MHz |
| | Sleep mode | | — | 55 | 75 | mA | f = 20 MHz |
| | Standby mode*6 | | — | 0.01 | 5.0 | µA | $T_a \le 50°C$ |
| | | | — | — | 20.0 | µA | $50°C < T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 1.5 | 3.0 | mA | |
| | Idle | | — | 0.01 | 5.0 | µA | $AV_{CC}$ = 2.0 V to 5.5 V |
| Analog power supply voltage*1 | | $AV_{CC}$ | 4.5 | — | 5.5 | V | Operating |
| | | | 2.0 | — | 5.5 | V | Idle/not used |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: *1 Do not leave the $AV_{CC}$, and $AV_{SS}$ pins open even if the A/D converter is not used.
Even if the A/D converter is not used, apply a value in the range 2.0 V to 5.5 V to $AV_{CC}$ by connection to the power supply ($V_{CC}$), or some other method.

*2 P67 to P60 include supporting module inputs multiplexed on those pins.

*3 $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

*4 The upper limit of the port 6 applied voltage is $V_{CC}$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}$ + 0.3 V and $AV_{CC}$ + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

*5 Current dissipation values are for $V_{IH}$ min = $V_{CC}$ – 0.5 V and $V_{IL}$ max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

*6 The values are for $V_{RAM} \le V_{CC} < 4.5$ V, $V_{IH}$ min = $V_{CC} \times 0.9$, and $V_{IL}$ max = 0.3 V.

**Table 22.26 DC Characteristics (2)**

Conditions: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$*1 = 4.0 V to 5.5 V, $V_{SS}$ = $AV_{SS}$*1 = 0 V,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

| Item | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60*2*4, $\overline{IRQ2}$ to $\overline{IRQ0}$*3 | (1) | $V_T^-$ | 1.0 | — | — | V | $V_{CC}$ = 4.5 V to 5.5 V |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | 0.4 | — | — | V | |
| | | | $V_T^-$ | 0.8 | — | — | V | $V_{CC}$ < 4.5 V |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | 0.3 | — | — | V | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0 | (2) | $V_{IH}$ | $V_{CC}$ – 0.7 | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | Port 7 | | | 2.0 | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | | 2.0 | — | $V_{CC}$ +0.3 | V | |
| Input low voltage | $\overline{RES}$, $\overline{STBY}$, MD1, MD0 | (3) | $V_{IL}$ | –0.3 | — | 0.5 | V | |
| | NMI, EXTAL, input pins except (1) and (3) above | | | –0.3 | — | 0.8 | V | |
| Output high voltage | All output pins | | $V_{OH}$ | $V_{CC}$ – 0.5 | — | — | V | $I_{OH}$ = –200 µA |
| | | | | 3.5 | — | — | V | $I_{OH}$ = –1 mA, $V_{CC}$= 4.5 V to 5.5 V |
| | | | | 3.0 | — | — | V | $I_{OH}$ = –1 mA, $V_{CC}$ < 4.5 V |
| Output low voltage | All output pins | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | Ports 1 to 3 | | | — | — | 1.0 | V | $I_{OL}$ = 10 mA |
| Input leakage current | $\overline{RES}$ | | $\lvert I_{in} \rvert$ | — | — | 10.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| | $\overline{STBY}$, NMI, MD1, MD0 | | | — | — | 1.0 | µA | |
| | Port 7 | | | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $AV_{CC}$ – 0.5 V |

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Three-state leakage current (off state) | Ports 1 to 6 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| Input pull-up MOS current | Ports 1 to 3 | $-I_P$ | 50 | — | 300 | µA | $V_{in}$ = 0 V, $V_{CC}$ = 4.5 V to 5.5 V |
| | | | 30 | — | 200 | µA | $V_{in}$ = 0 V, $V_{CC}$ < 4.5 V |
| Input capacitance | $\overline{RES}$ (4) | $C_{in}$ | — | — | 80 | pF | $V_{in}$ = 0 V, f = 1 MHz, $T_a$ = 25°C |
| | NMI | | — | — | 50 | pF | |
| | P52, P47, P24, P23 | | — | — | 20 | pF | |
| | Input pins except (4) above | | — | — | 15 | pF | |
| Current dissipation*5 | Normal operation | $I_{CC}$ | — | 55 | 75 | mA | f = 16 MHz |
| | Sleep mode | | — | 42 | 62 | mA | f = 16 MHz |
| | Standby mode*6 | | — | 0.01 | 5.0 | µA | $T_a \le 50°C$ |
| | | | — | — | 20.0 | µA | 50°C < $T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 1.5 | 3.0 | mA | |
| | Idle | | — | 0.01 | 5.0 | µA | $AV_{CC}$ = 2.0 V to 5.5 V |
| Analog power supply voltage*1 | | $AV_{CC}$ | 4.0 | — | 5.5 | V | Operating |
| | | | 2.0 | — | 5.5 | V | Idle/not used |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: *1 Do not leave the $AV_{CC}$, and $AV_{SS}$ pins open even if the A/D converter is not used.
Even if the A/D converter is not used, apply a value in the range 2.0 V to 5.5 V to $AV_{CC}$ by connection to the power supply ($V_{CC}$), or some other method.

*2 P67 to P60 include supporting module inputs multiplexed on those pins.

*3 $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

*4 The upper limit of the port 6 applied voltage is $V_{CC}$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}$ + 0.3 V and $AV_{CC}$ + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

*5 Current dissipation values are for $V_{IH}$ min = $V_{CC}$ – 0.5 V and $V_{IL}$ max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

*6 The values are for $V_{RAM} \le V_{CC}$ < 4.0 V, $V_{IH}$ min = $V_{CC} \times 0.9$, and $V_{IL}$ max = 0.3 V.

**Table 22.26 DC Characteristics (3)**

Conditions : $V_{CC}$ = 2.7 V to 5.5 V, $AV_{CC}$*1 = 2.7 V to 5.5 V,
$V_{SS}$ = $AV_{SS}$*1 = 0 V, $T_a$ = –20 to +75°C

| Item | | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|
| Schmitt trigger input voltage | P67 to P60*2*4, $\overline{IRQ2}$ to $\overline{IRQ0}$*3 | (1) | $V_T^-$ | $V_{CC} \times 0.2$ | — | — | V | |
| | | | $V_T^+$ | — | — | $V_{CC} \times 0.7$ | V | |
| | | | $V_T^+ - V_T^-$ | $V_{CC} \times 0.05$ | — | — | V | |
| Input high voltage | $\overline{RES}$, $\overline{STBY}$, NMI, MD1, MD0 | (2) | $V_{IH}$ | $V_{CC} \times 0.9$ | — | $V_{CC}$ +0.3 | V | |
| | EXTAL | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| | Port 7 | | | $V_{CC} \times 0.7$ | — | $AV_{CC}$ +0.3 | V | |
| | Input pins except (1) and (2) above | | | $V_{CC} \times 0.7$ | — | $V_{CC}$ +0.3 | V | |
| Input low voltage | $\overline{RES}$, $\overline{STBY}$, MD1, MD0 | (3) | $V_{IL}$ | –0.3 | — | $V_{CC} \times 0.1$ | V | |
| | NMI, EXTAL, input pins except (1) and (3) above | | | –0.3 | — | $V_{CC} \times 0.2$ | V | $V_{CC}$ < 4.0 V |
| | | | | | | 0.8 | V | $V_{CC}$ = 4.0 V to 5.5 V |
| Output high voltage | All output pins | | $V_{OH}$ | $V_{CC}$ – 0.5 | — | — | V | $I_{OH}$ = –200 µA |
| | | | | $V_{CC}$ – 1.0 | — | — | V | $I_{OH}$ = –1 mA ($V_{CC}$ < 4.0 V) |
| Output low voltage | All output pins | | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| | Ports 1 to 3 | | | — | — | 1.0 | V | $I_{OL}$ = 5 mA ($V_{CC}$ < 4.0 V), $I_{OL}$ = 10 mA (4.0 V ≤ $V_{CC}$ ≤ 5.5 V) |
| Input leakage current | $\overline{RES}$ | | $\lvert I_{in} \rvert$ | — | — | 10.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| | $\overline{STBY}$, NMI, MD1, MD0 | | | — | — | 1.0 | µA | |
| | Port 7 | | | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $AV_{CC}$ – 0.5 V |

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Three-state leakage current (off state) | Ports 1 to 6 | $\lvert I_{TSI} \rvert$ | — | — | 1.0 | µA | $V_{in}$ = 0.5 to $V_{CC}$ – 0.5 V |
| Input pull-up MOS current | Ports 1 to 3 | $-I_P$ | 10 | — | 150 | µA | $V_{in}$ = 0 V, $V_{CC}$ = 2.7 V to 3.6 V |
| Input capacitance | $\overline{RES}$ (4) | $C_{in}$ | — | — | 80 | pF | $V_{in}$ = 0 V, f = 1 MHz, Ta = 25°C |
| | NMI | | — | — | 50 | pF | |
| | P52, P47, P24, P23 | | — | — | 20 | pF | |
| | Input pins except (4) above | | — | — | 15 | pF | |
| Current dissipation*5 | Normal operation | $I_{CC}$ | — | 40 | 52 | mA | f = 10 MHz |
| | Sleep mode | | — | 30 | 42 | mA | f = 10 MHz |
| | Standby mode*6 | | — | 0.01 | 5.0 | µA | $T_a \leq 50°C$ |
| | | | — | — | 20.0 | µA | $50°C < T_a$ |
| Analog power supply current | During A/D conversion | $AI_{CC}$ | — | 1.5 | 3.0 | mA | |
| | Idle | | — | 0.01 | 5.0 | µA | $AV_{CC}$ = 2.0 V to 5.5 V |
| Analog power supply voltage*1 | | $AV_{CC}$ | 2.7 | — | 5.5 | V | Operating |
| | | | 2.0 | — | 5.5 | V | Idle/not used |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: *1 Do not leave the $AV_{CC}$, and $AV_{SS}$ pins open even if the A/D converter is not used.
Even if the A/D converter is not used, apply a value in the range 2.0 V to 5.5 V to $AV_{CC}$ by connection to the power supply ($V_{CC}$), or some other method.

*2 P67 to P60 include supporting module inputs multiplexed on those pins.

*3 $\overline{IRQ2}$ includes the $\overline{ADTRG}$ signal multiplexed on that pin.

*4 The upper limit of the port 6 applied voltage is $V_{CC}$ + 0.3 V when CIN input is not selected, and the lower of $V_{CC}$ + 0.3 V and $AV_{CC}$ + 0.3 V when CIN input is selected. When a pin is in output mode, the output voltage is equivalent to the applied voltage.

*5 Current dissipation values are for $V_{IH}$ min = $V_{CC}$ – 0.5 V and $V_{IL}$ max = 0.5 V with all output pins unloaded and the on-chip pull-up MOSs in the off state.

*6 The values are for $V_{RAM} \leq V_{CC} < 2.7$ V, $V_{IH}$ min = $V_{CC} \times 0.9$, and $V_{IL}$ max = 0.3 V.

**Table 22.27 Permissible Output Currents**

Conditions: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, Ta = –20 to +75°C (regular specifications),
Ta = –40 to +85°C (wide-range specifications)

| Item | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Permissible output low current (per pin) | Ports 1, 2, 3 | $I_{OL}$ | — | — | 10 | mA |
| | Other output pins | | — | — | 2 | mA |
| Permissible output low current (total) | Total of ports 1, 2, and 3 | $\sum I_{OL}$ | — | — | 80 | mA |
| | Total of all output pins, including the above | | — | — | 120 | mA |
| Permissible output high current (per pin) | All output pins | $-I_{OH}$ | — | — | 2 | mA |
| Permissible output high current (total) | Total of all output pins | $\sum -I_{OH}$ | — | — | 40 | mA |

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22.27.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 22.50 and 22.51.

**Table 22.27 Permissible Output Currents (cont)** **– Preliminary –**

Conditions: $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V, Ta = –20 to +75°C

| Item | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Permissible output low current (per pin) | Ports 1, 2, 3 | $I_{OL}$ | — | — | 2 | mA |
| | Other output pins | | — | — | 1 | mA |
| Permissible output low current (total) | Total of ports 1, 2, and 3 | $\sum I_{OL}$ | — | — | 40 | mA |
| | Total of all output pins, including the above | | — | — | 60 | mA |
| Permissible output high current (per pin) | All output pins | $-I_{OH}$ | — | — | 2 | mA |
| Permissible output high current (total) | Total of all output pins | $\sum -I_{OH}$ | — | — | 30 | mA |

Notes: 1. To protect chip reliability, do not exceed the output current values in table 22.27.
2. When driving a Darlington pair or LED, always insert a current-limiting resistor in the output line, as show in figures 22.50 and 22.51.

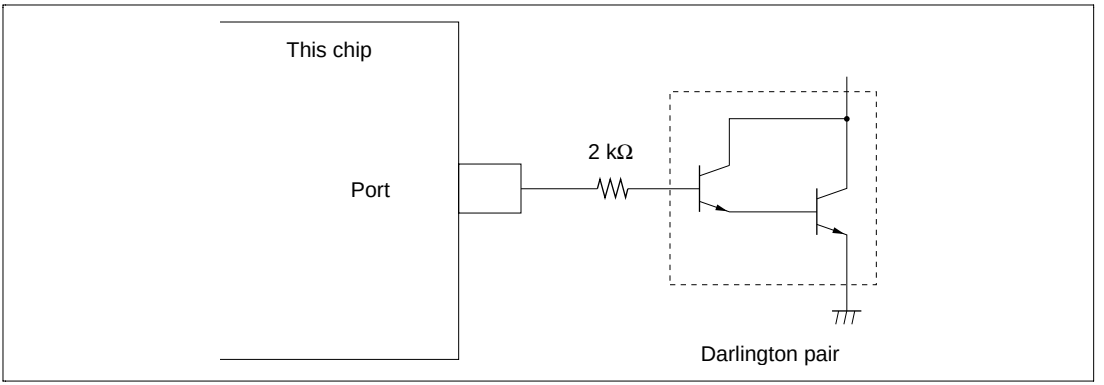



**Figure 22.50 Darlington Pair Drive Circuit (Example)**

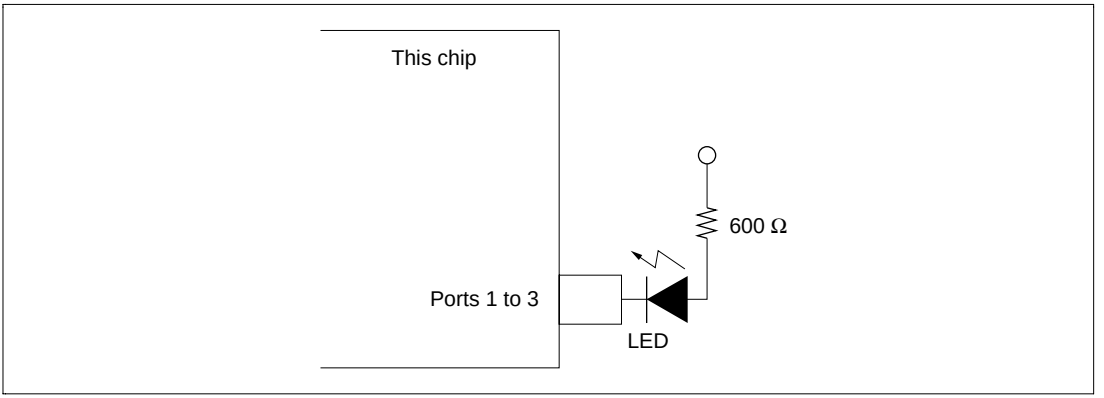



**Figure 22.51 LED Drive Circuit (Example)**

### 22.4.3 AC Characteristics

Figure 22.52 shows the test conditions for the AC characteristics.

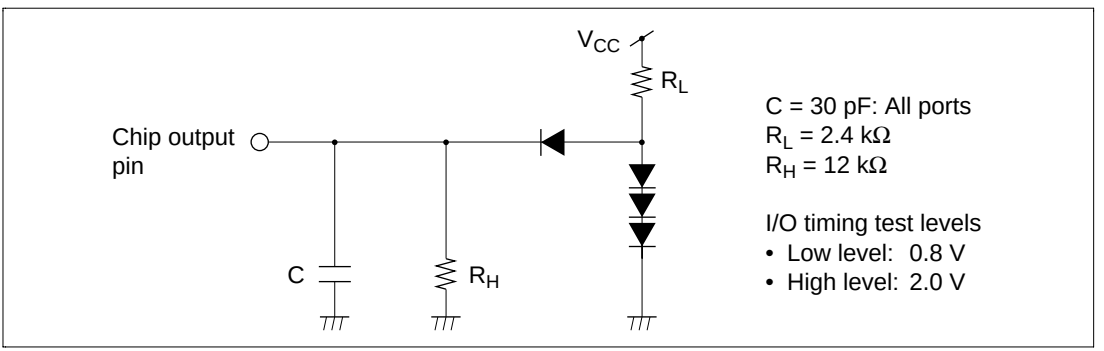



**Figure 22.52 Output Load Circuit**

### (1) Clock Timing

Table 22.28 shows the clock timing. The clock timing specified here covers clock (ø) output and clock pulse generator (crystal) and external clock input (EXTAL pin) oscillation settling times. For details of external clock input (EXTAL pin and EXCL pin) timing, see section 20, Clock Pulse Generator.

**Table 22.28 Clock Timing**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test Conditions |
| Clock cycle time | $t_{cyc}$ | 50 | 500 | 62.5 | 500 | 100 | 500 | ns | Figure 22.53 |
| Clock high pulse width | $t_{CH}$ | 17 | — | 20 | — | 30 | — | ns | Figure 22.53 |
| Clock low pulse width | $t_{CL}$ | 17 | — | 20 | — | 30 | — | ns | |
| Clock rise time | $t_{Cr}$ | — | 8 | — | 10 | — | 20 | ns | |
| Clock fall time | $t_{Cf}$ | — | 8 | — | 10 | — | 20 | ns | |
| Oscillation settling time at reset (crystal) | $t_{OSC1}$ | 10 | — | 10 | — | 20 | — | ms | Figure 22.54<br>Figure 22.55 |
| Oscillation settling time in software standby (crystal) | $t_{OSC2}$ | 8 | — | 8 | — | 8 | — | ms | |
| External clock output stabilization delay time | $t_{DEXT}$ | 500 | — | 500 | — | 500 | — | µs | |

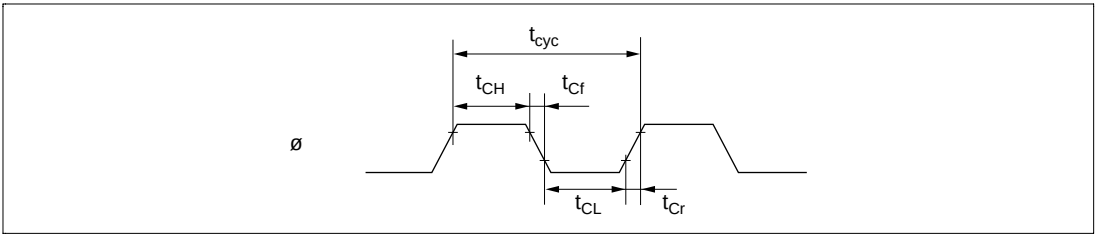



**Figure 22.53 System Clock Timing**

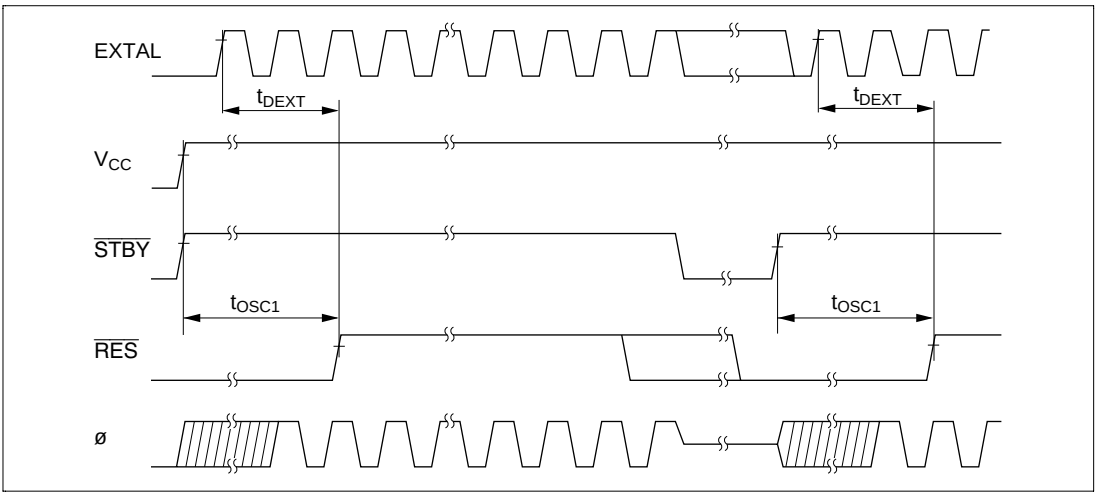



**Figure 22.54 Oscillation Settling Timing**

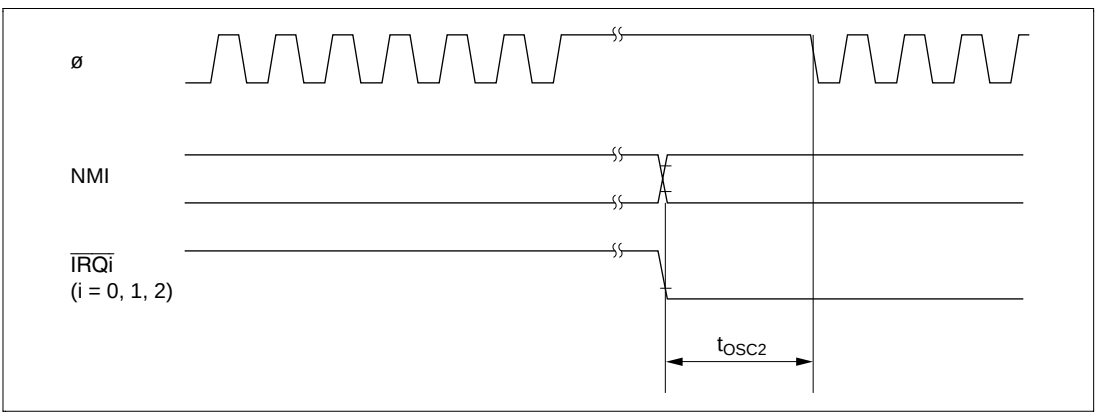



**Figure 22.55 Oscillation Setting Timing (Exiting Software Standby Mode)**

### (2) Control Signal Timing

Table 22.29 shows the control signal timing. The only external interrupts that can operate on the subclock (ø = 32.768 kHz) are NMI and IRQ0, 1, and IRQ2.

**Table 22.29 Control Signal Timing**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V, ø = 32.768 kHz, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C

| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | Test |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Conditions |
| $\overline{RES}$ setup time | $t_{RESS}$ | 200 | — | 200 | — | 300 | — | ns | Figure 22.56 |
| $\overline{RES}$ pulse width | $t_{RESW}$ | 20 | — | 20 | — | 20 | — | $t_{cyc}$ | |
| NMI setup time (NMI) | $t_{NMIS}$ | 150 | — | 150 | — | 250 | — | ns | Figure 22.57 |
| NMI hold time (NMI) | $t_{NMIH}$ | 10 | — | 10 | — | 10 | — | ns | |
| NMI pulse width (exiting software standby mode) | $t_{NMIW}$ | 200 | — | 200 | — | 200 | — | ns | |
| IRQ setup time ($\overline{IRQ2}$ to $\overline{IRQ0}$) | $t_{IRQS}$ | 150 | — | 150 | — | 250 | — | ns | |
| IRQ hold time ($\overline{IRQ2}$ to $\overline{IRQ0}$) | $t_{IRQH}$ | 10 | — | 10 | — | 10 | — | ns | |
| IRQ pulse width ($\overline{IRQ2}$ to $\overline{IRQ0}$) (exiting software standby mode) | $t_{IRQW}$ | 200 | — | 200 | — | 200 | — | ns | |

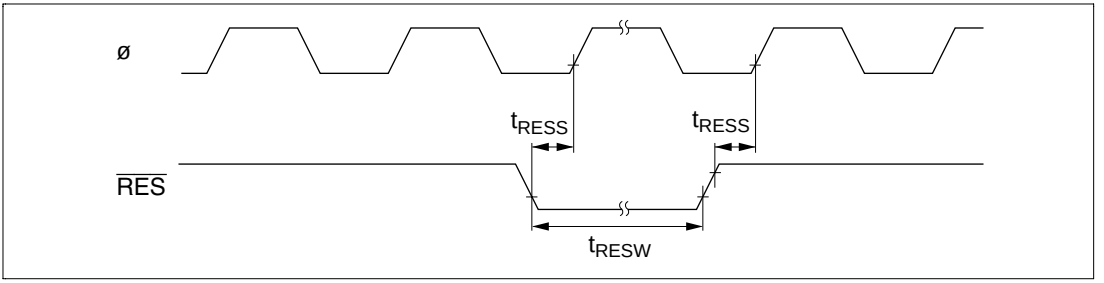



**Figure 22.56 Reset Input Timing**

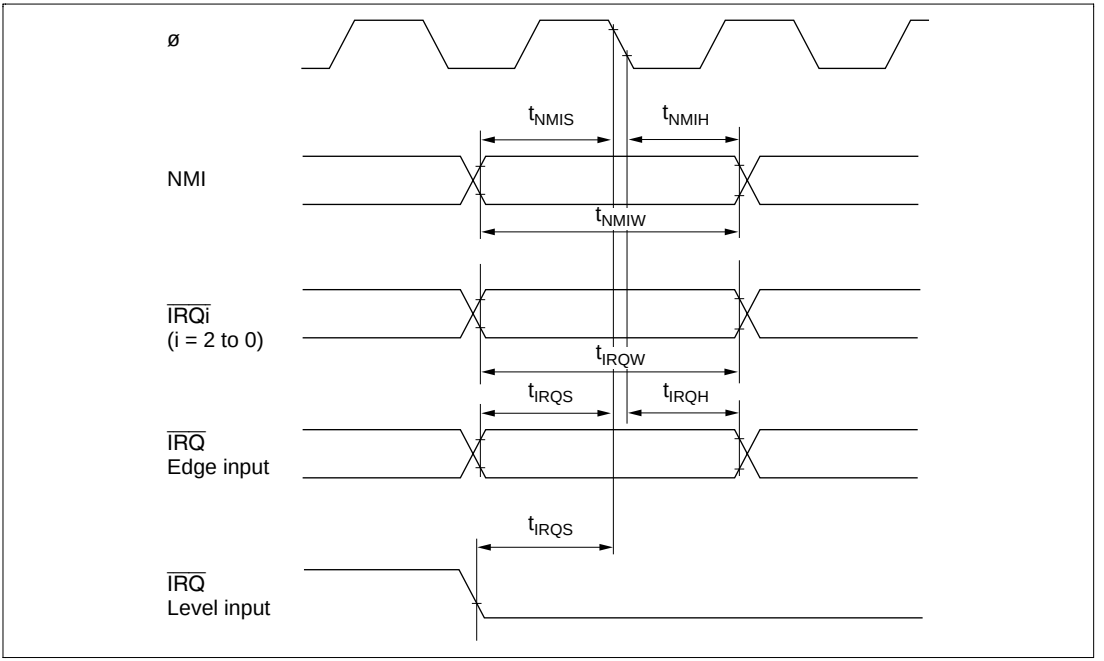



**Figure 22.57 Interrupt Input Timing**

### (3) Bus Timing

Table 22.30 shows the bus timing. Operation in external expansion mode is not guaranteed when operating on the subclock (ø = 32.768 kHz).

**Table 22.30 Bus Timing**

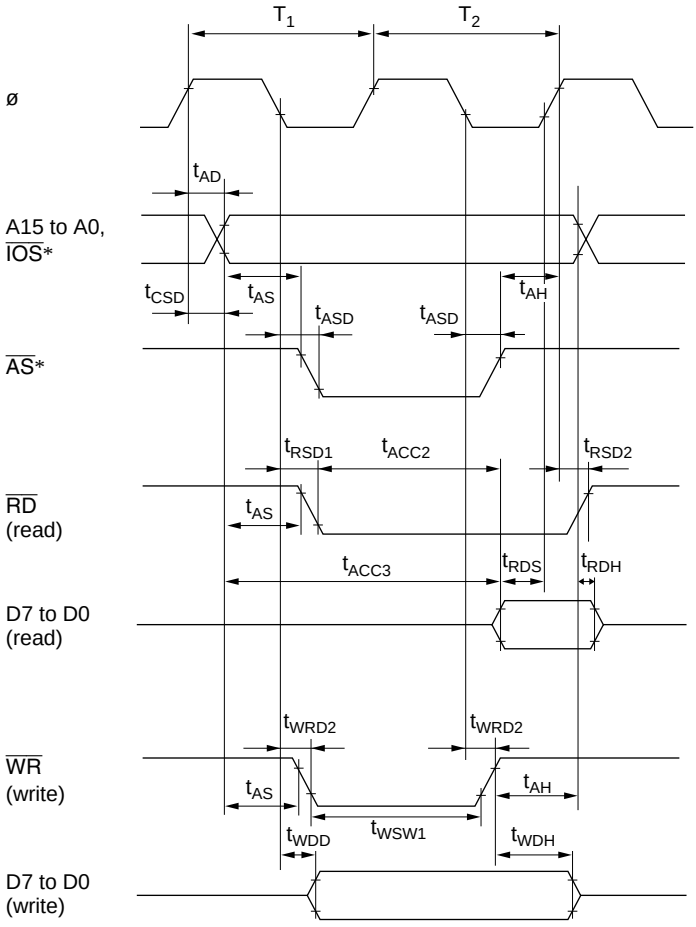
Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

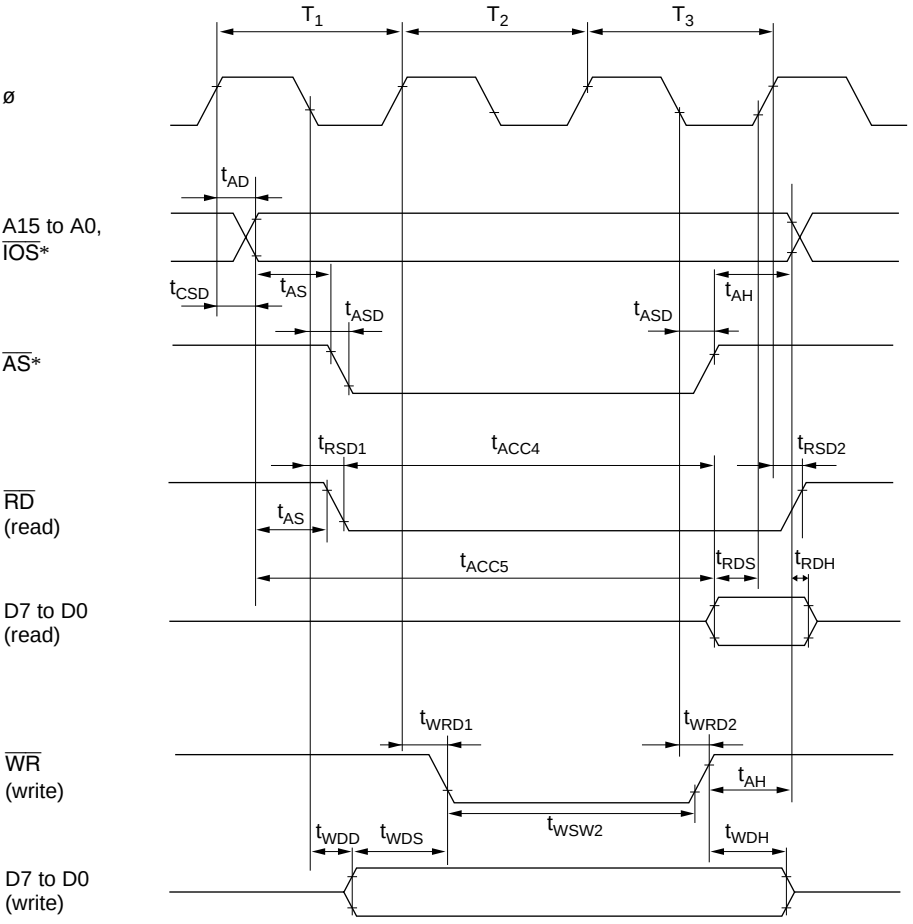
| | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 20 MHz | | 16 MHz | | 10 MHz | | | |
| Item | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test Conditions |
| Address delay time | $t_{AD}$ | — | 20 | — | 30 | — | 40 | ns | Figure 22.58 to figure 22.62 |
| Address setup time | $t_{AS}$ | 0.5 × $t_{cyc}$ – 15 | — | 0.5 × $t_{cyc}$ – 20 | — | 0.5 × $t_{cyc}$ – 30 | — | ns | |
| Address hold time | $t_{AH}$ | 0.5 × $t_{cyc}$ – 10 | — | 0.5 × $t_{cyc}$ – 15 | — | 0.5 × $t_{cyc}$ – 20 | — | ns | |
| $\overline{CS}$ delay time ($\overline{IOS}$) | $t_{CSD}$ | — | 20 | — | 30 | — | 40 | ns | |
| $\overline{AS}$ delay time | $t_{ASD}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{RD}$ delay time 1 | $t_{RSD1}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{RD}$ delay time 2 | $t_{RSD2}$ | — | 30 | — | 45 | — | 60 | ns | |
| Read data setup time | $t_{RDS}$ | 15 | — | 20 | — | 35 | — | ns | |
| Read data hold time | $t_{RDH}$ | 0 | — | 0 | — | 0 | — | ns | |
| Read data access time 1 | $t_{ACC1}$ | — | 1.0 × $t_{cyc}$ – 30 | — | 1.0 × $t_{cyc}$ – 40 | — | 1.0 × $t_{cyc}$ – 60 | ns | |
| Read data access time 2 | $t_{ACC2}$ | — | 1.5 × $t_{cyc}$ – 25 | — | 1.5 × $t_{cyc}$ – 35 | — | 1.5 × $t_{cyc}$ – 50 | ns | |

| Item | Symbol | Condition A 20 MHz Min | Condition A 20 MHz Max | Condition B 16 MHz Min | Condition B 16 MHz Max | Condition C 10 MHz Min | Condition C 10 MHz Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|
| Read data access time 3 | $t_{ACC3}$ | — | $2.0 \times t_{cyc} - 30$ | — | $2.0 \times t_{cyc} - 40$ | — | $2.0 \times t_{cyc} - 60$ | ns | Figure 22.58 to figure 22.62 |
| Read data access time 4 | $t_{ACC4}$ | — | $2.5 \times t_{cyc} - 25$ | — | $2.5 \times t_{cyc} - 35$ | — | $2.5 \times t_{cyc} - 50$ | ns | |
| Read data access time 5 | $t_{ACC5}$ | — | $3.0 \times t_{cyc} - 30$ | — | $3.0 \times t_{cyc} - 40$ | — | $3.0 \times t_{cyc} - 60$ | ns | |
| $\overline{WR}$ delay time 1 | $t_{WRD1}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{WR}$ delay time 2 | $t_{WRD2}$ | — | 30 | — | 45 | — | 60 | ns | |
| $\overline{WR}$ pulse width 1 | $t_{WSW1}$ | $1.0 \times t_{cyc} - 20$ | — | $1.0 \times t_{cyc} - 30$ | — | $1.0 \times t_{cyc} - 40$ | — | ns | |
| $\overline{WR}$ pulse width 2 | $t_{WSW2}$ | $1.5 \times t_{cyc} - 20$ | — | $1.5 \times t_{cyc} - 30$ | — | $1.5 \times t_{cyc} - 40$ | — | ns | |
| Write data delay time | $t_{WDD}$ | — | 30 | — | 45 | — | 60 | ns | |
| Write data setup time | $t_{WDS}$ | 0 | — | 0 | — | 0 | — | ns | |
| Write data hold time | $t_{WDH}$ | 10 | — | 15 | — | 20 | — | ns | |
| $\overline{WAIT}$ setup time | $t_{WTS}$ | 30 | — | 45 | — | 60 | — | ns | |
| $\overline{WAIT}$ hold time | $t_{WTH}$ | 5 | — | 5 | — | 10 | — | ns | |



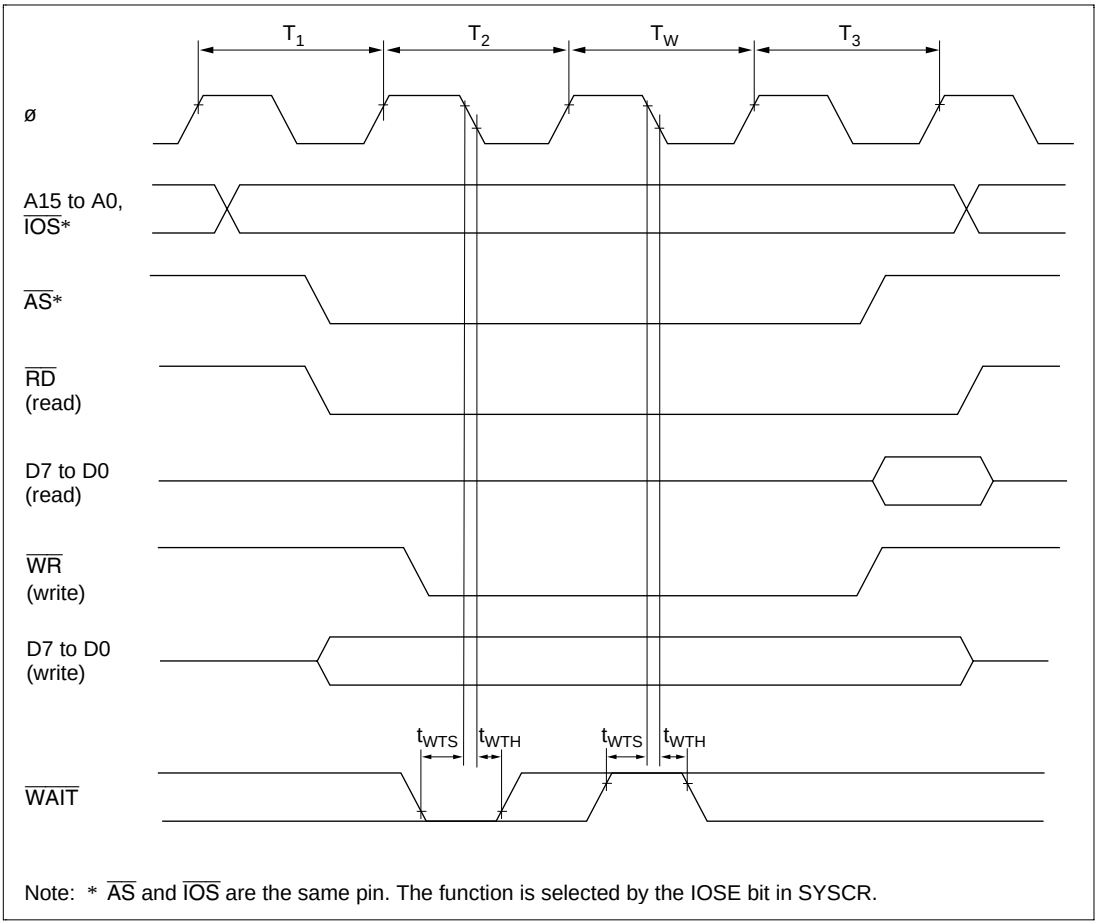

Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.58 Basic Bus Timing (Two-State Access)**



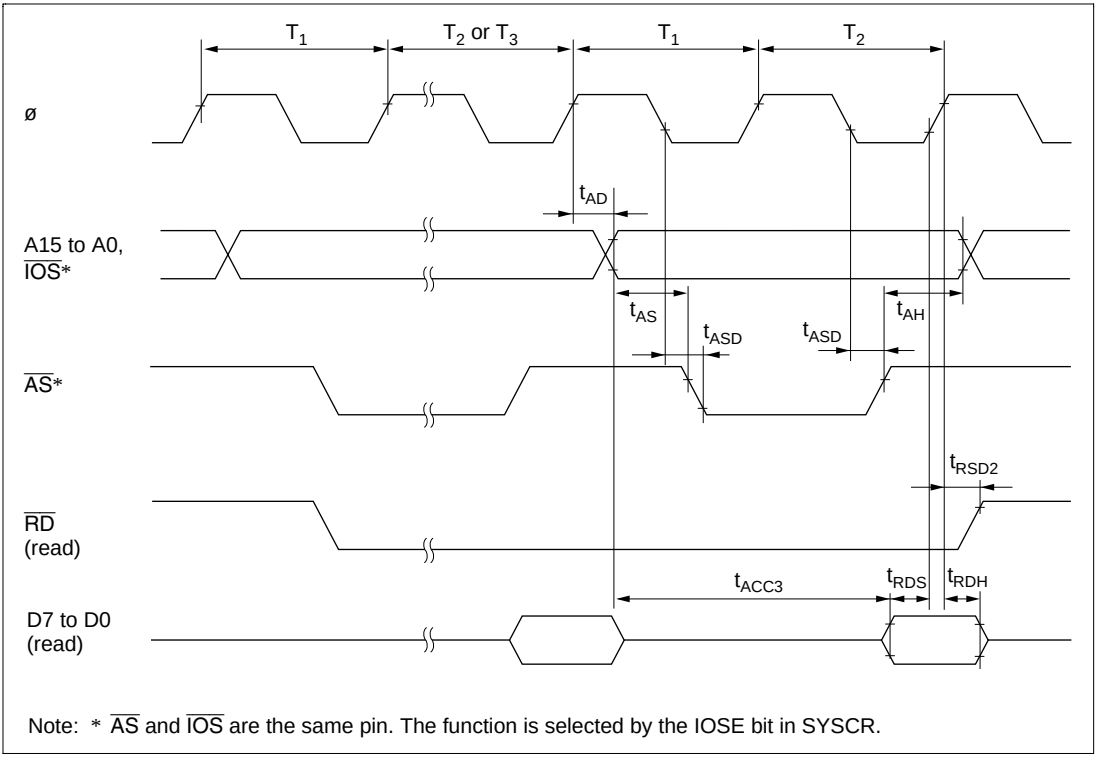

Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.59 Basic Bus Timing (Three-State Access)**



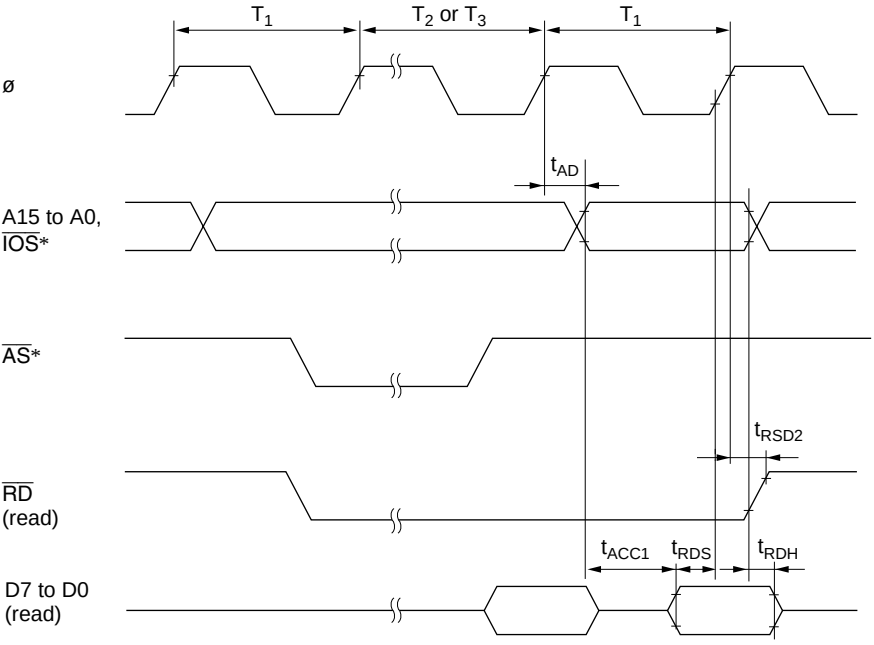

Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.60 Basic Bus Timing (Three-State Access with One Wait State)**




Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.61 Burst ROM Access Timing (Two-State Access)**




Note: * AS and IOS are the same pin. The function is selected by the IOSE bit in SYSCR.

**Figure 22.62 Burst ROM Access Timing (One-State Access)**

### (4) Timing of On-Chip Supporting Modules

Table 22.31 shows the on-chip supporting module timing. The only on-chip supporting modules that can operate in subclock operation (ø = 32.768 kHz) are the I/O ports, external interrupts (NMI and IRQ0, 1, and IRQ2), the watchdog timer, and the 8-bit timer (channels 0 and 1).

**Table 22.31 Timing of On-Chip Supporting Modules**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $V_{SS}$ = 0 V, ø = 32.768 kHz*, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $V_{SS}$ = 0 V, ø = 32.768 kHz*, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C (regular specifications), $T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V, $V_{SS}$ = 0 V, ø = 32.768 kHz*, 2 MHz to maximum operating frequency, $T_a$ = –20 to +75°C

| | | | | Condition A | | Condition B | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 20 MHz | | 16 MHz | | 10 MHz | | | |
| Item | | | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test Conditions |
| I/O ports | Output data delay time | | $t_{PWD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.63 |
| | Input data setup time | | $t_{PRS}$ | 30 | — | 30 | — | 50 | — | | |
| | Input data hold time | | $t_{PRH}$ | 30 | — | 30 | — | 50 | — | | |
| FRT | Timer output delay time | | $t_{FTOD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.64 |
| | Timer input setup time | | $t_{FTIS}$ | 30 | — | 30 | — | 50 | — | | |
| | Timer clock input setup time | | $t_{FTCS}$ | 30 | — | 30 | — | 50 | — | | Figure 22.65 |
| | Timer clock pulse width | Single edge | $t_{FTCWH}$ | 1.5 | — | 1.5 | — | 1.5 | — | $t_{cyc}$ | |
| | | Both edges | $t_{FTCWL}$ | 2.5 | — | 2.5 | — | 2.5 | — | | |

| Item | | | Symbol | Condition A 20 MHz Min | Condition A 20 MHz Max | Condition B 16 MHz Min | Condition B 16 MHz Max | Condition C 10 MHz Min | Condition C 10 MHz Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMR | Timer output delay time | | $t_{TMOD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.66 |
| | Timer reset input setup time | | $t_{TMRS}$ | 30 | — | 30 | — | 50 | — | | Figure 22.68 |
| | Timer clock input setup time | | $t_{TMCS}$ | 30 | — | 30 | — | 50 | — | | Figure 22.67 |
| | Timer clock pulse width | Single edge | $t_{TMCWH}$ | 1.5 | — | 1.5 | — | 1.5 | — | $t_{cyc}$ | |
| | | Both edges | $t_{TMCWL}$ | 2.5 | — | 2.5 | — | 2.5 | — | | |
| SCI | Input clock cycle | Asynchronous | $t_{Scyc}$ | 4 | — | 4 | — | 4 | — | $t_{cyc}$ | Figure 22.69 |
| | | Synchronous | | 6 | — | 6 | — | 6 | — | | |
| | Input clock pulse width | | $t_{SCKW}$ | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | $t_{Scyc}$ | |
| | Input clock rise time | | $t_{SCKr}$ | — | 1.5 | — | 1.5 | — | 1.5 | $t_{cyc}$ | |
| | Input clock fall time | | $t_{SCKf}$ | — | 1.5 | — | 1.5 | — | 1.5 | | |
| | Transmit data delay time (synchronous) | | $t_{TXD}$ | — | 50 | — | 50 | — | 100 | ns | Figure 22.70 |
| | Receive data setup time (synchronous) | | $t_{RXS}$ | 50 | — | 50 | — | 100 | — | ns | |
| | Receive data hold time (synchronous) | | $t_{RXH}$ | 50 | — | 50 | — | 100 | — | ns | |
| A/D converter | Trigger input setup time | | $t_{TRGS}$ | 30 | — | 30 | — | 50 | — | ns | Figure 22.71 |

Note: * Only supporting modules that can be used in subclock operation

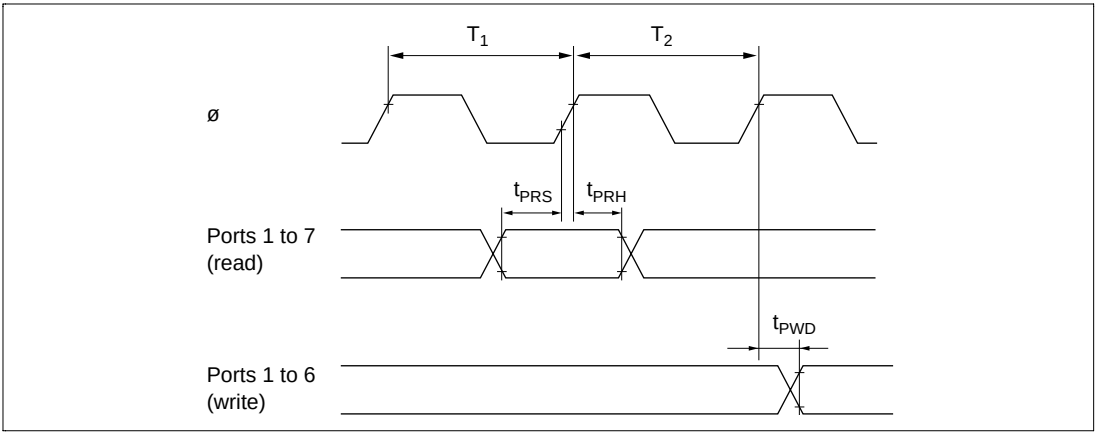



**Figure 22.63 I/O Port Input/Output Timing**

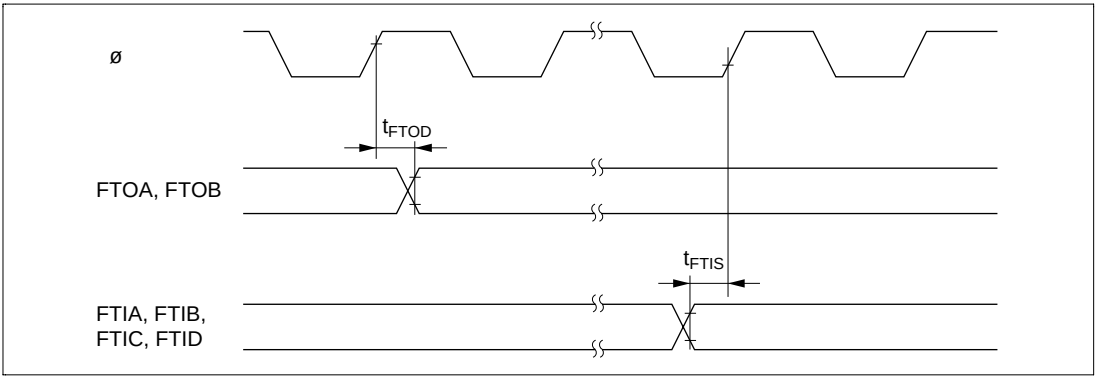



**Figure 22.64 FRT Input/Output Timing**

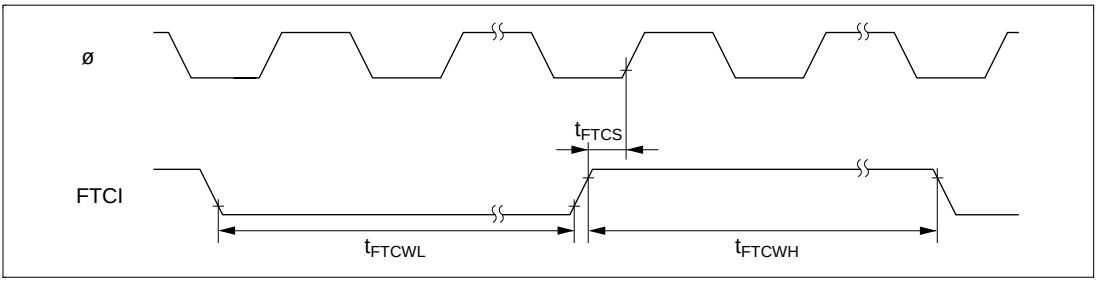



**Figure 22.65 FRT Clock Input Timing**

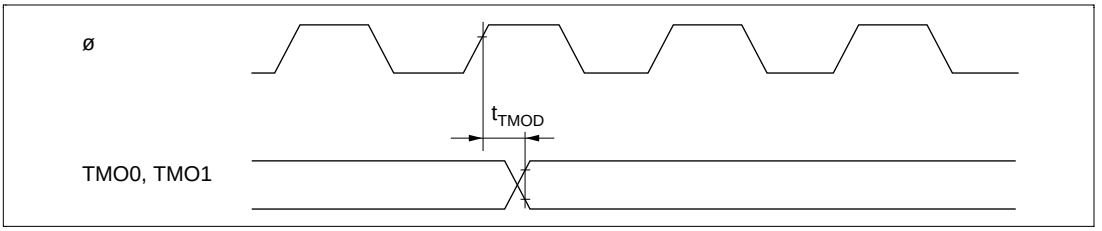



**Figure 22.66 8-Bit Timer Output Timing**

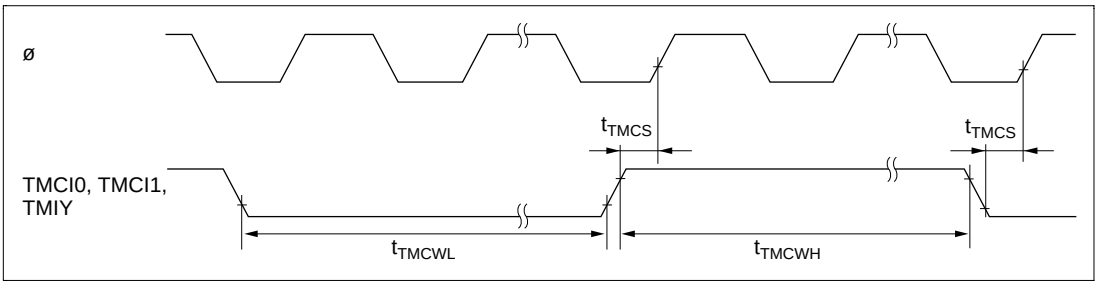



**Figure 22.67 8-Bit Timer Clock Input Timing**

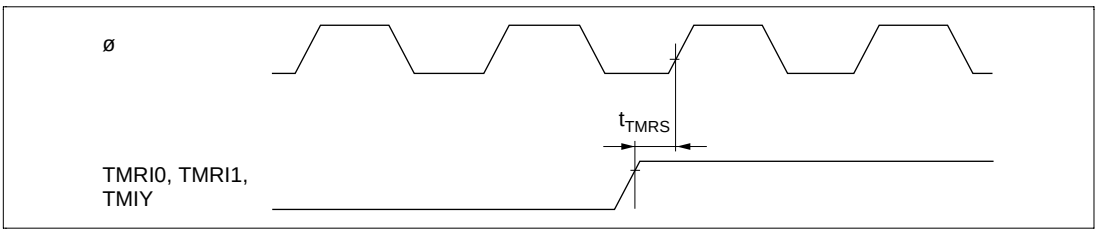



**Figure 22.68 8-Bit Timer Reset Input Timing**

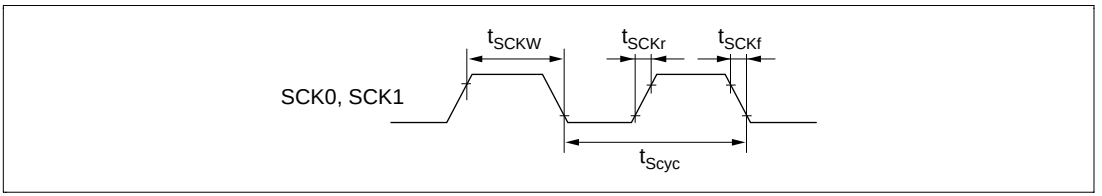



**Figure 22.69 SCK Clock Input Timing**

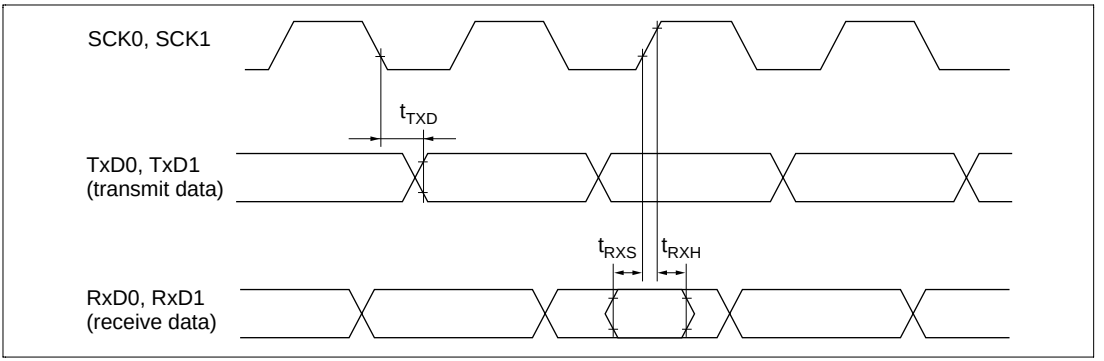



**Figure 22.70 SCI Input/Output Timing (Synchronous Mode)**

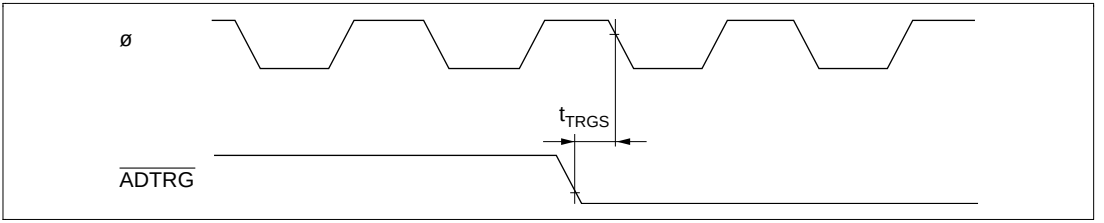



**Figure 22.71 A/D Converter External Trigger Input Timing**

### 22.4.4 A/D Conversion Characteristics

Tables 22.32 and 22.33 list the A/D conversion characteristics.

**Table 22.32 A/D Conversion Characteristics (AN7 to AN0 Input: 134/266-State Conversion)**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $AV_{CC}$ = 5.0 V ± 10%
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$ = 4.0 V to 5.5 V
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V, $AV_{CC}$ = 2.7 V to 5.5 V
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

| | Condition A | | | Condition B | | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 20 MHz | | | 16 MHz | | | 10 MHz | | | |
| **Item** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Resolution | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | Bits |
| Conversion time*5 | — | — | 6.7 | — | — | 8.4 | — | — | 13.4 | µs |
| Analog input capacitance | — | — | 20 | — | — | 20 | — | — | 20 | pF |
| Permissible signal-source impedance | — | — | 10*3<br>5*4 | — | — | 10*3<br>5*4 | — | — | 10*1<br>5*2 | kΩ |
| Nonlinearity error | — | — | ±3.0 | — | — | ±3.0 | — | — | ±7.0 | LSB |
| Offset error | — | — | ±3.5 | — | — | ±3.5 | — | — | ±7.5 | LSB |
| Full-scale error | — | — | ±3.5 | — | — | ±3.5 | — | — | ±7.5 | LSB |
| Quantization error | — | — | ±0.5 | — | — | ±0.5 | — | — | ±0.5 | LSB |
| Absolute accuracy | — | — | ±4.0 | — | — | ±4.0 | — | — | ±8.0 | LSB |

Notes: *1 When 4.0 V ≤ $AV_{CC}$ ≤ 5.5 V
*2 When 2.7 V ≤ $AV_{CC}$ < 4.0 V
*3 When conversion time ≥ 11. 17 µs (CKS = 1 and ø ≤ 12 MHz, or CKS = 0)
*4 When conversion time < 11. 17 µs (CKS = 1 and ø > 12 MHz)
*5 At the maximum operating frequency in single mode

**Table 22.33 A/D Conversion Characteristics**
**(CIN7 to CIN0 Input: 134/266-State Conversion)**

Condition A: $V_{CC}$ = 5.0 V ± 10%, $AV_{CC}$ = 5.0 V ± 10%
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition B: $V_{CC}$ = 4.0 V to 5.5 V, $AV_{CC}$ = 4.0 V to 5.5 V
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C (regular specifications),
$T_a$ = –40 to +85°C (wide-range specifications)

Condition C: $V_{CC}$ = 2.7 V to 5.5 V, $AV_{CC}$ = 2.7 V to 5.5 V
$V_{SS}$ = $AV_{SS}$ = 0 V, ø = 2 MHz to maximum operating frequency,
$T_a$ = –20 to +75°C

| | Condition A | | | Condition B | | | Condition C | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | 20 MHz | | | 16 MHz | | | 10 MHz | | | |
| **Item** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| Resolution | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | Bits |
| Conversion time*5 | — | — | 6.7 | — | — | 8.4 | — | — | 13.4 | µs |
| Analog input capacitance | — | — | 20 | — | — | 20 | — | — | 20 | pF |
| Permissible signal-source impedance | — | — | 10*3<br>5*4 | — | — | 10*3<br>5*4 | — | — | 10*1<br>5*2 | kΩ |
| Nonlinearity error | — | — | ±5.0 | — | — | ±5.0 | — | — | ±11.0 | LSB |
| Offset error | — | — | ±5.5 | — | — | ±5.5 | — | — | ±11.5 | LSB |
| Full-scale error | — | — | ±5.5 | — | — | ±5.5 | — | — | ±11.5 | LSB |
| Quantization error | — | — | ±0.5 | — | — | ±0.5 | — | — | ±0.5 | LSB |
| Absolute accuracy | — | — | ±6.0 | — | — | ±6.0 | — | — | ±12.0 | LSB |

Notes: *1 When 4.0 V ≤ $AV_{CC}$ ≤ 5.5 V
*2 When 2.7 V ≤ $AV_{CC}$ < 4.0 V
*3 When conversion time ≥ 11. 17 µs (CKS = 1 and ø ≤ 12 MHz, or CKS = 0)
*4 When conversion time < 11. 17 µs (CKS = 1 and ø > 12 MHz)
*5 At the maximum operating frequency in single mode

### 22.4.5 Usage Note

The specifications of the H8S/2128 F-ZTAT version and H8S/2124 Series mask ROM version differ in terms of on-chip module functions provided and port (P47, P52) output specifications. Also, while the F-ZTAT and mask ROM versions both satisfy the electrical characteristics shown in this manual, actual electrical characteristic values, operating margins, noise margins, and other properties may vary due to differences in manufacturing process, on-chip ROM, layout patterns, etc.

When system evaluation testing is carried out using the H8S/2128 F-ZTAT version, the above differences must be taken into consideration in system design, and the same evaluation testing should also be conducted for the mask ROM version when changing over to that version.

# Appendix F Product Code Lineup

**Table F.1 H8S/2128 Series and H8S/2124 Series Product Code Lineup — Preliminary —**

| Product Type | | | | Product Code | Mark Code | Package (Hitachi Package Code) | Notes |
|---|---|---|---|---|---|---|---|
| H8S/2128 Series | H8S/2128 | F-ZTAT version | Standard product (5 V/4 V version) | HD64F2128 | HD64F2128PS20 | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD64F2128FA20 | 64-pin QFP (FP-64A) | |
| | | | | | HD64F2128TF20 | 80-pin TQFP (TFP-80C) | |
| | | | Low-voltage version (3 V version) | HD64F2128V | HD64F2128VPS10 | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD64F2128VFA10 | 64-pin QFP (FP-64A) | |
| | | | | | HD64F2128VTF10 | 80-pin TQFP (TFP-80C) | |
| | H8S/2127 | Mask ROM version | Standard product (5 V version, 4 V version, 3 V version) | HD6432127R | HD6432127R(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432127R(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432127R(***)TF | 80-pin TQFP (TFP-80C) | |
| | | | Version with on-chip $I^2C$ bus interface (5 V version, 4 V version, 3 V version) | HD6432127RW | HD6432127RW(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432127RW(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432127RW(***)TF | 80-pin TQFP (TFP-80C) | |
| | H8S/2126 | Mask ROM version | Standard product (5 V version, 4 V version, 3 V version) | HD6432126R | HD6432126R(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432126R(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432126R(***)TF | 80-pin TQFP (TFP-80C) | |
| | | | Version with on-chip $I^2C$ bus interface (5 V version, 4 V version, 3 V version) | HD6432126RW | HD6432126RW(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432126RW(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432126RW(***)TF | 80-pin TQFP (TFP-80C) | |

| Product Type | | | | Product Code | Mark Code | Package (Hitachi Package Code) | Notes |
|---|---|---|---|---|---|---|---|
| H8S/2128S Series | H8S/2128S | Mask ROM version | Standard product (5 V version, 4 V version) | HD6432128S | HD6432128S(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432128S(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432128S(***)TF | 80-pin TQFP (TFP-80C) | |
| | | | Low-voltage version (3 V version) | HD6432128SV | HD6432128SV(***)PS | 64-pin shrink DIP (DP-64S) | Under planning |
| | | | | | HD6432128SV(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432128SV(***)TF | 80-pin TQFP (TFP-80C) | |
| | | | Standard product with on-chip $I^2C$ bus interface (5 V version, 4 V version) | HD6432128SW | HD6432128SW(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432128SW(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432128SW(***)TF | 80-pin TQFP (TFP-80C) | |
| | | | Low-voltage version with on-chip $I^2C$ bus interface (3 V version) | HD6432128SVW | HD6432128SVW(***)PS | 64-pin shrink DIP (DP-64S) | Under planning |
| | | | | | HD6432128SVW(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432128SVW(***)TF | 80-pin TQFP (TFP-80C) | |
| | H8S/2127S | Mask ROM version | Standard product (5 V version, 4 V version) | HD6432127S | HD6432127S(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432127S(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432127S(***)TF | 80-pin TQFP (TFP-80C) | |
| | | | Low-voltage version (3 V version) | HD6432127SV | HD6432127SV(***)PS | 64-pin shrink DIP (DP-64S) | Under planning |
| | | | | | HD6432127SV(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432127SV(***)TF | 80-pin TQFP (TFP-80C) | |
| | | | Standard product with on-chip $I^2C$ bus interface (5 V version, 4 V version) | HD6432127SW | HD6432127SW(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432127SW(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432127SW(***)TF | 80-pin TQFP (TFP-80C) | |
| | | | Low-voltage version with on-chip $I^2C$ bus interface (3 V version) | HD6432127SVW | HD6432127SVW(***)PS | 64-pin shrink DIP (DP-64S) | Under planning |
| | | | | | HD6432127SVW(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432127SVW(***)TF | 80-pin TQFP (TFP-80C) | |

| Product Type | | | | Product Code | Mark Code | Package (Hitachi Package Code) | Notes |
|---|---|---|---|---|---|---|---|
| H8S/2124 Series | H8S/2122 | Mask ROM version | Standard product (5 V version, 4 V version, 3 V version) | HD6432122 | HD6432122(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432122(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432122(***)TF | 80-pin TQFP (TFP-80C) | |
| | H8S/2120 | Mask ROM version | Standard product (5 V version, 4 V version, 3 V version) | HD6432120 | HD6432120(***)PS | 64-pin shrink DIP (DP-64S) | |
| | | | | | HD6432120(***)FA | 64-pin QFP (FP-64A) | |
| | | | | | HD6432120(***)TF | 80-pin TQFP (TFP-80C) | |

Note: (***) is the ROM code.

The F-ZTAT version of the H8S/2128 has an on-chip $I^2C$ bus interface as standard.

The F-ZTAT 5 V/4 V version supports the operating ranges of the 5 V version and the 4 V version.

The operating range of the F-ZTAT low-voltage version will be decided later.

The above table includes products in the planning stage or under development. Information on the status of individual products can be obtained from Hitachi's sales offices.

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