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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HD74HC390

Dual Decade Counters



ADE-205-503 (Z)

1st. Edition

Sep. 2000

Description

The HD74HC390 incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual binary, or various combinations up to a single divide-by-100 counter.

The HD74HC390 is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

Features

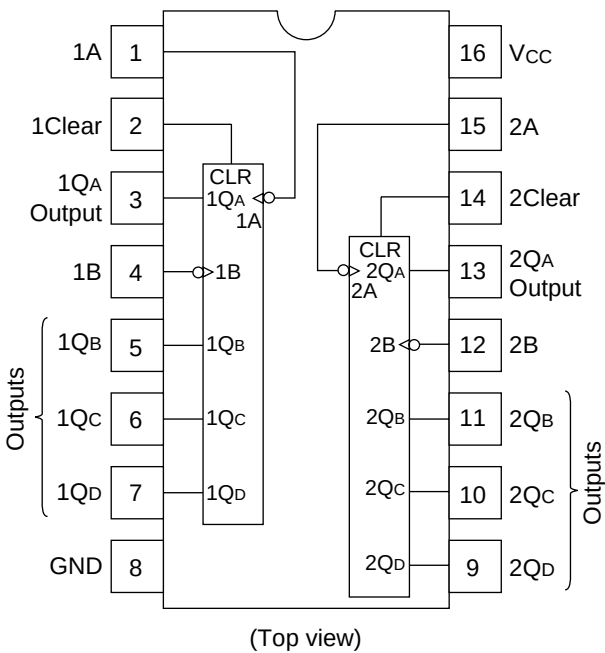
- High Speed Operation: t_{pd} (Clock A to Q_A) = 11 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)

Function Table

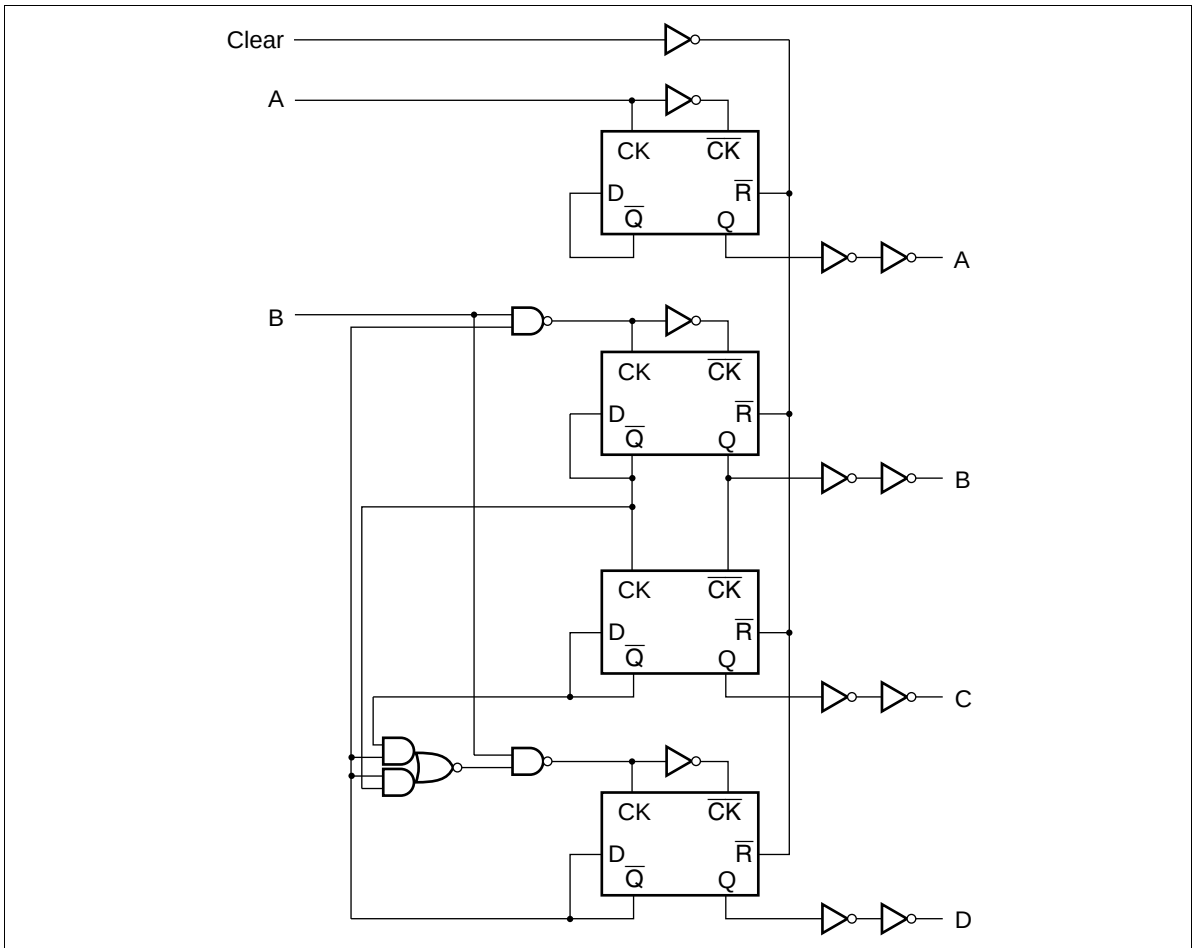
Clock

A	B	Clear	Operation
X	X	H	Clear $\div 2$ and $\div 5$
	X	L	Increment $\div 2$
X		L	Increment $\div 5$

Pin Arrangement



Block Diagram (1/2)



DC Characteristics

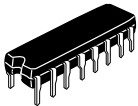
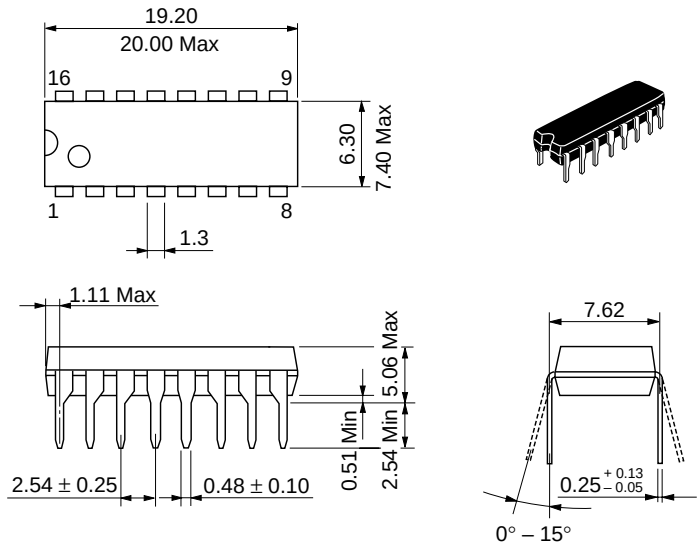
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V _{CC} (V)	Ta = 25°C		Ta = −40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min			Max
Maximum clock frequency	f _{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t _{PLH}	2.0	—	—	120	—	150	ns	Clock A to Q _A
		4.5	—	11	24	—	30		
		6.0	—	—	20	—	26		
	t _{PHL}	2.0	—	—	290	—	365	ns	Clock A to Q _C (Q _A connected to Clock B)
		4.5	—	32	58	—	73		
		6.0	—	—	49	—	62		
	t _{PLH}	2.0	—	—	130	—	165	ns	Clock B to Q _B
		4.5	—	16	26	—	33		
		6.0	—	—	22	—	28		
	t _{PHL}	2.0	—	—	185	—	230	ns	Clock B to Q _C
		4.5	—	20	37	—	46		
		6.0	—	—	31	—	39		
	t _{PLH}	2.0	—	—	130	—	165	ns	Clock B to Q _D
		4.5	—	15	26	—	33		
		6.0	—	—	22	—	28		
	t _{PHL}	2.0	—	—	165	—	205	ns	Clear to Q _A , Q _B , Q _C , Q _D
		4.5	—	14	33	—	41		
		6.0	—	—	28	—	35		
Pulse width	t _w	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Removal time	t _h	2.0	25	—	—	31	—	ns	
		4.5	5	1	—	6	—		
		6.0	4	—	—	5	—		
Output rise/fall time	t _{TLH}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C _{in}	—	—	5	10	—	10	pF	

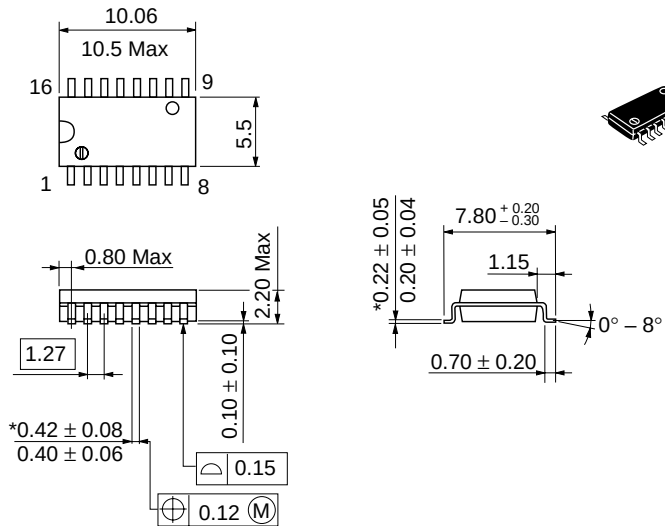
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

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