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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HD74HCT242/HD74HCT243

Quad. Bus Transceivers (with 3-state outputs)



ADE-205-552 (Z)
1st. Edition
Sep. 2000

Description

The HD74HCT242 is an inverting buffer and the HD74HCT243 is a noninverting buffer. Each device has one active high enable (GBA), and one active low enable ($\overline{\text{GAB}}$). GBA enables the A outputs and $\overline{\text{GAB}}$ enables the B outputs.

The device does not have schmitt trigger inputs.

Features

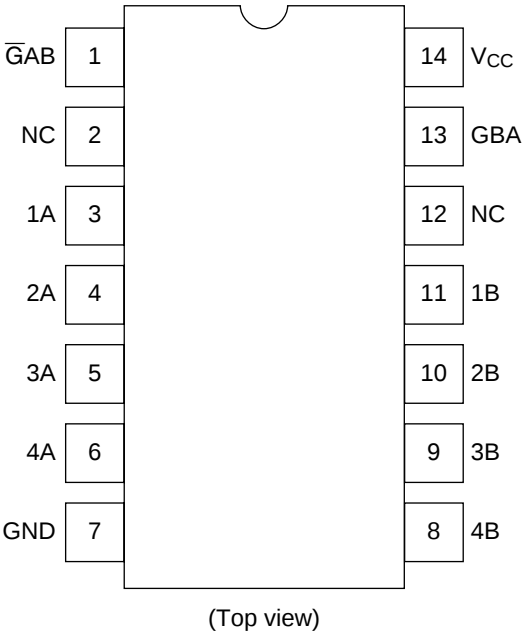
- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (A to Y) = 9.5 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: $1\text{ }\mu\text{A}$ max
- Low Quiescent Supply Current: I_{CC} (static) = $4\text{ }\mu\text{A}$ max ($T_a = 25^\circ\text{C}$)

Function Table

		HD74HCT242		HD74HCT243	
Control Inputs		Data Port Status		Data Port Status	
$\overline{\text{G}}_{\text{AB}}$	G_{BA}	A	B	A	B
H	H	$\overline{\text{O}}$	I	O	I
L	H	Z	Z	Z	Z
H	L	Z	Z	Z	Z
L	L	I	$\overline{\text{O}}$	I	O

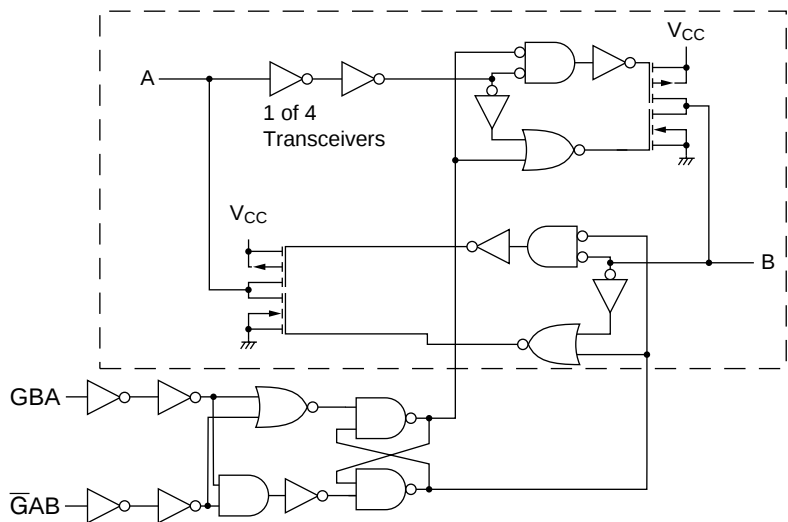
- I : Input
O : Output
 $\overline{\text{O}}$: Inverting Output
Z : High Impedance

Pin Arrangement

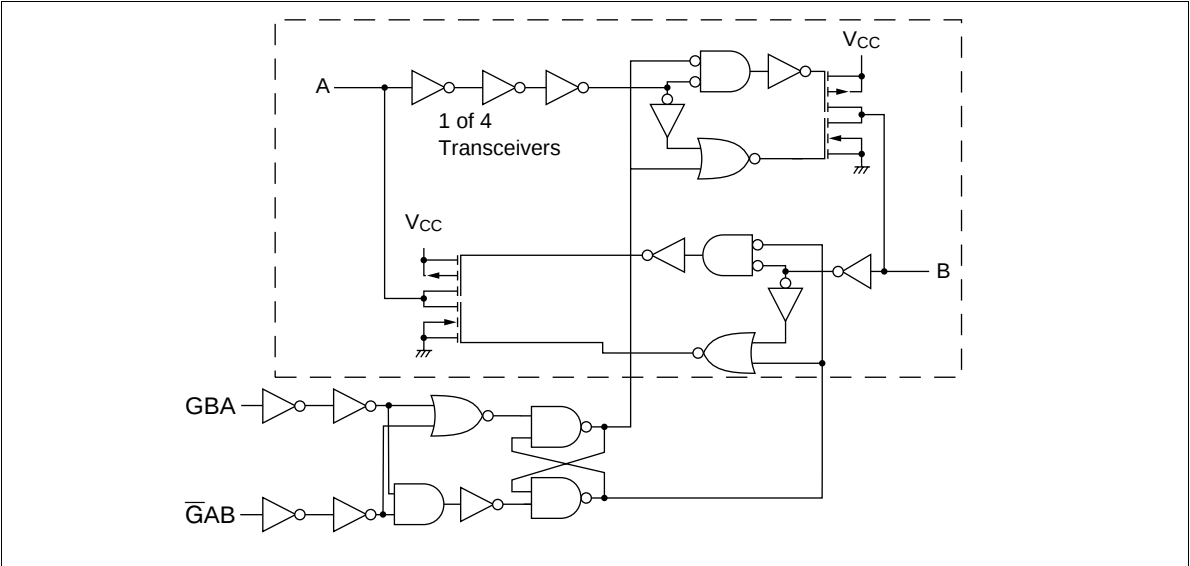


Block Diagram

HD74HCT242



HD74HCT243



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	-0.5 to +7.0	V
Input voltage	V_{IN}	-0.5 to $V_{CC} + 0.5$	V
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
DC current drain per pin	I_{OUT}	± 35	mA
DC current drain per V_{CC} , GND	I_{CC} , I_{GND}	± 75	mA
DC input diode current	I_{IK}	± 20	mA
DC output diode current	I_{OK}	± 20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	-65 to +150	°C

DC Characteristics

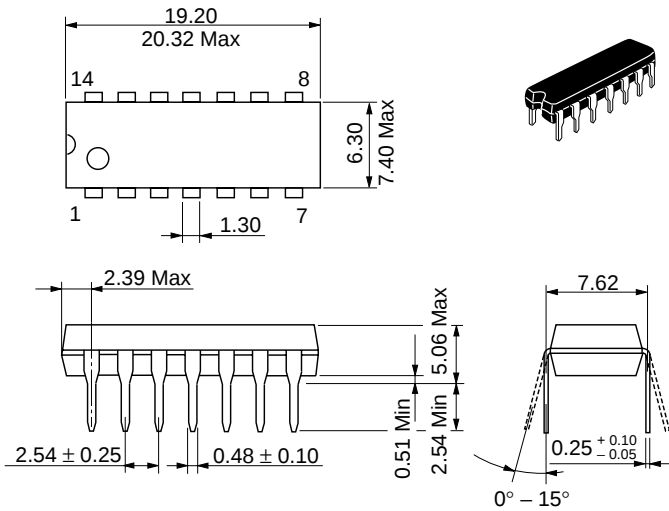
Item	Symbol	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min	Max		V _{CC} (V)	
Input voltage	V _{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5	
	V _{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5	
Output voltage	V _{OH}	4.4	—	—	4.4	—	V	4.5	Vin = V _{IH} or V _{IL} , I _{OH} = -20 μA
		4.18	—	—	4.13	—		4.5	I _{OH} = -6 mA
	V _{OL}	—	—	0.1	—	0.1	V	4.5	Vin = V _{IH} or V _{IL} , I _{OL} = 20 μA
		—	—	0.26	—	0.33		4.5	I _{OL} = 6 mA
Off-state output current	I _{OZ}	—	—	±0.5	—	±5.0	μA	5.5	Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND
Input current	I _{in}	—	—	±0.1	—	±1.0	μA	5.5	Vin = V _{CC} or GND
Quiescent current	I _{CC}	—	—	4.0	—	40	μA	5.5	Vin = V _{CC} or GND, Iout = 0 μA

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min	Max		V _{CC} (V)	
Propagation delay time	t _{PHL}	—	10	18	—	22	ns	4.5	
	t _{PLH}	—	9	18	—	22		4.5	
Output enable time	t _{ZL}	—	14	30	—	38	ns	4.5	
	t _{ZH}	—	13	30	—	38		4.5	
Output disable time	t _{LZ}	—	16	30	—	38	ns	4.5	
	t _{HZ}	—	17	30	—	38		4.5	
Output rise/fall time	t _{TLH} t _{THL}	—	4	12	—	15	ns	4.5	
Input capacitance	C _{in}	—	5	10	—	10	pF	—	

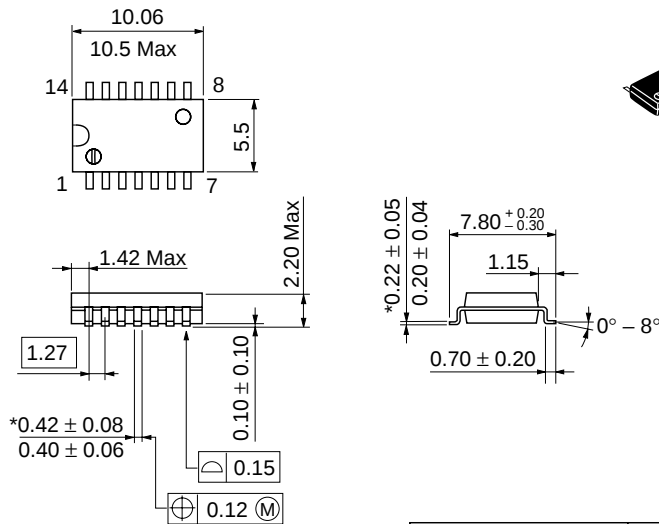
Package Dimensions

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.97 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.23 g

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