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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74HC194

4-bit Bidirectional Universal Shift Register

ADE-205-466 (Z)
1st. Edition
Sep. 2000

Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation: parallel (broadside) load, shift right (in the direction Q_A toware Q_D); shift left; inhibit clock (do nothing).

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1, high. The data are loaded into their respective flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift left serial input. Clocking of the flip-flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the clock input is high.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 12 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max

Function Table

Operating Mode	Inputs										Outputs			
		Mode			Serial		Parallel							
	Clear	S_1	S_0	Clock	Shift Left	Shift Right	A	B	C	D	Q_A	Q_B	Q_C	Q_D
Clear	L	X	X	X	X	X	X	X	X	X	L	L	L	L
Parallel load	H	H	H	↑	X	X	a	b	c	d	a	b	c	d
Shift right	H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
	H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
Shift left	H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
	H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
Hold	H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
	H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
	H	X	X	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H : high level (Steady state)

L : low level (Steady state)

X : don't care

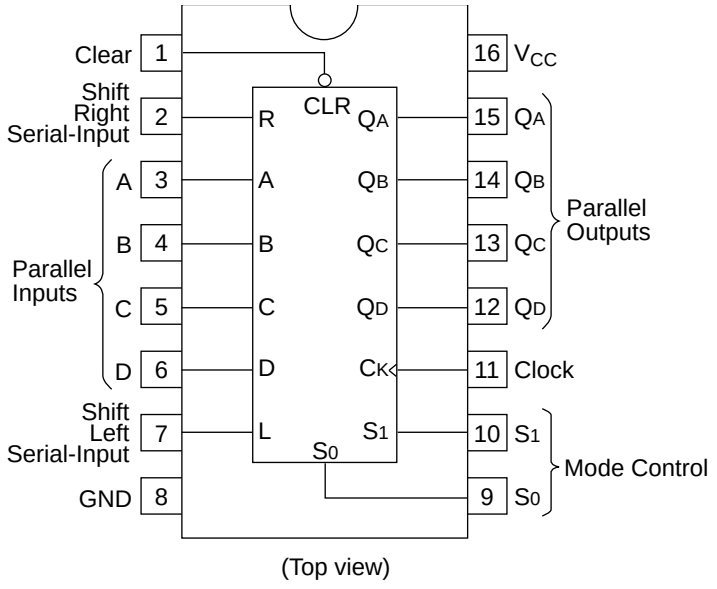
↑ : transition from low to high level.

a, b, c, d : the level of steady-state input at inputs A, B, C or D respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} : the level of Q_A, Q_B, Q_C or Q_D respectively, before the indicated steady-state input conditions were established.

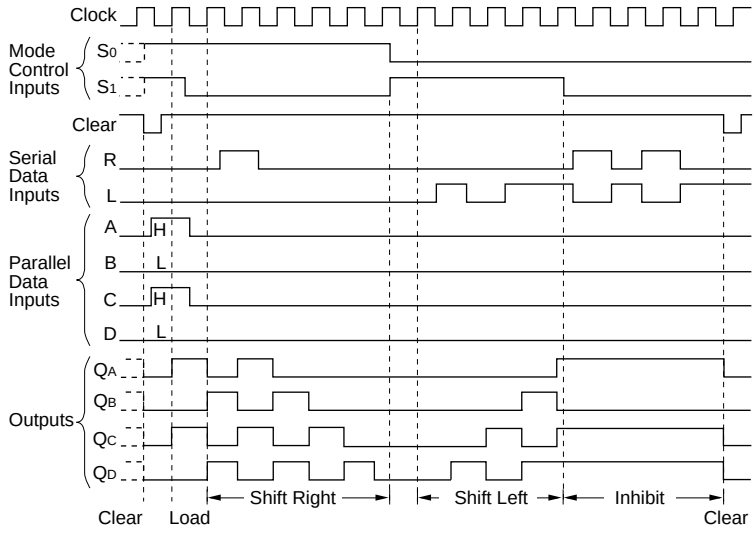
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} : the level of Q_A, Q_B, Q_C or Q_D respectively before the most recent ↑ transition of the clock.

Pin Arrangement

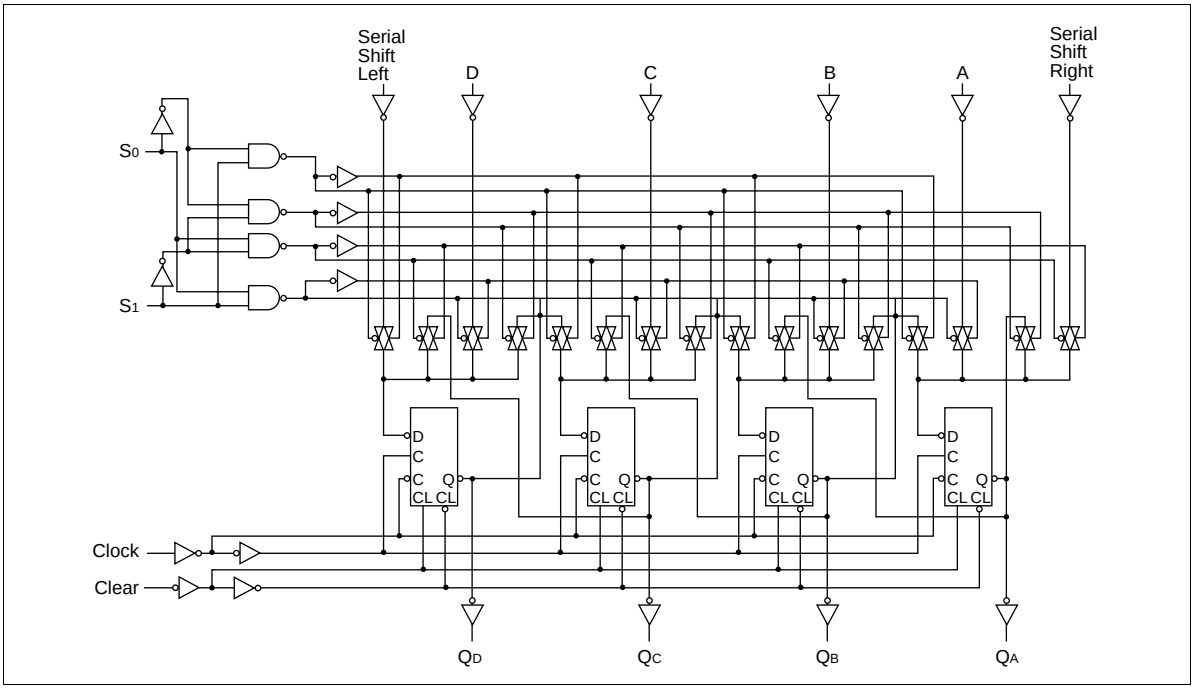


(Top view)

Timing Diagram



Logic Diagram



DC Characteristics

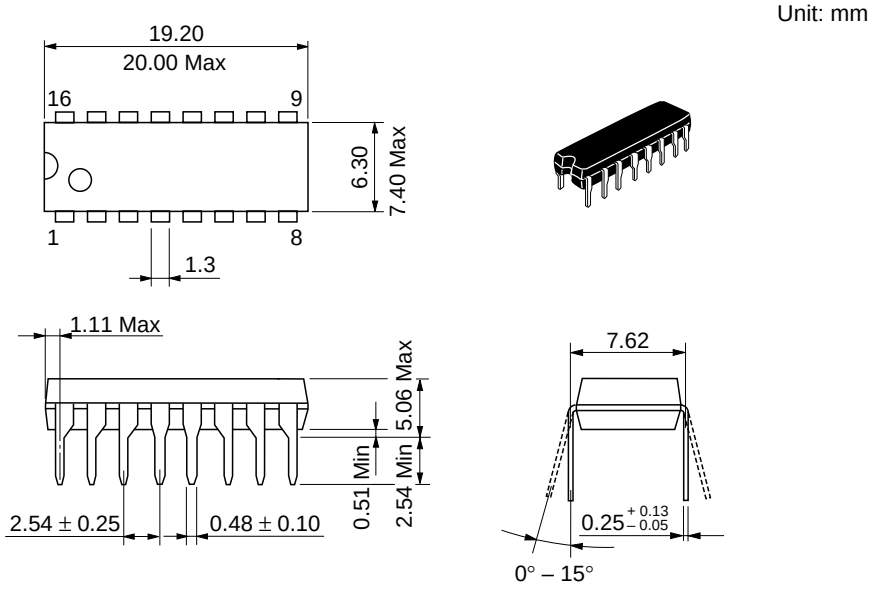
Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V_{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—		I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33		I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA

AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	6	—	5	ns	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t_{PHL}	2.0	—	—	140	—	175	ns	Clock to Q
		4.5	—	12	28	—	35		
		6.0	—	—	24	—	30		
	t_{PLH}	2.0	—	—	140	—	175	ns	
		4.5	—	12	28	—	35		
		6.0	—	—	24	—	30		
	t_{PHL}	2.0	—	—	150	—	190	ns	Clear to Q
		4.5	—	13	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock or Clear
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	A, B, C or D to Clock
		4.5	20	7	—	25	—		
		6.0	17	—	—	21	—		
		2.0	150	—	—	187	—	ns	Mode controls to Clock
		4.5	30	17	—	37	—		
		6.0	25	—	—	31	—		
Hold time	t_h	2.0	0	—	—	0	—	ns	Any input
		4.5	0	–4	—	0	—		
		6.0	0	—	—	0	—		
Removal time	t_{rem}	2.0	25	—	—	31	—	ns	Clear inactive to Clock
		4.5	5	1	—	6	—		
		6.0	4	—	—	5	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	
	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	—	5	10	—	10	pF	

Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

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