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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74AC373/HD74ACT373

Octal Transparent Latch with 3-State Output

ADE-205-394 (Z)
1st. Edition
Sep. 2000

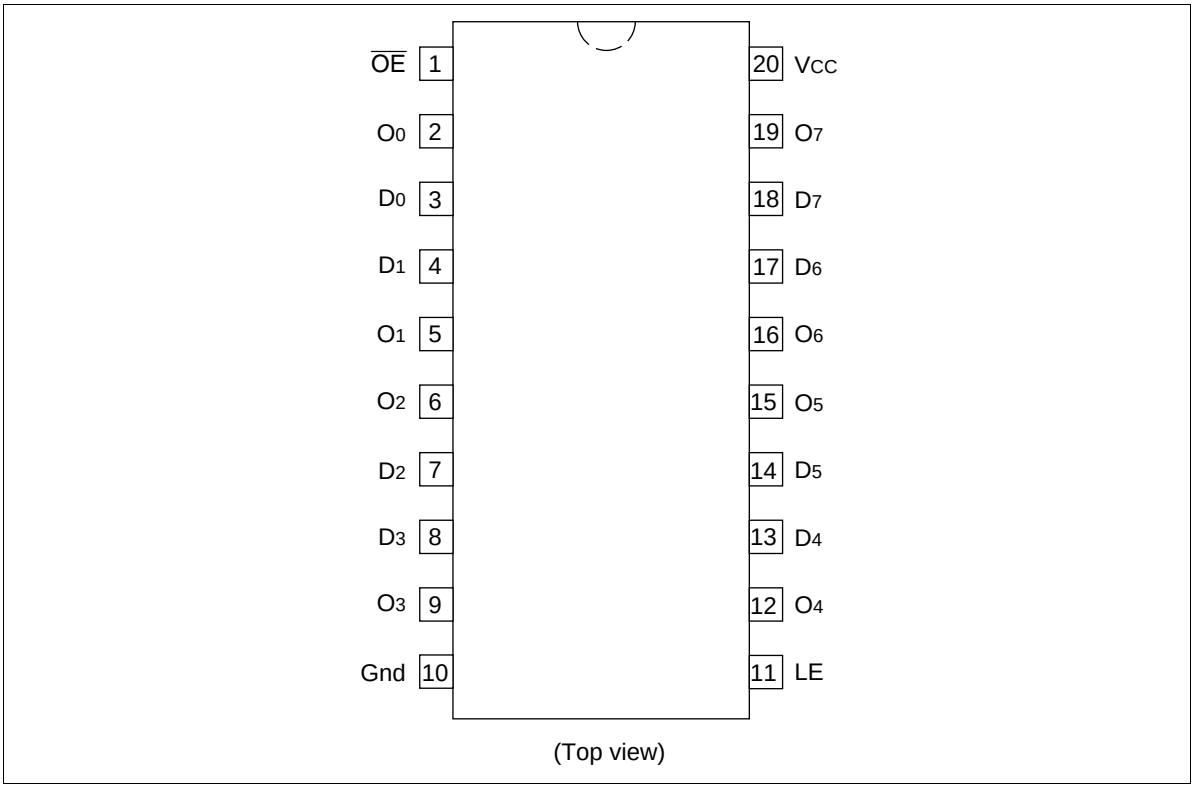
Description Diagram

The HD74AC373/HD74ACT373 consists of eight latches with 3-state outputs from bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is High. When LE is Low, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High, the bus output is in the high impedance state.

Features

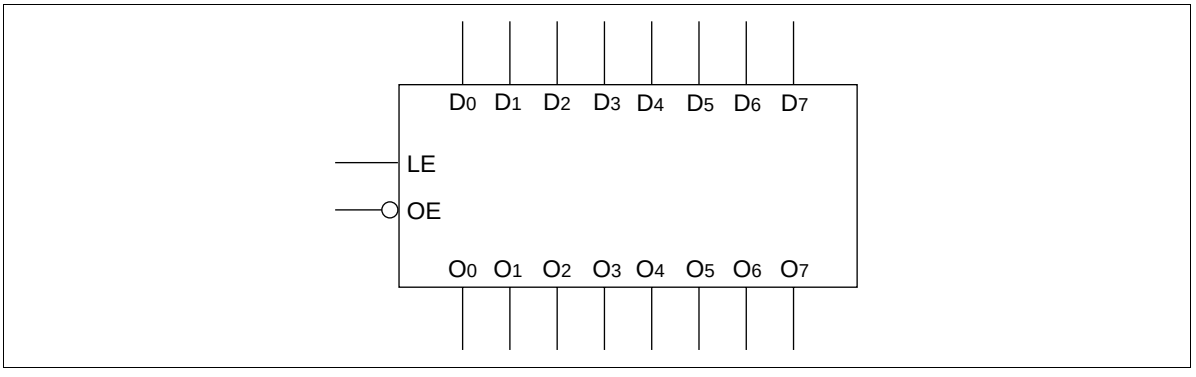
- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- HD74AC373 has TTL-Compatible Inputs

Pin Arrangement



(Top view)

Logic Symbol



Pin Names

$D_0 – D_7$	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
$O_0 – O_7$	3-State Latch Outputs

Truth Table

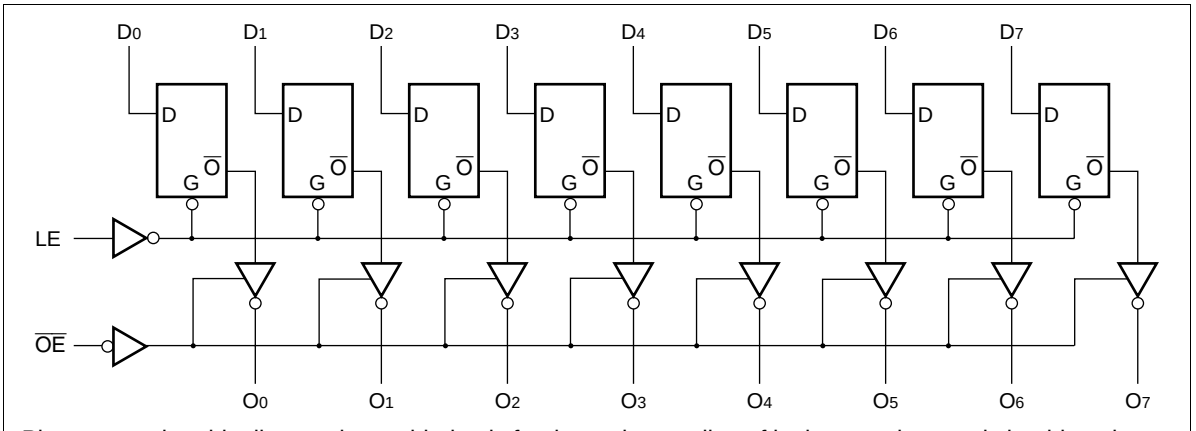
Inputs			Outputs
$\overline{OE}$	LE	D_n	O_n
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	O_0

H : High Voltage Level
L : Low Voltage Level
Z : High Impedance
X : Immaterial
O_0 : Previous O_0 before Low-to-High Transition of Clock

Functional Description

The HD74AC373/HD74ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is High, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is Low, the latches store the information that was present on the D inputs setup time proceding the High-to-Low transition of LE. The 3-state standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is Low, the standard outputs are in the 2-state mode. When $\overline{OE}$ is High, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = Worst case
Maximum quiescent supply current	I_{CC}	8.0	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = 25°C
Maximum I_{CC}/input (HD74ACT373)	I_{CCT}	1.5	mA	V_{IN} = V_{CC} – 2.1 V, V_{CC} = 5.5 V, Ta = Worst case

AC Characteristics: HD74AC373

			Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		
Item	**Symbol**	**V_{CC} (V)*[1]**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
Propagation delay	t_{PLH}	3.3	1.0	10.0	13.5	1.0	15.0	ns
D_n to O_n		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay	t_{PHL}	3.3	1.0	9.5	13.0	1.0	14.5	ns
D_n to O_n		5.0	1.0	7.0	9.5	1.0	10.5	
Propagation delay	t_{PLH}	3.3	1.0	10.0	13.5	1.0	15.0	ns
LE to O_n		5.0	1.0	7.5	9.5	1.0	10.5	
Propagation delay	t_{PHL}	3.3	1.0	9.5	12.5	1.0	14.0	ns
LE to O_n		5.0	1.0	7.0	9.5	1.0	10.5	
Output enable time	t_{ZH}	3.3	1.0	9.0	11.5	1.0	13.0	ns
		5.0	1.0	7.0	8.5	1.0	9.5	
Output enable time	t_{ZL}	3.3	1.0	8.5	11.5	1.0	13.0	ns
		5.0	1.0	6.5	8.5	1.0	9.5	
Output disable time	t_{HZ}	3.3	1.0	10.0	12.5	1.0	14.5	ns
		5.0	1.0	8.0	11.0	1.0	12.5	
Output disable time	t_{LZ}	3.3	1.0	8.0	11.5	1.0	12.5	ns
		5.0	1.0	6.5	8.5	1.0	10.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74AC373

			Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		
Item	**Symbol**	**V_{CC} (V)*[1]**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**
Propagation delay D_n to O_n	t_{PLH}	5.0	1.0	8.5	10.0	1.0	11.5	ns
Propagation delay D_n to O_n	t_{PHL}	5.0	1.0	8.0	10.0	1.0	11.5	ns
Propagation delay LE to O_n	t_{PLH}	5.0	1.0	8.5	11.0	1.0	11.5	ns
Propagation delay LE to O_n	t_{PHL}	5.0	1.0	8.0	10.0	1.0	11.5	ns
Output enable time	t_{ZH}	5.0	1.0	8.0	9.5	1.0	10.5	ns
Output enable time	t_{ZL}	5.0	1.0	7.5	9.0	1.0	10.5	ns
Output disable time	t_{HZ}	5.0	1.0	9.0	11.0	1.0	12.5	ns
Output disable time	t_{LZ}	5.0	1.0	7.5	8.5	1.0	10.0	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC373

			Ta = +25°C C_L = 50 pF		Ta = –40°C to +85°C C_L = 50 pF	
Item	**Symbol**	**V_{CC} (V)*[1]**	**Typ**	**Guaranteed Minimum**		**Unit**
Setup time, HIGH or LOW	t_{su}	3.3	3.5	5.5	6.0	ns
D_n to LE		5.0	2.0	4.0	4.5	
Hold time, HIGH or LOW	t_h	3.3	–3.0	0.0	0.0	ns
D_n to LE		5.0	–1.5	0.0	0.0	
LE pulse width, HIGH	t_w	3.3	4.0	5.5	6.0	ns
		5.0	2.0	4.0	4.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT373

			Ta = +25°C C_L = 50 pF		Ta = –40°C to +85°C C_L = 50 pF	
Item	**Symbol**	**V_{CC} (V)*[1]**	**Typ**	**Guaranteed Minimum**		**Unit**
Setup time, HIGH or LOW D_n to LE	t_{su}	5.0	3.0	7.0	8.0	ns
Hold time, HIGH or LOW D_n to LE	t_h	5.0	0.0	0.0	1.0	ns
LE pulse width, HIGH	t_w	5.0	2.0	7.0	8.0	ns

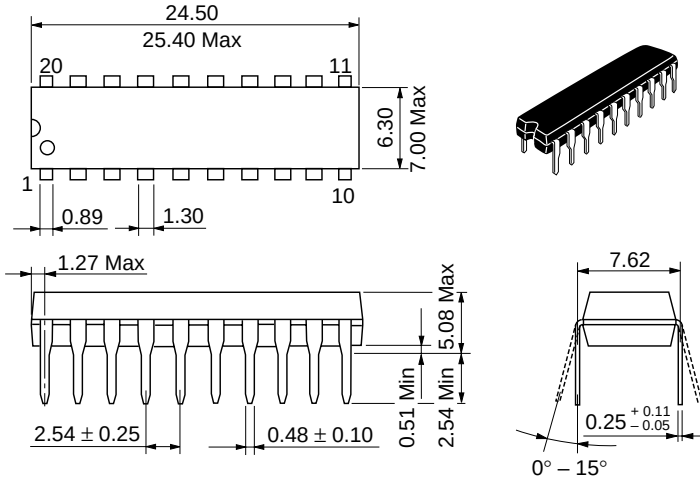
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	**Symbol**	**Typ**	**Unit**	**Condition**
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	40.0	pF	V_{CC} = 5.0 V

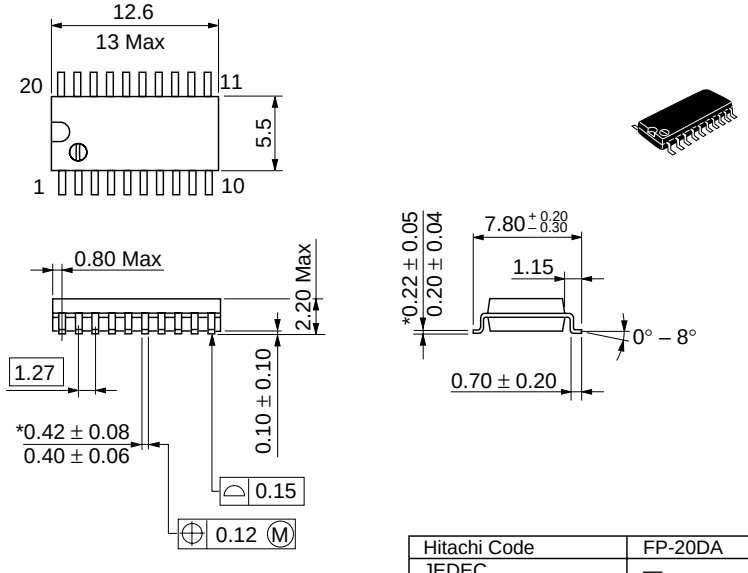
Package Dimensions

Unit: mm



Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Mass (reference value)	1.26 g

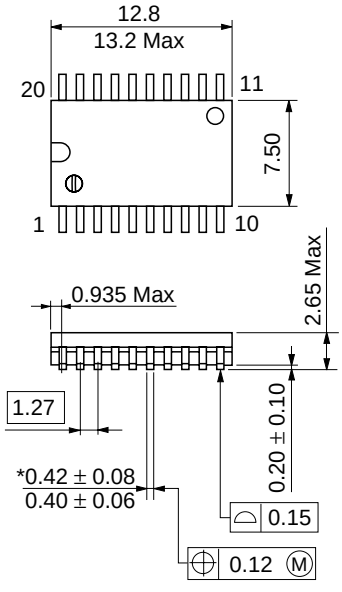
Unit: mm

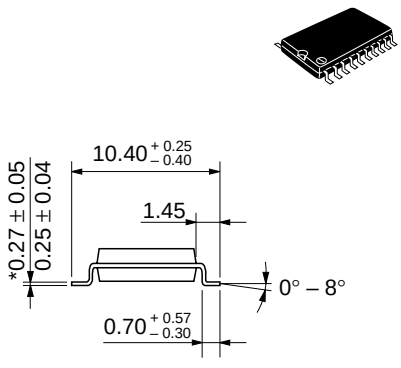


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.31 g

Unit: mm

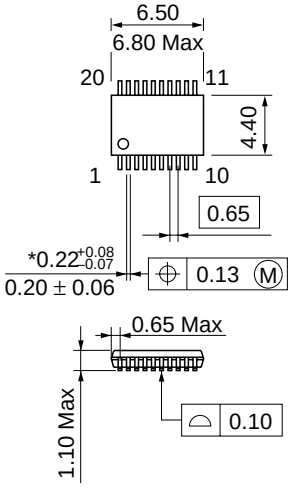


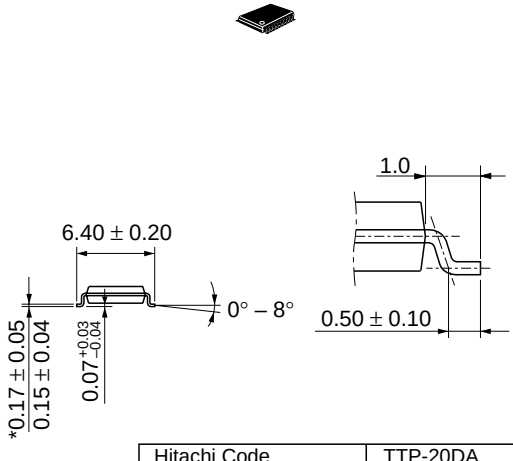


*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.52 g

Unit: mm





*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.07 g

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