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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HD74AC123A

Dual Retriggerable Resettable Multivibrator



ADE-205-365 (Z)

1st. Edition

Sep. 2000

Description

Each half of the HD74AC123A features retriggerable capability, complementary dc level triggering and overriding Direct Clear. When a circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per the Truth Table) will cause the delay period to start again, without disturbing the outputs. By repeating this process, the output pulse period (Q High, $\overline{Q}$ Low) can be made as long as desired. Alternatively, a delay period can be terminated at any time by a Low signal on $\overline{C}_D$, which also inhibits triggering. An internal connection from $\overline{C}_D$ to the input gate makes it possible to trigger the circuit by a positive-going signal on $\overline{C}_D$, as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows.

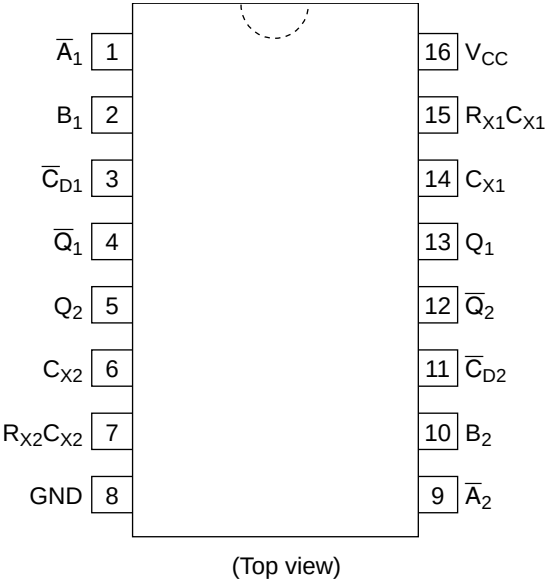
Where t_w is in ns, R_x is in $k\Omega$ and C_x is in pF.

$$t_w = R_x C_x$$

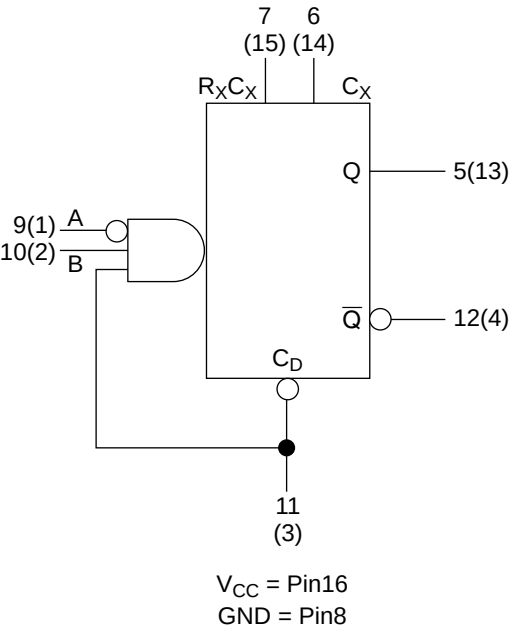
Feature

- Outputs Source/Sink 24 mA

Pin Arrangement



Logic Symbol



Pin Names

- $\overline{A}_1, \overline{A}_2$

Trigger Inputs (Active Falling Edge)
- B_1, B_2

Trigger Inputs (Active Rising Edge)
- $\overline{C}_{D1}, \overline{C}_{D2}$

Direct Clear Inputs (Active Low)
- Q_1, Q_2

Positive Pulse Outputs
- $\overline{Q}_1, \overline{Q}_2$

Negative Pulse Outputs

Triggering Truth Table

Inputs			
A	B	$\overline{C}_D$	Response
X	X	L	No trigger
	L	X	No trigger
	H	H	Trigger
H		X	No trigger
L		H	Trigger
L	H		Trigger
H : High Voltage Level			
L : Low Voltage Level			
X : Immaterial			
 : Low-to-High Transition			
 : High-to-Low Transition			

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	220	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	130	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$, $T_a = 25^\circ C$

HD74AC123A

AC Characteristics: HD74AC123A

Item	Symbol	V_{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit	Condition
			Min	Typ	Max	Min	Max		
Propagation delay $\bar{A}$ or B to Q	t_{PLH}	3.3	1.0	—	19.0	1.0	22.0	ns	Cext = 0 pF
		5.0	1.0	—	15.0	1.0	17.0		Rest = 5 kΩ
Propagation delay $\bar{A}$ or B to $\bar{Q}$	t_{PHL}	3.3	1.0	—	19.0	1.0	22.0	ns	
		5.0	1.0	—	15.0	1.0	17.0		
Propagation delay $\bar{C}_{Dn}$ to $\bar{Q}$	t_{PLH}	3.3	1.0	—	15.0	1.0	18.0	ns	
		5.0	1.0	—	12.0	1.0	13.5		
Propagation delay $\bar{C}_{Dn}$ to Q	t_{PHL}	3.3	1.0	—	15.0	1.0	18.0	ns	
		5.0	1.0	—	12.0	1.0	13.5		

Note: 1. Voltage Range 3.3 is 3.3 V $\pm$ 0.3 V
Voltage Range 5.0 is 5.0 V $\pm$ 0.5 V

AC Operating Requirements: HD74AC123A

Item	Symbol	V_{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = -40 to +85°C C _L = 50 pF		Unit	Condition
			Typ	Guaranteed Minimum				
Pulse width	t_w	3.3	—	5.0	7.0		ns	Cext = 0 pF
$\bar{A}$ or B or $\bar{C}_{Dn}$		5.0	—	4.5	5.0			Rext = 5 kΩ
Recovery time	t_{rec}	3.3	—	2.0	2.0		ns	
$\bar{C}_{Dn}$ to $\bar{A}$ or B		5.0	—	2.0	2.0			

Note: 1. Voltage Range 3.3 is 3.3 V $\pm$ 0.3 V
Voltage Range 5.0 is 5.0 V $\pm$ 0.5 V

Item	Symbol	V_{CC} (V)*1	Ta = +25°C CL = 50 pF			Ta = -40°C to +85°C CL = 50 pF		Unit	Condition
			Min	Typ	Max	Min	Max		
Output pulse width	TWQ	3.3	—	—	—	—	—	ms	Cext = 0.1 μF
		5.0	0.90	—	1.10	0.85	1.15		Rext = 10 kΩ
Minimum output pulse width	TWQ(min)	3.3	190	—	350	170	380	ns	Cext = 28 pF
		5.0	160	—	300	140	330		Rext = 2 kΩ

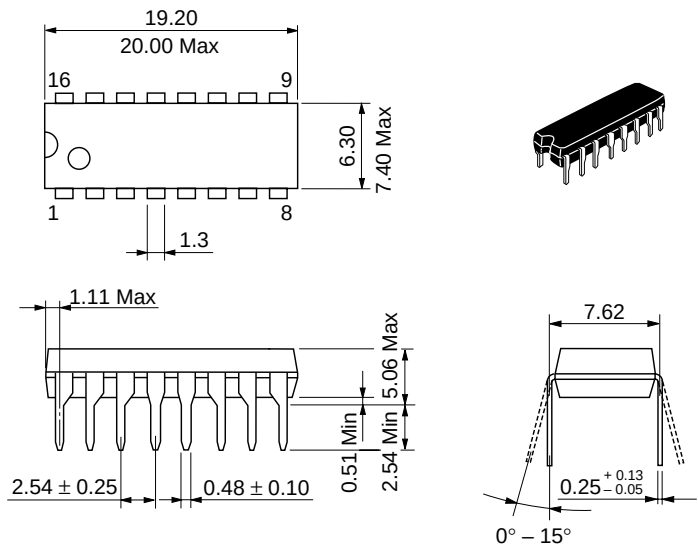
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V

Voltage Range 5.0 is 5.0 V ± 0.5 V

Cext and Rext should be connected as close to the IC terminals as possible, in order to prevent malfunction.

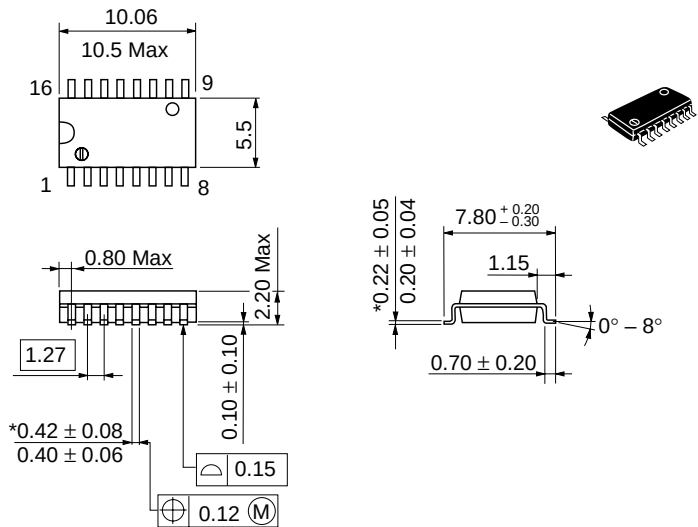
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

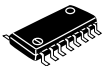
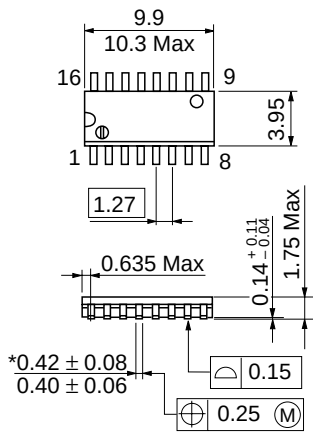
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

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