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## 8-bit Shift Registers with 3-state Outputs



ADE-205-281 (Z)

1st Edition April 1999

#### **Description**

This device each contains an 8-bit serial-in, parallel-out shift registers that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and the storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

#### **Features**

- $V_{cc} = 2.0 \text{ V}$  to 5.5 V operation
- All inputs  $V_{IH}$  (Max.) = 5.5 V (@ $V_{CC}$  = 0 V to 5.5 V)
- All outputs  $V_o$  (Max.) = 5.5 V (@ $V_{cc}$  = 0 V)
- Typical  $V_{OL}$  ground bounce < 0.8 V (@ $V_{CC}$  = 3.3 V, Ta = 25°C)
- Typical  $V_{OH}$  undershoot > 2.3 V (@ $V_{CC}$  = 3.3 V, Ta = 25°C)
- Output current  $\pm 6 \text{ mA}$  (@V<sub>cc</sub> = 3.0 V to 3.6 V),  $\pm 12 \text{ mA}$  (@V<sub>cc</sub> = 4.5 V to 5.5 V)

#### **Function Table**

#### Inputs

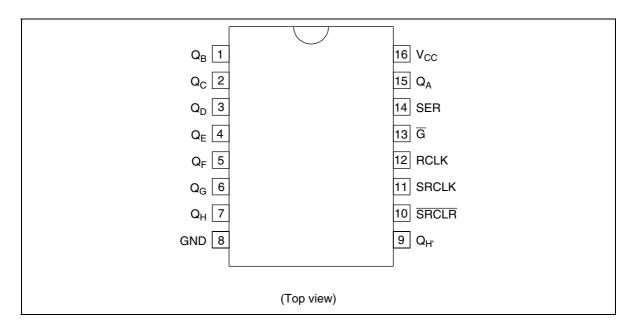
SER	SRCLK	SRCLR	RCLK	G	Function
Х	Х	Х	Х	Н	Force outputs into high-impedance state
Х	Х	Х	Х	L	Enable paralle output
Х	Χ	L	Χ	Χ	Reset shift register
L	<b>↑</b>	Н	Χ	Χ	Shift data into shift register
Н	<b>↑</b>	Н	Х	Х	Shift data into shift register
Х	$\downarrow$	Н	Х	Х	Shift register remains unchanged
Х	Х	Х	<b>↑</b>	Х	Transfer shift register contents to latch register
Х	Х	Х	$\downarrow$	Х	Latch register remains unchanged

Note: H: High level

L: Low level X: Immaterial

↑: Low to high transition↓: High to low transition

#### **Pin Arrangement**



#### **Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V <sub>cc</sub>	-0.5 to 7.0	V	
Input voltage range*1	V,	-0.5 to 7.0	V	
Output voltage range*1,2	V <sub>o</sub>	$-0.5$ to $V_{cc}$ + $0.5$	V	Output: H or L
		-0.5 to 7.0	_	Output: Z or V <sub>cc</sub> : OFF
Input clamp current	I <sub>IK</sub>	-20	mA	V <sub>1</sub> < 0
Output clamp current	I <sub>ok</sub>	±50	mA	$V_o < 0 \text{ or } V_o > V_{cc}$
Continuous output current	I <sub>o</sub>	±25	mA	$V_{o} = 0 \text{ to } V_{cc}$
Continuous current through $V_{cc}$ or GND	$I_{\rm cc}$ or $I_{\rm GND}$	±70	mA	
Maximum power dissipation at Ta = 25°C (in still air)* <sup>3</sup>	P <sub>T</sub>	785	mW	SOP
		500	=	TSSOP
Storage temperature	Tstg	-65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

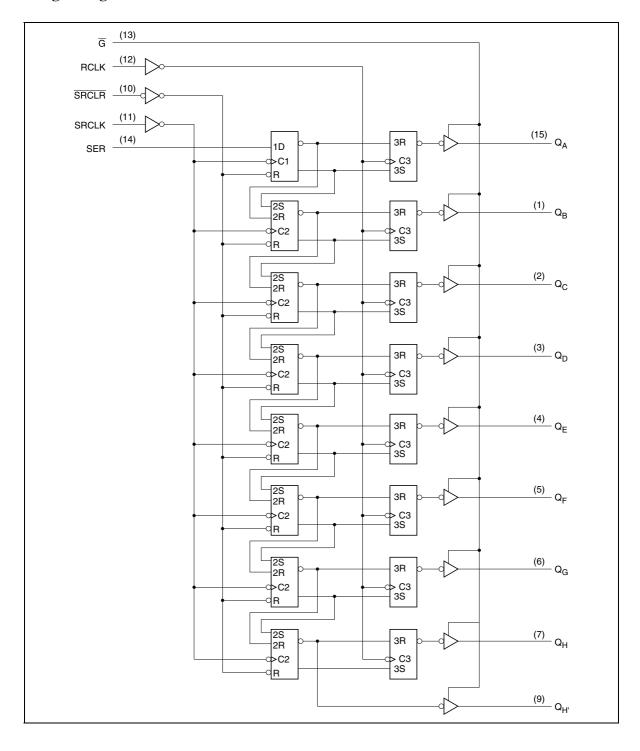
- 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 2. This value is limited to 5.5 V maximum.
- 3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

## **Recommended Operating Conditions**

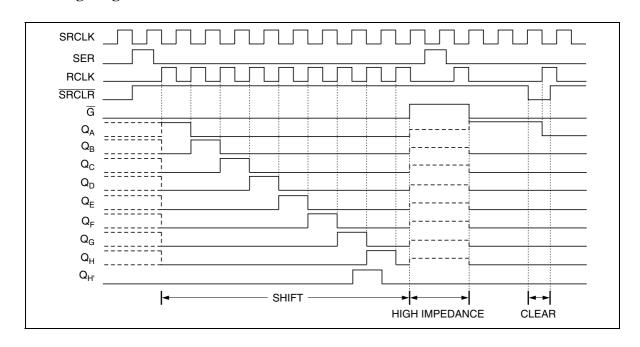
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V <sub>cc</sub>	2.0	5.5	V	
Input voltage range	V <sub>i</sub>	0	5.5	V	
Output voltage range	V <sub>o</sub>	0	V <sub>cc</sub>	V	H or L
		0	5.5		High impedance state
Output current	I <sub>OH</sub>	_	-50	μΑ	V <sub>cc</sub> = 2.0 V
		_	-2	mA	$V_{cc} = 2.3 \text{ to } 2.7 \text{ V}$
		_	-6		$V_{cc} = 3.0 \text{ to } 3.6 \text{ V}$
		_	-12		$V_{cc} = 4.5 \text{ to } 5.5 \text{ V}$
	I <sub>OL</sub>	_	50	μΑ	V <sub>cc</sub> = 2.0 V
		_	2	mA	$V_{cc} = 2.3 \text{ to } 2.7 \text{ V}$
		_	6		$V_{cc} = 3.0 \text{ to } 3.6 \text{ V}$
		_	12		$V_{cc} = 4.5 \text{ to } 5.5 \text{ V}$
Input transition rise or fall rate	Δt /Δν	0	200	ns/V	$V_{cc} = 2.3 \text{ to } 2.7 \text{ V}$
		0	100		$V_{cc} = 3.0 \text{ to } 3.6 \text{ V}$
		0	20		$V_{cc} = 4.5 \text{ to } 5.5 \text{ V}$
Operating free-air temperature	Та	-40	85	°C	

Note: Unused or floating inputs must be held high or low.

#### Logic Diagram



## **Timing Diagram**



#### **DC Electrical Characteristics**

 $Ta = -40 \text{ to } 85^{\circ}\text{C}$ 

Item	Symbol	V <sub>cc</sub> (V)*	Min	Тур	Max	Unit	Test Conditions
Input voltage	V <sub>IH</sub>	2.0	1.5	_	_	٧	
		2.3 to 2.7	$V_{cc} \times 0.7$	_	_	_	
		3.0 to 3.6	$V_{cc} \times 0.7$	_	_		
		4.5 to 5.5	$V_{cc} \times 0.7$	_	_	_	
	V <sub>IL</sub>	2.0	_	_	0.5	_	
		2.3 to 2.7	_	_	$V_{\text{cc}}\! imes\!0.3$	_	
		3.0 to 3.6	_	_	$V_{\text{cc}} \times 0.3$	_	
		4.5 to 5.5	_	_	$V_{\text{cc}}\! imes\!0.3$		
Output voltage	$V_{\text{OH}}$	Min to Max	V <sub>cc</sub> – 0.1	_	_	V	I <sub>OH</sub> = -50 μA
		2.3	2.0	_	_	_	I <sub>OH</sub> = -2 mA
		3.0	2.48	_	_	_	I <sub>OH</sub> = -6 mA
		4.5	3.8	_	_	_	$I_{OH} = -12 \text{ mA}$
	V <sub>oL</sub>	Min to Max	_	_	0.1	_	I <sub>oL</sub> = 50 μA
		2.3	_	_	0.4		I <sub>OL</sub> = 2 mA
		3.0	_	_	0.44		I <sub>OL</sub> = 6 mA
		4.5	_	_	0.55	_	I <sub>OL</sub> = 12 mA
Input current	I <sub>IN</sub>	0 to 5.5	_	_	±1	μΑ	V <sub>IN</sub> = 5.5 V or GND
Off-state output current	l <sub>oz</sub>	5.5	_	_	±5	μΑ	$V_o = V_{cc}$ or GND
Quiescent supply current	I <sub>cc</sub>	5.5	_	_	20	μА	$V_{IN} = V_{CC}$ or GND, $I_{O} = 0$
Output leakage current	l <sub>OFF</sub>	0	_	_	5	μА	$V_{_{\rm I}}$ or $V_{_{\rm O}}$ = 0 to 5.5 V
Input capacitance	C <sub>IN</sub>	3.3	_	3.5	_	рF	$V_{_{I}} = V_{_{CC}}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

## **Switching Characteristics**

 $V_{cc} = 2.5 \pm 0.2 \text{ V}$ 

		Ta = 2	5°C		Ta = -4	40 to 85°C				
Item	Symbol	Min	Тур	Max	Min	Max	Unit	Test Conditions	FROM (Input)	TO (Output)
Maximum	$\mathbf{f}_{\text{max}}$	65	80	_	45	_	MHz	C <sub>∟</sub> = 15 pF		
clock frequency		60	70	_	40	_	-	C <sub>L</sub> = 50 pF	_	
Propagation	$t_{_{\mathrm{PLH}}}/t_{_{\mathrm{PHL}}}$	_	11.6	16.4	1.0	19.5	ns	C <sub>L</sub> = 15 pF	SRCLK	Q <sub>H</sub> '
delay time		_	14.8	19.4	1.0	22.5	=	C <sub>L</sub> = 50 pF		
		_	10.5	15.3	1.0	18.0	=	C <sub>L</sub> = 15 pF	RCLK	$Q_A - Q_H$
		_	13.7	18.3	1.0	21.0	=	C <sub>L</sub> = 50 pF	<del></del>	
	t <sub>PHL</sub>	_	11.2	16.2	1.0	18.2	=	C <sub>L</sub> = 15 pF	SRCLK	Q <sub>H</sub> '
		_	14.4	19.2	1.0	21.2	=	C <sub>L</sub> = 50 pF	<del></del>	
Enable time	t <sub>zH</sub>	_	10.3	14.8	1.0	17.5	ns	C <sub>L</sub> = 15 pF	G	$Q_A - Q_H$
	$\mathbf{t}_{_{\mathrm{ZL}}}$	_	12.2	17.7	1.0	20.5	=	C <sub>L</sub> = 50 pF		
Disable time	t <sub>HZ</sub>	_	7.6	11.5	1.0	13.5	ns	C <sub>L</sub> = 15 pF		
	$\mathbf{t}_{\scriptscriptstyle{LZ}}$	_	14.4	18.2	1.0	19.2	=	C <sub>L</sub> = 50 pF	<del></del>	
Setup time	t <sub>su</sub>	5.5	_	_	5.5	_	ns		SER befo	ore SRCLK ↑
		10.0	_	_	10.5	_	_		SRCLK 1	before
		10.0	_	_	11.0	_	_		SRCLR I	ow before
		5.0	_	_	5.0	_	_		SRCLR h (inactive) SRCLK 1	before
Hold time	t <sub>h</sub>	2.0	_	_	2.0	_	ns		SER afte	r SRCLK ↑
		0.5	_	_	0.5	_	_		SRCLK 1	after
		0.5	_	_	0.5	_	-		SRCLR I	ow after
Pulse width	t <sub>w</sub>	7.0	_	_	7.5	_	ns		RCLK hig	h or low
		7.0	_	_	7.5	_	_		SRCLK h	igh or low
		6.0	_	_	6.5	_	=		SRCLR I	OW

 $V_{cc} = 3.3 \pm 0.3 \text{ V}$ 

		Ta =	25°C		Ta = -	40 to 85°C				
Item	Symbol	Min	Тур	Max	Min	Max	Unit	Test Conditions	FROM (Input)	TO (Output)
Maximum	f <sub>max</sub>	80	150	_	70	_	MHz	C <sub>L</sub> = 15 pF		
clock frequency		55	130	_	50	_	_	C <sub>L</sub> = 50 pF	_	
Propagation	$t_{_{\mathrm{PLH}}}/t_{_{\mathrm{PHL}}}$	_	8.8	13.0	1.0	15.0	ns	C <sub>L</sub> = 15 pF	SRCLK	Q <sub>H</sub> '
delay time		_	11.3	16.5	1.0	18.5	=	C <sub>L</sub> = 50 pF	_	
		_	7.7	11.9	1.0	13.5	_	C <sub>L</sub> = 15 pF	RCLK	$\mathbf{Q}_{\scriptscriptstyle{A}} - \mathbf{Q}_{\scriptscriptstyle{H}}$
		_	10.2	15.4	1.0	17.0	_	C <sub>L</sub> = 50 pF	_	
	t <sub>PHL</sub>	_	8.4	12.8	1.0	13.7		C <sub>L</sub> = 15 pF	SRCLK	Q <sub>H</sub> '
		_	10.9	16.3	1.0	17.2	_	C <sub>L</sub> = 50 pF	_	
Enable time	t <sub>zн</sub>	_	7.5	11.5	1.0	13.5	ns	C <sub>L</sub> = 15 pF	G	$Q_{_{\mathrm{A}}} - Q_{_{\mathrm{H}}}$
	$\mathbf{t}_{_{\mathbf{ZL}}}$	_	9.0	15.0	1.0	17.0	_	C <sub>L</sub> = 50 pF	_	
Disable time	t <sub>HZ</sub>	_	5.9	11.7	1.0	13.5	ns	C <sub>L</sub> = 15 pF	_	
	$\mathbf{t}_{\scriptscriptstyle{LZ}}$	_	12.1	15.7	1.0	16.2	_	C <sub>L</sub> = 50 pF	_	
Setup time	$\mathbf{t}_{_{\mathrm{SU}}}$	3.5	_	_	3.5	_	ns		SER before	SRCLK ↑
		8.0	_	_	8.5	_	_		SRCLK ↑ be	efore RCLK ↑
		8.0	_	_	9.0	_	_		SRCLR low	before RCLK ↑
		3.0	_	_	3.0	_			SRCLR high before SRC	,
Hold time	t <sub>h</sub>	1.5	_	_	1.5	_	ns		SER after S	RCLK ↑
		0.0	_	_	0.0	_	=		SRCLK ↑ af	ter RCLK ↑
		0.0	_	_	0.0	_	=		SRCLR low	after RCLK ↑
Pulse width	t <sub>w</sub>	5.0	_	_	5.0	_	ns		RCLK high	or low
		5.0	_	_	5.0	_	=		SRCLK high	n or low
		5.0	_	_	5.0	_	_		SRCLR low	

## **Switching Characteristics (cont)**

 $V_{cc} = 5.0 \pm 0.5 \text{ V}$ 

		Ta =	25°C		Ta = -	40 to 85°C				
Item	Symbol	Min	Тур	Max	Min	Max	Unit	Test Conditions	FROM (Input)	TO (Output)
Maximum	f <sub>max</sub>	135	185	_	115	_	MHz	C <sub>∟</sub> = 15 pF		
clock frequency		95	155	_	85	_	-	C <sub>L</sub> = 50 pF	-	
Propagation	$t_{\scriptscriptstyle PLH}/t_{\scriptscriptstyle PHL}$	_	6.2	8.2	1.0	9.4	ns	C <sub>L</sub> = 15 pF	SRCLK	Q <sub>H</sub> '
delay time		_	7.7	10.2	1.0	11.4	-	C <sub>L</sub> = 50 pF		
		_	5.4	7.4	1.0	8.5	-	C <sub>L</sub> = 15 pF	RCLK	$Q_{\scriptscriptstyle A} - Q_{\scriptscriptstyle H}$
		_	6.9	9.4	1.0	10.5	-	C <sub>L</sub> = 50 pF	<del>.</del>	
	t <sub>PHL</sub>	_	5.9	8.0	1.0	9.1	-	C <sub>L</sub> = 15 pF	SRCLK	Q <sub>H</sub> '
		_	7.4	10.0	1.0	11.1	-	C <sub>L</sub> = 50 pF	<del>-</del>	
Enable time	t <sub>zH</sub>	_	4.8	8.6	1.0	10.0	ns	C <sub>L</sub> = 15 pF	G	$Q_A - Q_H$
	$\mathbf{t}_{_{\mathrm{ZL}}}$	_	8.3	10.6	1.0	12.0	-	C <sub>L</sub> = 50 pF	<del>.</del>	
Disable time	t <sub>HZ</sub>	_	4.8	8.6	1.0	10.0	ns	C <sub>L</sub> = 15 pF	-	
	$\mathbf{t}_{\scriptscriptstyle{LZ}}$	_	7.6	11.0	1.0	11.0	-	C <sub>L</sub> = 50 pF	-	
Setup time	t <sub>su</sub>	3.0	_	_	3.0	_	ns		SER before	SRCLK 1
		5.0	_	_	5.0	_	-		SRCLK ↑ be	fore RCLK ↑
		5.0	_	_	5.0	_	-		SRCLR low I	oefore RCLK ↑
		2.5	_	_	2.5	_			SRCLR high before SRCL	•
Hold time	t <sub>h</sub>	2.0	_	_	2.0	_	ns		SER after SF	RCLK ↑
		0.0	_	_	0.0	_	-		SRCLK ↑ aft	er RCLK ↑
		0.0	_	_	0.0	_	-		SRCLR low a	after RCLK ↑
Pulse width	t <sub>w</sub>	5.0	_	_	5.0	_	ns		RCLK high o	r low
		5.0	_	_	5.0	_	-		SRCLK high	or low
		5.0		_	5.0	_			SRCLR low	

#### **Output-skew Characteristics**

 $C_L = 50 \text{ pF}$ 

			Ta = 25°C		Ta = -40  to	85°C		
Item	Symbol	$V_{cc} = (V)$	Min	Max	Min	Max	Unit	
Output skew	t <sub>sk (O)</sub>	2.3 to 2.7	_	2.0	_	2.0	ns	
		3.0 to 3.6	_	1.5	_	1.5	-	
		4.5 to 5.5	_	1.0	_	1.0	_	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

#### **Operating Characteristics**

 $C_L = 50 \text{ pF}$ 

			$Ta = 25^{\circ}$	C			
Item	Symbol	$V_{cc} = (V)$	Min	Тур	Max	Unit	<b>Test Conditions</b>
Power dissipation capacitance	$C_{\scriptscriptstylePD}$	3.3	_	32.7	_	pF	f = 10 MHz
		5.0	_	33.1	_		

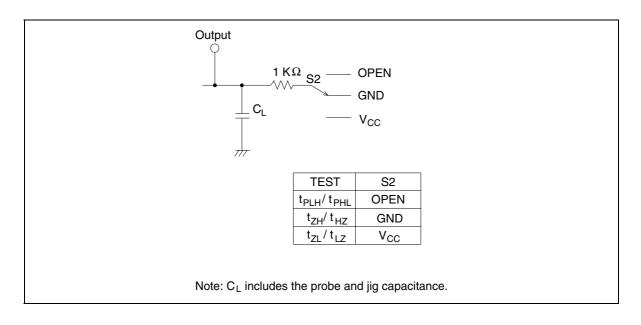
#### **Noise Characteristics**

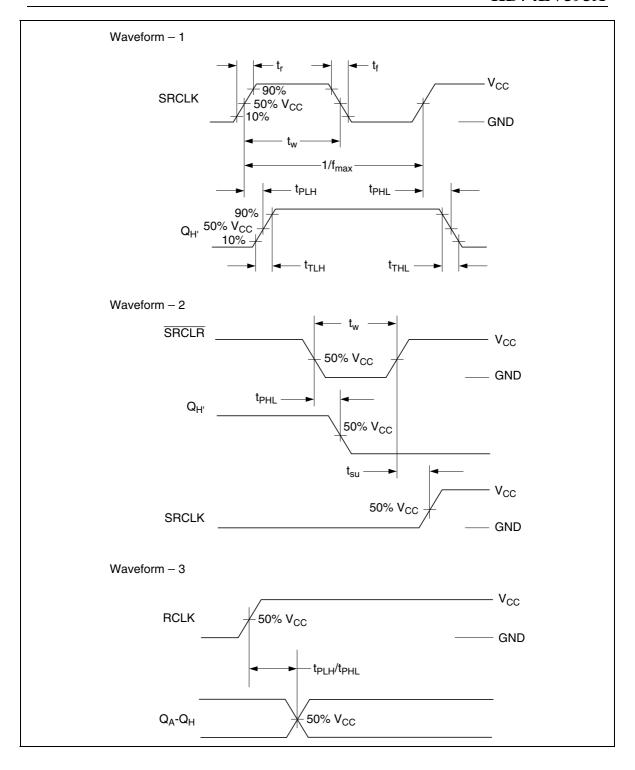
 $C_L = 50 \text{ pF}$ 

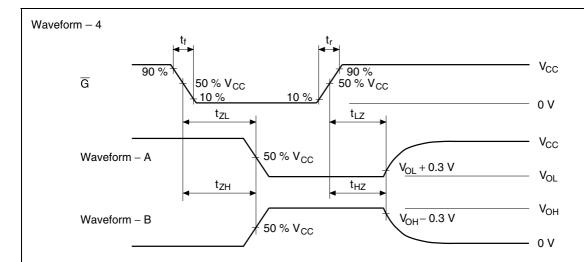
Ta = 25°C

Item	Symbol	$V_{cc} = (V)$	Min	Тур	Max	Unit	<b>Test Conditions</b>
Quiet output, maximum dynamic V <sub>oL</sub>	$V_{_{OL(P)}}$	3.3	_	0.65	0.8	V	
Quiet output, minimum dynamic V <sub>oL</sub>	$V_{OL(V)}$	3.3	_	-0.59	-0.8		
Quiet output, minimum dynamic V <sub>OH</sub>	$V_{_{\mathrm{OH}(V)}}$	3.3	_	2.84	_		
High-level dynamic input voltage	$V_{_{IH\;(D)}}$	3.3	2.31	_	_		
Low-level dynamic inout voltage	V <sub>IL (D)</sub>	3.3	_	_	0.99		

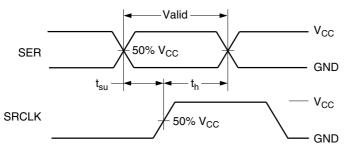
#### **Test Circuit**



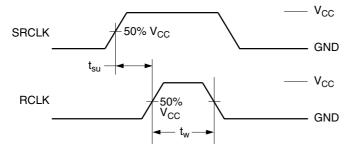




Waveform - 5



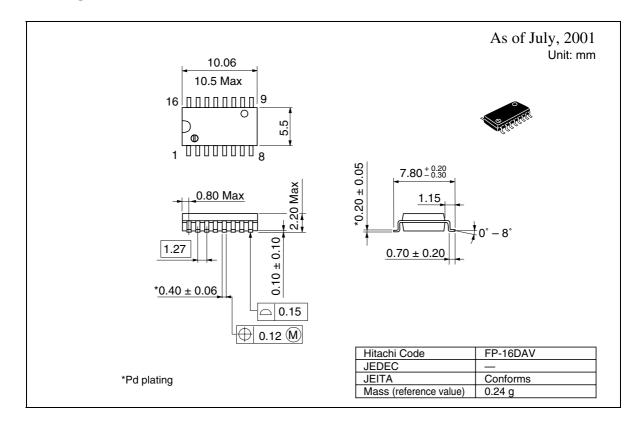
Waveform - 6

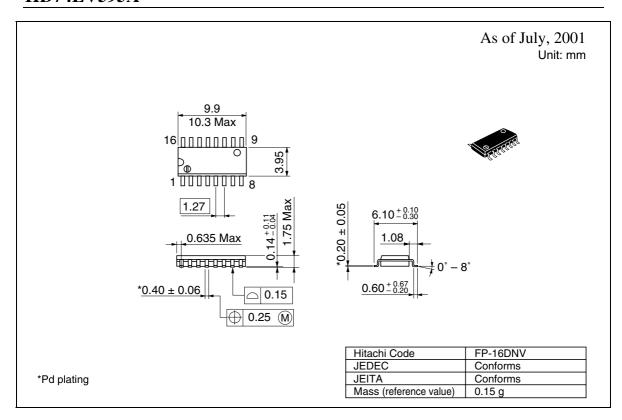


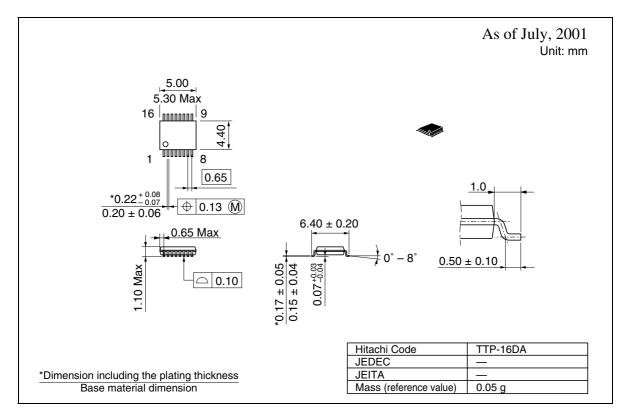
Notes: 1. Input waveform: PRR  $\leq$  1 MHz, Zo = 50  $\Omega$ , t  $\leq$  3 ns, t  $\leq$  3 ns

- 2. Waveform—A is for an output with internal conditions such that the output is low except when disabled by the output control.
- 3. Waveform—B is for an output with internal conditions such that the output is high except when disabled by the output control.
- 4. The output are measured one at a time with one transition per measurement.

#### **Package Dimensions**







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