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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74LV163A

Synchronous 4-bit Binary Counter (Synchronous Clear)



ADE-205-265C (Z)

4th. Edition
Jul. 2001

Description

The HD74LV163A is 4-bit binary counters. All flip flops are clocked simultaneously on the low to high to transition (positive edge) of the clock input waveform. These counters may be preset using the load input. Presetting of all four flip flops is synchronous to the rising edge of clock. When load is held low counting is disabled and the data on the A, B, C and D inputs is loaded into the counter on the rising edge clock. If the load input is taken high before the positive edge of clock the count operation will be unaffected.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

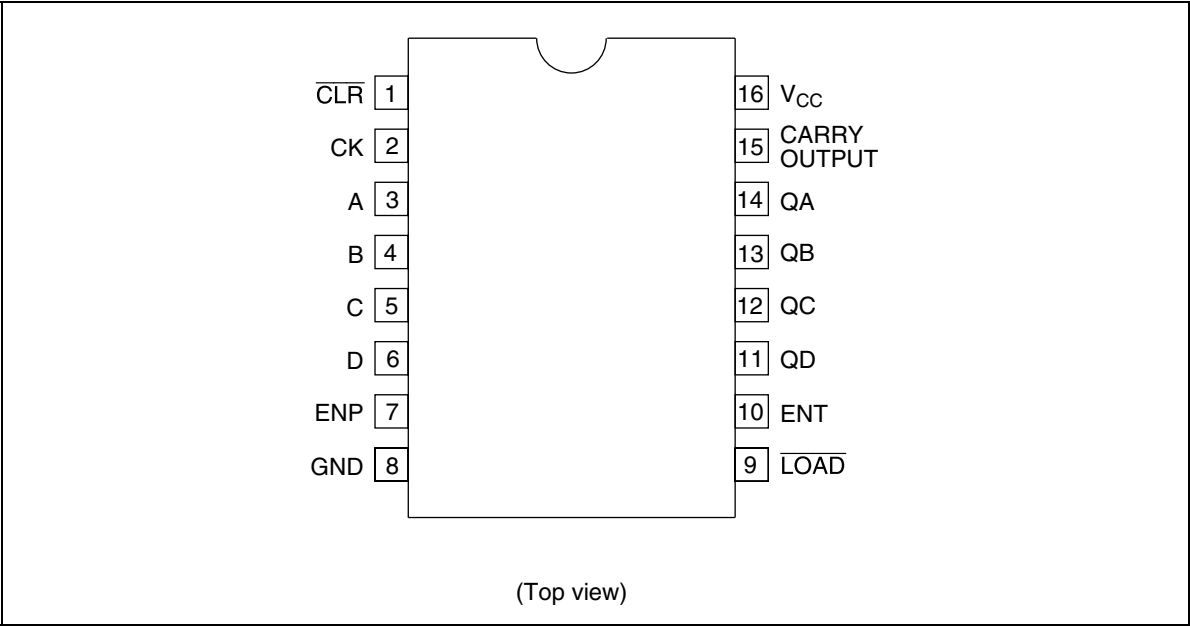
- $V_{CC} = 2.0\text{ V to }5.5\text{ V}$ operation
- All inputs $V_{IH}(\text{Max.}) = 5.5\text{ V}$ ($@V_{CC} = 0\text{ V to }5.5\text{ V}$)
- All outputs $V_O(\text{Max.}) = 5.5\text{ V}$ ($@V_{CC} = 0\text{ V}$)
- Typical V_{OL} ground bounce $< 0.8\text{ V}$ ($@V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.3\text{ V}$ ($@V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 6\text{ mA}$ ($@V_{CC} = 3.0\text{ V to }3.6\text{ V}$), $\pm 12\text{ mA}$ ($@V_{CC} = 4.5\text{ V to }5.5\text{ V}$)

Function Table

Inputs					Outputs			
CLR	LOAD	ENP	ENT	CLK	QA	QB	QC	QD
L	X	X	X	↑	L	L	L	L
H	L	X	X	↑	A	B	C	D
H	H	X	L	↑	No change			
H	H	L	X	↑	No change			
H	H	H	H	↑	Count up			
X	X	X	X	↓	No change			

Note: H: High level
L: Low level
X: Immaterial
↑: Low to high transition
↓: High to low transition
A, B, C, D: Data input
Carry = ENT • QA • QB • QC • QD

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	−0.5 to 7.0	V	
Input voltage range* ¹	V_I	−0.5 to 7.0	V	
Output voltage range* ^{1, 2}	V_O	−0.5 to $V_{CC} + 0.5$	V	Output: H or L
		−0.5 to 7.0		V_{CC} : OFF
Input clamp current	I_{IK}	−20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	T_{stg}	−65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

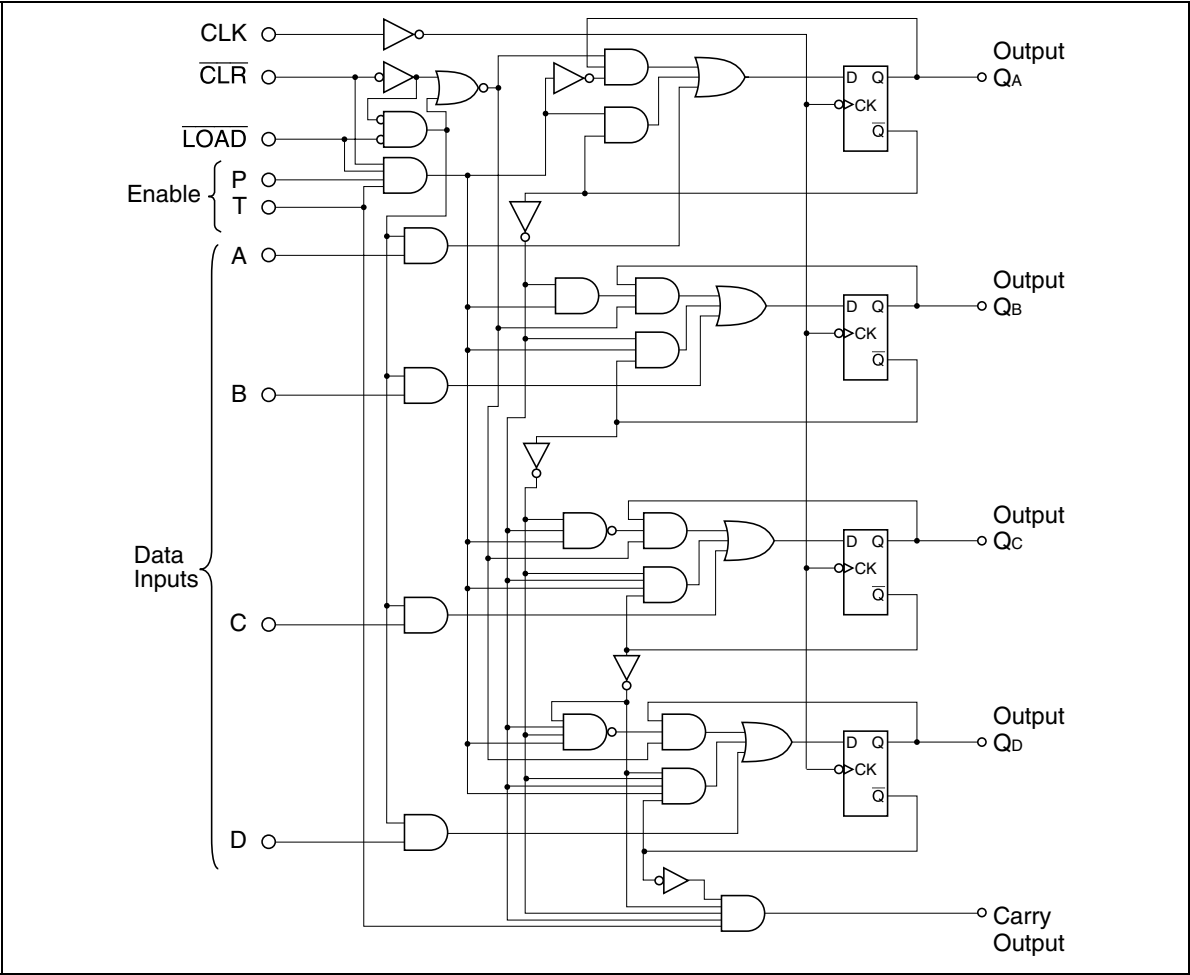
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

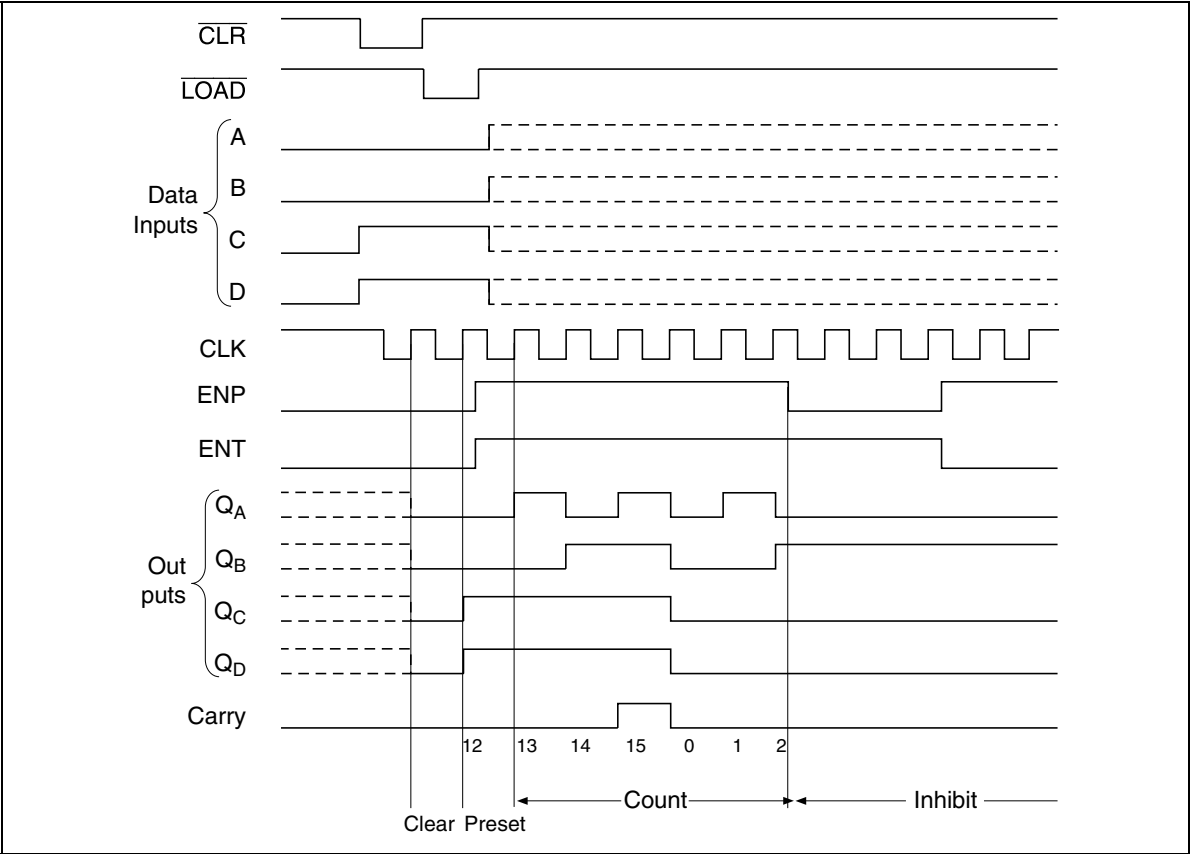
Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
Output current	I_{OH}	—	−50	μA	$V_{CC} = 2.0\text{ V}$
		—	−2	mA	$V_{CC} = 2.3\text{ to }2.7\text{ V}$
		—	−6		$V_{CC} = 3.0\text{ to }3.6\text{ V}$
		—	−12		$V_{CC} = 4.5\text{ to }5.5\text{ V}$
	I_{OL}	—	50	μA	$V_{CC} = 2.0\text{ V}$
		—	2	mA	$V_{CC} = 2.3\text{ to }2.7\text{ V}$
		—	6		$V_{CC} = 3.0\text{ to }3.6\text{ V}$
		—	12		$V_{CC} = 4.5\text{ to }5.5\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3\text{ to }2.7\text{ V}$
		0	100		$V_{CC} = 3.0\text{ to }3.6\text{ V}$
		0	20		$V_{CC} = 4.5\text{ to }5.5\text{ V}$
Operating free-air temperature	T_a	−40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



Timing Diagram



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	V _{CC} × 0.7	—	—		
		3.0 to 3.6	V _{CC} × 0.7	—	—		
		4.5 to 5.5	V _{CC} × 0.7	—	—		
	V _{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	V _{CC} × 0.3		
		3.0 to 3.6	—	—	V _{CC} × 0.3		
		4.5 to 5.5	—	—	V _{CC} × 0.3		
Output voltage	V _{OH}	Min to Max	V _{CC} - 0.1	—	—	V	I _{OL} = -50 μA
		2.3	2.0	—	—		I _{OL} = -2 mA
		3.0	2.48	—	—		I _{OL} = -6 mA
		4.5	3.8	—	—		I _{OL} = -12 mA
	V _{OL}	Min to Max	—	—	0.1		I _{OL} = 50 μA
		2.3	—	—	0.4		I _{OL} = 2 mA
		3.0	—	—	0.44		I _{OL} = 6 mA
		4.5	—	—	0.55		I _{OL} = 12 mA
Input current	I _{IN}	0 to 5.5	—	—	±1	μA	V _{IN} = 5.5 V or GND
Quiescent supply current	I _{CC}	5.5	—	—	20	μA	V _{IN} = V _{CC} or GND, I _O = 0
Output leakage current	I _{OFF}	0	—	—	5	μA	V _I or V _O = 0 V to 5.5 V
Input capacitance	C _{IN}	3.3	—	1.7	—	pF	V _I = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

$V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	fmax	50	90	—	40	—	MHz	C _L = 15 pF		
		30	60	—	25	—		C _L = 50 pF		
Propagation delay time	t _{PLH} /t _{PHL}	—	11.1	16.2	1.0	19.5	ns	C _L = 15 pF	CLK	Q
		—	14.3	19.2	1.0	22.5		C _L = 50 pF		
	t _{PLH} /t _{PHL}	—	11.5	17.0	1.0	20.5		C _L = 15 pF	CLK	Carry
		—	14.7	20.0	1.0	23.5		C _L = 50 pF		
	Count mode	—	14.7	20.0	1.0	23.5		C _L = 50 pF		
	t _{PLH} /t _{PHL}	—	13.8	20.6	1.0	24.5		C _L = 15 pF	CLK	Carry
		—	17.0	23.6	1.0	27.5		C _L = 50 pF		
	Load mode	—	17.0	23.6	1.0	27.5		C _L = 50 pF		
Setup time	t _{su}	—	10.3	15.7	1.0	19.0	ns	C _L = 15 pF	ENT	Carry
		—	14.0	18.7	1.0	22.0		C _L = 50 pF		
	t _{su}	7.5	—	—	8.5	—			Data before CLK ↑	
		10.0	—	—	11.5	—			$\overline{\text{LOAD}}$ before CLK ↑	
		9.5	—	—	11.0	—			ENT, ENP before CLK ↑	
		6.0	—	—	6.0	—			$\overline{\text{CLR}}$ before CLK ↑	
Hold time	t _h	1.5	—	—	1.5	—	ns			
		1.5	—	—	1.5	—			$\overline{\text{CLR}}$ after CLK ↑	
Pulse width	t _w	7.0	—	—	7.0	—	ns		CLK H or L	

Switching Characteristics (cont)

$$V_{CC} = 3.3 \pm 0.3 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t_{max}	80	130	—	70	—	MHz	$C_L = 15 \text{ pF}$		
		55	85	—	50	—		$C_L = 50 \text{ pF}$		
Propagation delay time	t_{PLH}/t_{PHL}	—	8.3	12.8	1.0	15.0	ns	$C_L = 15 \text{ pF}$	CLK	Q
		—	10.8	16.3	1.0	18.5		$C_L = 50 \text{ pF}$		
	t_{PLH}/t_{PHL}	—	8.7	13.6	1.0	16.0		$C_L = 15 \text{ pF}$	CLK	Carry
		—	11.2	17.1	1.0	19.5		$C_L = 50 \text{ pF}$		
	Count mode	—	11.2	17.1	1.0	19.5		$C_L = 50 \text{ pF}$		
	t_{PLH}/t_{PHL}	—	11.0	17.2	1.0	20.0		$C_L = 15 \text{ pF}$	CLK	Carry
		—	13.5	20.7	1.0	23.5		$C_L = 50 \text{ pF}$		
	t_{PLH}/t_{PHL}	—	7.5	12.3	1.0	14.5		$C_L = 15 \text{ pF}$	ENT	Carry
		—	10.5	15.8	1.0	18.0		$C_L = 50 \text{ pF}$		
Setup time	t_{su}	5.5	—	—	6.5	—	ns		Data before CLK ↑	
		8.0	—	—	9.5	—			LOAD before CLK ↑	
		7.5	—	—	9.0	—			ENT, ENP before CLK ↑	
		4.0	—	—	4.0	—			CLR before CLK ↑	
Hold time	t_h	1.0	—	—	1.0	—	ns			
		1.0	—	—	1.0	—			CLR after CLK ↑	
Pulse width	t_w	5.0	—	—	5.0	—	ns		CLK H or L	

Switching Characteristics (cont)

$$V_{CC} = 5.0 \pm 0.5 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	t_{max}	135	185	—	115	—	MHz	$C_L = 15 \text{ pF}$		
		95	125	—	85	—		$C_L = 50 \text{ pF}$		
Propagation delay time	t_{PLH}/t_{PHL}	—	4.9	8.1	1.0	9.5	ns	$C_L = 15 \text{ pF}$	CLK	Q
		—	8.7	10.1	1.0	11.5		$C_L = 50 \text{ pF}$		
	t_{PLH}/t_{PHL}	—	4.9	8.1	1.0	9.5		$C_L = 15 \text{ pF}$	CLK	Carry
		—	6.4	10.1	1.0	11.5		$C_L = 50 \text{ pF}$		
	Count mode	—	6.4	10.1	1.0	11.5		$C_L = 50 \text{ pF}$		
	t_{PLH}/t_{PHL}	—	6.2	10.3	1.0	12.0		$C_L = 15 \text{ pF}$	CLK	Carry
		—	7.7	12.3	1.0	14.0		$C_L = 50 \text{ pF}$		
	t_{PLH}/t_{PHL}	—	4.9	8.1	1.0	9.5		$C_L = 15 \text{ pF}$	ENT	Carry
		—	6.4	10.1	1.0	11.5		$C_L = 50 \text{ pF}$		
Setup time	t_{su}	4.5	—	—	4.5	—	ns		Data before CLK ↑	
		5.0	—	—	6.0	—			LOAD before CLK ↑	
		5.0	—	—	6.0	—			ENT, ENP before CLK ↑	
		3.5	—	—	3.5	—			CLR before CLK ↑	
Hold time	t_h	1.0	—	—	1.0	—	ns			
		1.5	—	—	1.5	—			CLR after CLK ↑	
Pulse width	t_w	5.0	—	—	5.0	—	ns		CLK H or L	

Operating Characteristics

 $C_L = 50 \text{ pF}$

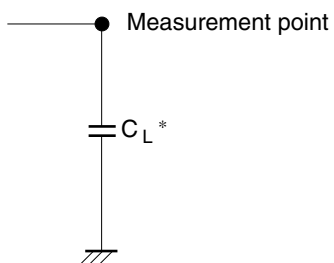
Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	3.3	—	17.3	—	pF	$f = 10 \text{ MHz}$
		5.0	—	20.6	—		

Noise Characteristics

 $C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$	3.3	—	−0.3	−0.8		
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$	3.3	—	3.0	—		
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—		
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99		

Test Circuit

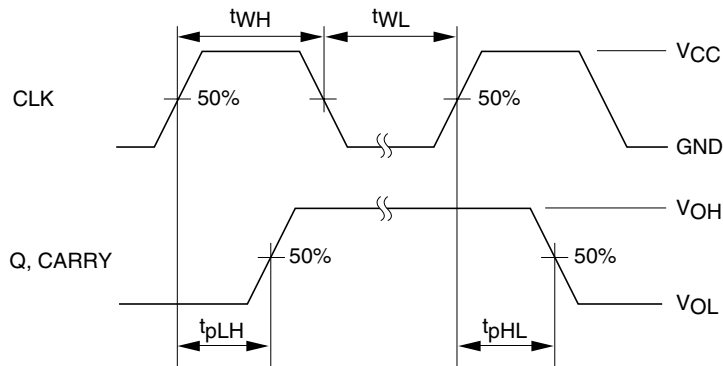


Note: 1. C_L includes the probe and jig capacitance.

Waveform

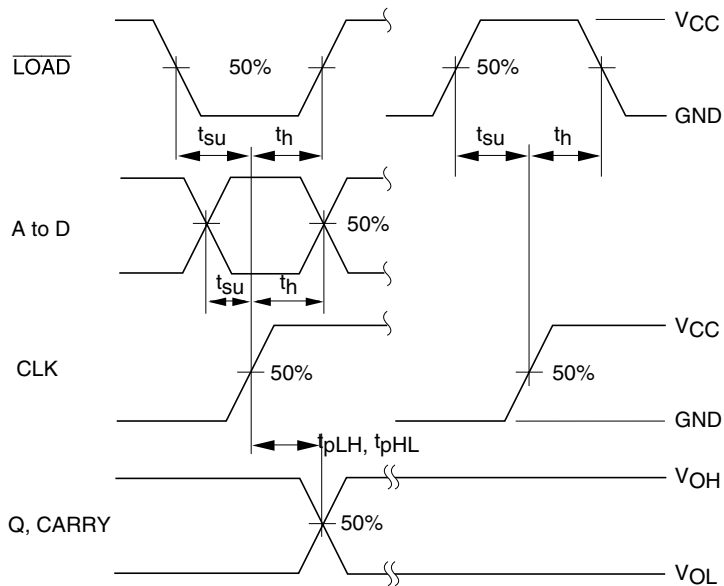
Waveform – 1

Count mode



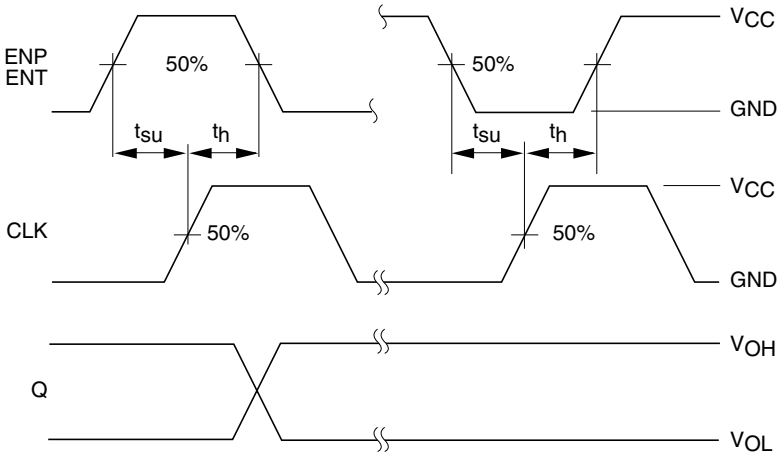
Waveform – 2

Preset mode



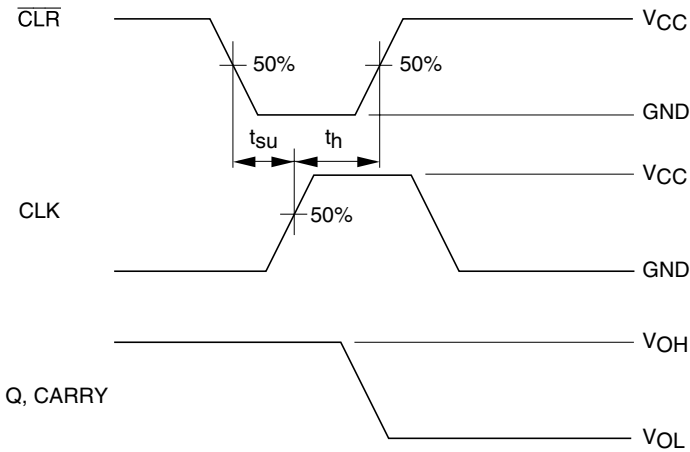
Waveform – 3

Count enable mode

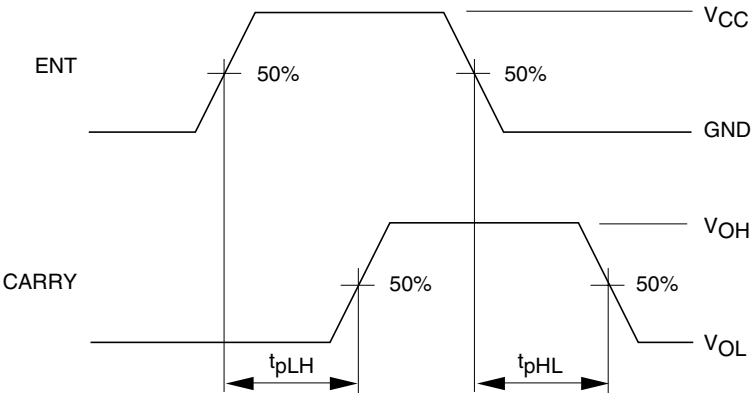


Waveform – 4

Clear mode



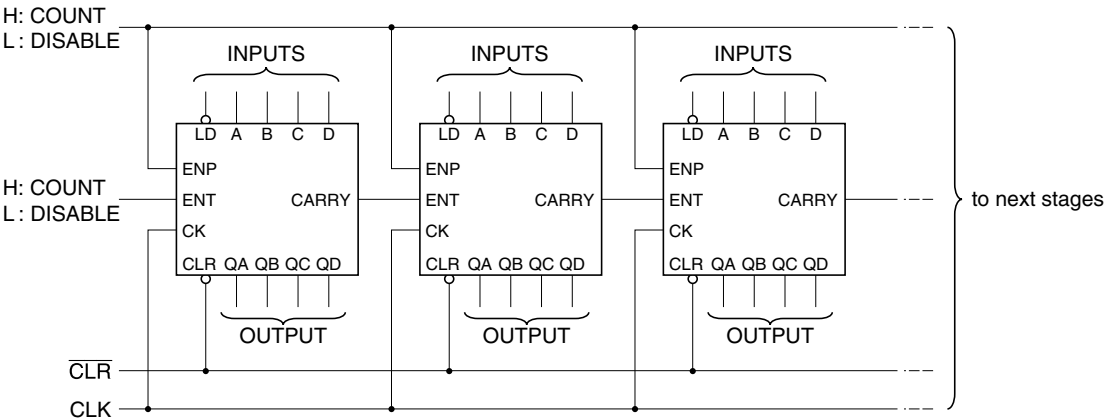
Waveform – 5
Cascade mode
(set to maximum count number)



Note: 1. Input waveform: PRR≤1 MHz, duty cycle 50%, t_r ≤3 ns, t_f ≤3 ns

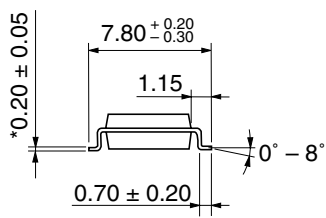
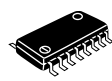
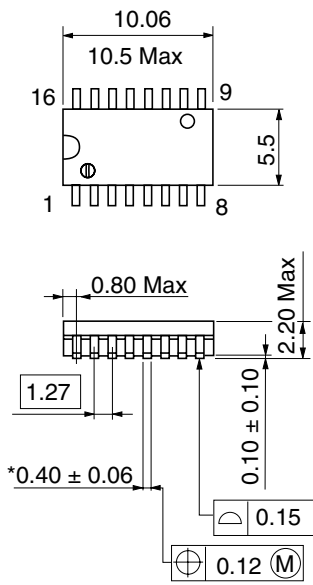
Application

Cascade circuitry



Package Dimensions

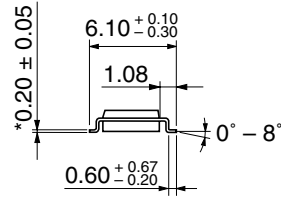
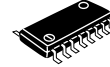
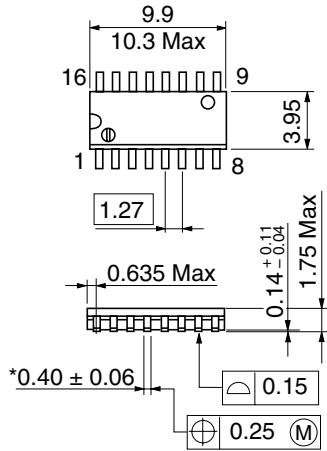
As of July, 2001
Unit: mm



*Pd plating

Hitachi Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

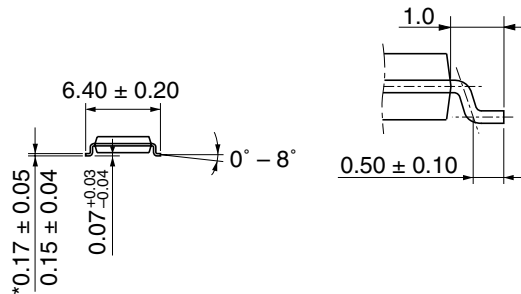
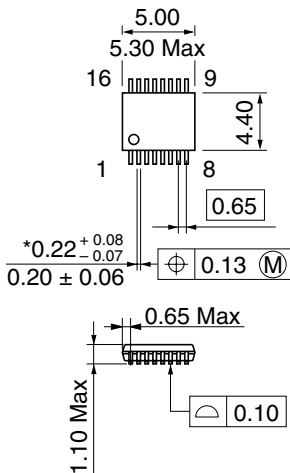
As of July, 2001
Unit: mm



*Pd plating

Hitachi Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

As of July, 2001
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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