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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HD74LV125A

Quad. Bus Buffer Gates with 3-state Outputs



ADE-205-245A (Z)

2nd. Edition
Jul. 2001

Description

The HD74LV125A features independent line drivers with three state outputs. Each output is disabled when the associated output enable ($\overline{\text{OE}}$) input is high. To ensure the high impedance state during power up or power down, $\overline{\text{OE}}$ should be connected to V_{CC} through a pull-down resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver. Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{\text{CC}} = 2.0 \text{ V}$ to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@ $V_{\text{CC}} = 0 \text{ V}$ to 5.5 V)
- All outputs V_{O} (Max.) = 5.5 V (@ $V_{\text{CC}} = 0 \text{ V}$)
- Typical V_{OL} ground bounce $< 0.8 \text{ V}$ (@ $V_{\text{CC}} = 3.3 \text{ V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)
- Typical V_{OH} undershoot $> 2.3 \text{ V}$ (@ $V_{\text{CC}} = 3.3 \text{ V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)
- Output current $\pm 8 \text{ mA}$ (@ $V_{\text{CC}} = 3.0 \text{ V}$ to 3.6 V), $\pm 16 \text{ mA}$ (@ $V_{\text{CC}} = 4.5 \text{ V}$ to 5.5 V)

Function Table

Inputs

$\overline{\text{OE}}$	A	Output Y
L	H	H
L	L	L
H	X	Z

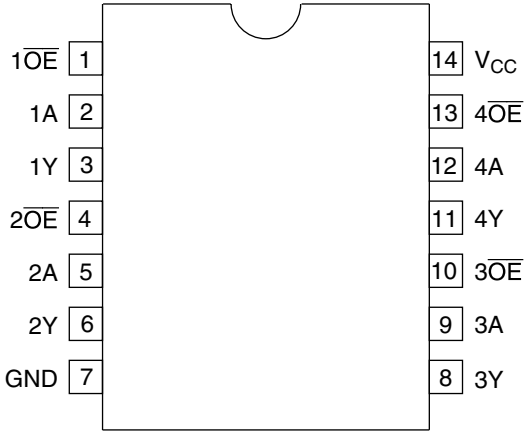
Note: H: High level

L: Low level

X: Immaterial

Z: High impedance

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	−0.5 to 7.0	V	
Input voltage range* ¹	V_I	−0.5 to 7.0	V	
Output voltage range* ^{1, 2}	V_O	−0.5 to $V_{CC} + 0.5$	V	Output: H or L
		−0.5 to 7.0		V_{CC} : OFF or Output: Z
Input clamp current	I_{IK}	−20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±35	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±70	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	T_{stg}	−65 to 150	°C	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

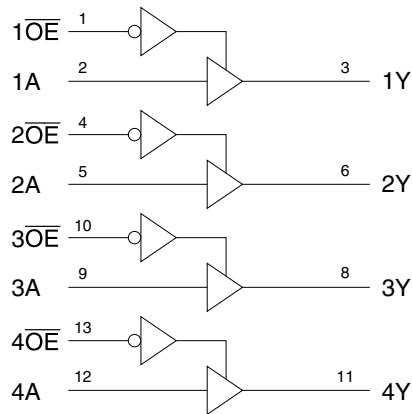
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
		0	5.5		High impedance state
Output current	I_{OH}	—	−50	μA	$V_{CC} = 2.0 V$
		—	−2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	−8		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	−16		$V_{CC} = 4.5 \text{ to } 5.5 V$
	I_{OL}	—	50	μA	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	8		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	16		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	T_a	−40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

Ta = -40 to 85°C

Item	Symbol	V _{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	V _{CC} × 0.7	—	—		
		3.0 to 3.6	V _{CC} × 0.7	—	—		
		4.5 to 5.5	V _{CC} × 0.7	—	—		
	V _{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	V _{CC} × 0.3		
		3.0 to 3.6	—	—	V _{CC} × 0.3		
		4.5 to 5.5	—	—	V _{CC} × 0.3		
Output voltage	V _{OH}	Min to Max	V _{CC} - 0.1	—	—	V	I _{OH} = -50 µA
		2.3	2.0	—	—		I _{OH} = -2 mA
		3.0	2.48	—	—		I _{OH} = -8 mA
		4.5	3.8	—	—		I _{OH} = -16 mA
	V _{OL}	Min to Max	—	—	0.1		I _{OL} = 50 µA
		2.3	—	—	0.4		I _{OL} = 2 mA
		3.0	—	—	0.44		I _{OL} = 8 mA
		4.5	—	—	0.55		I _{OL} = 16 mA
Input current	I _{IN}	0 to 5.5	—	—	±1	µA	V _I = 5.5 V or GND
Off-state output current	I _{OZ}	5.5	—	—	±5	µA	V _O = V _{CC} or GND
Quiescent supply current	I _{CC}	5.5	—	—	20	µA	V _I = V _{CC} or GND, I _O = 0
Output leakage current	I _{OFF}	0	—	—	5	µA	V _I or V _O = 0 V to 5.5 V
Input capacitance	C _{IN}	3.3	—	3.0	—	pF	V _I = V _{CC} or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

$$V_{CC} = 2.5 \pm 0.2 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	6.8	13.0	1.0	15.5	ns	$C_L = 15 \text{ pF}$	A	Y
	t_{PHL}	—	8.7	16.5	1.0	18.5		$C_L = 50 \text{ pF}$		
Enable time	t_{ZH}	—	7.0	13.0	1.0	15.5	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Y
	t_{ZL}	—	8.8	16.5	1.0	18.5		$C_L = 50 \text{ pF}$		
Disable time	t_{HZ}	—	5.1	14.7	1.0	17.0	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Y
	t_{LZ}	—	7.3	18.2	1.0	20.5		$C_L = 50 \text{ pF}$		

$$V_{CC} = 3.3 \pm 0.3 \text{ V}$$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t_{PLH}	—	4.8	8.0	1.0	9.5	ns	$C_L = 15 \text{ pF}$	A	Y
	t_{PHL}	—	6.1	11.5	1.0	13.0		$C_L = 50 \text{ pF}$		
Enable time	t_{ZH}	—	4.8	8.0	1.0	9.5	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Y
	t_{ZL}	—	6.2	11.5	1.0	13.0		$C_L = 50 \text{ pF}$		
Disable time	t_{HZ}	—	4.1	9.7	1.0	11.5	ns	$C_L = 15 \text{ pF}$	\overline{OE}	Y
	t_{LZ}	—	5.5	13.2	1.0	15.0		$C_L = 50 \text{ pF}$		

Switching Characteristics (cont)

$V_{CC} = 5.0 \pm 0.5 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	3.4	5.5	1.0	6.5	ns	C _L = 15 pF	A	Y
	t _{PHL}	—	4.3	7.5	1.0	8.5		C _L = 50 pF		
Enable time	t _{ZH}	—	3.4	5.1	1.0	6.0	ns	C _L = 15 pF	\overline{OE}	Y
	t _{ZL}	—	4.4	7.1	1.0	8.0		C _L = 50 pF		
Disable time	t _{HZ}	—	3.2	6.8	1.0	8.0	ns	C _L = 15 pF	\overline{OE}	Y
	t _{LZ}	—	4.0	8.8	1.0	10.0		C _L = 50 pF		

Output-skew Characteristics

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^{\circ}\text{C}$		$T_a = -40 \text{ to } 85^{\circ}\text{C}$		Unit
			Min	Max	Min	Max	
Output skew	$t_{sk(O)}$	2.3 to 2.7	—	2.0	—	2.0	ns
		3.0 to 3.6	—	1.5	—	1.5	
		4.5 to 5.5	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

Operating Characteristics

 $C_L = 50 \text{ pF}$

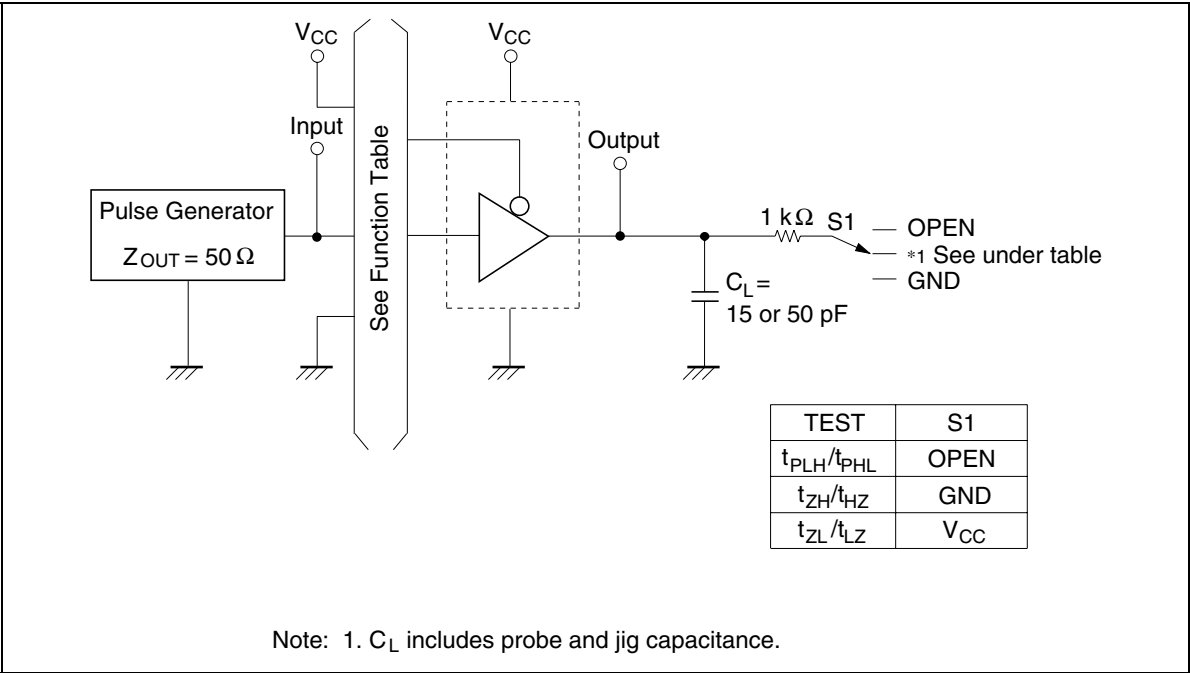
Item	Symbol	$V_{CC} = (V)$	$T_a = 25^{\circ}\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	3.3	—	15.5	—	pF	$f = 10 \text{ MHz}$
		5.0	—	17.6	—		

Noise Characteristics

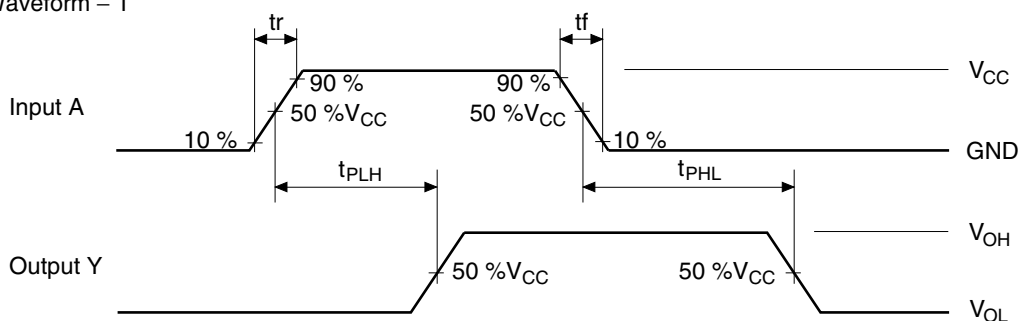
 $C_L = 50 \text{ pF}$

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^{\circ}\text{C}$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$	3.3	—	−0.3	−0.8		
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$	3.3	—	3.0	—		
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99		

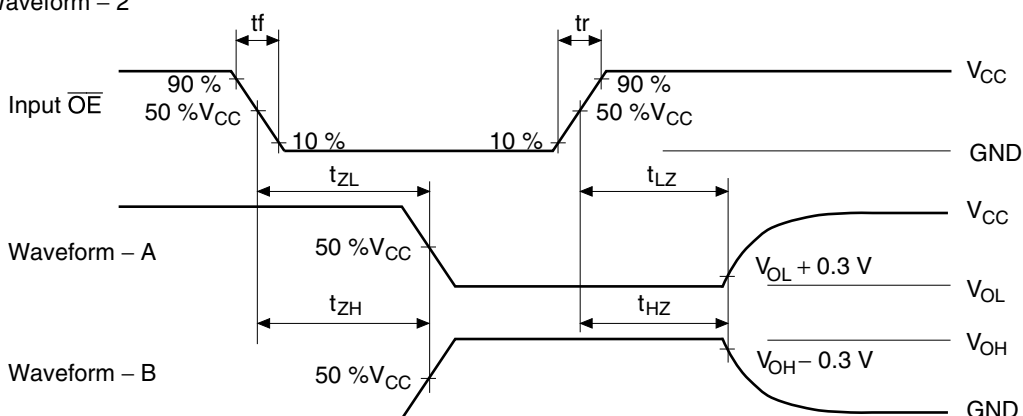
Test Circuit



• Waveform – 1



• Waveform – 2



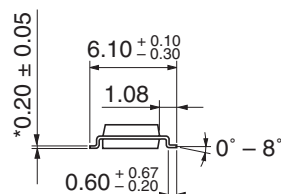
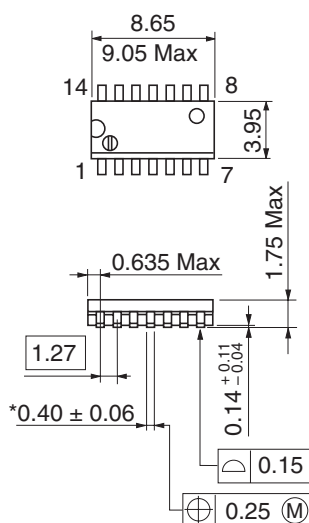
Notes: 1. $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$

2. Input waveform: PRR $\leq 1 \text{ MHz}$, duty cycle 50%

3. Waveform–A is for an output with internal conditions such that the output is low except when disabled by the output control.

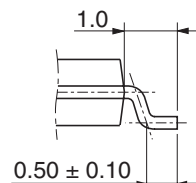
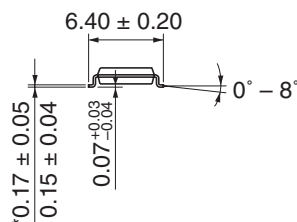
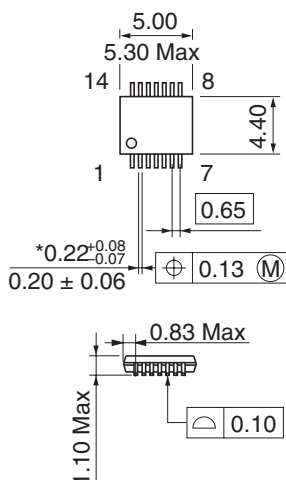
4. Waveform–B is for an output with internal conditions such that the output is high except when disabled by the output control.

As of July, 2001
Unit: mm



*Pd plating

Hitachi Code	FP-14DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.13 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-14D
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

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