

To all our customers

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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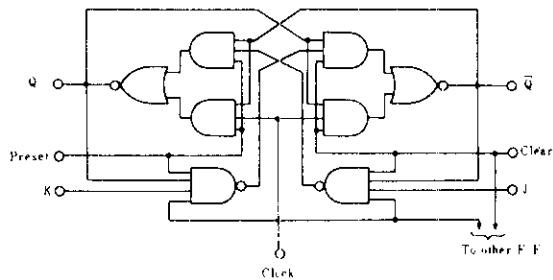
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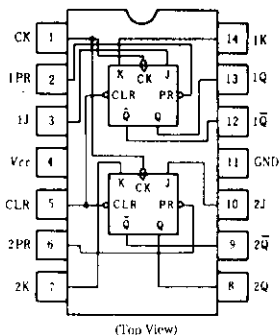
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HD74LS78A ● Dual J-K Flip-Flops (with Preset, Common Clear, and Common Clock)

■ BLOCK DIAGRAM (1/2)



■ PIN ARRANGEMENT

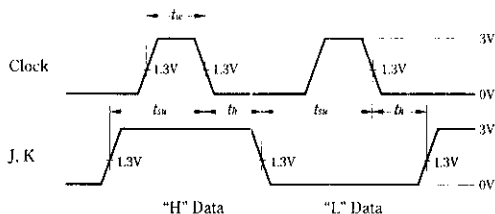


■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	Clock High	20	—	—	ns
	Preset Low	25	—	—	ns
Setup time	"H" Data	20↓	—	—	ns
	"L" Data	20↓	—	—	ns
Hold time	t_h	0↓	—	—	ns

Note) ↓: The arrow indicates the falling edge.

■ TIMING METHOD



■ FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q ₀	Q̄ ₀

Notes) H; high level, L; low level, X; irrelevant

↓; transition from high to low level

Q₀; level of Q before the indicated steady-state input conditions were established.

Q̄₀; complement of Q₀ or level of Q̄ before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

■ ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75°C)

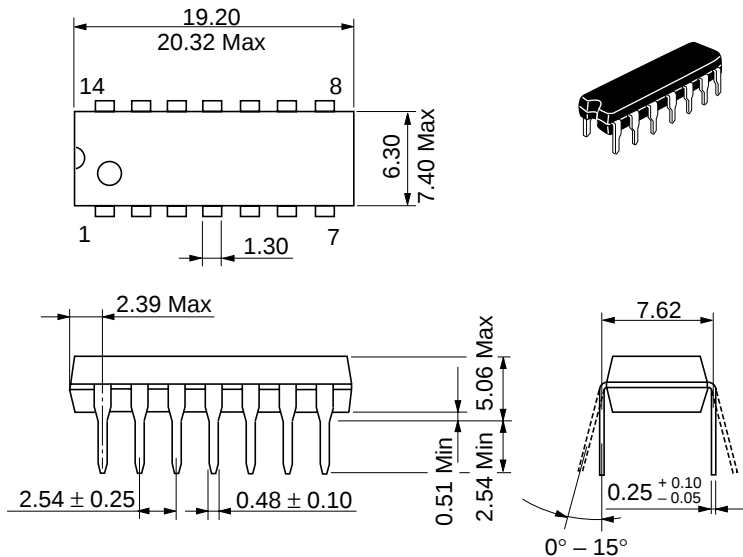
Item	Symbol	Test Conditions	min	typ*	max	Unit
Input voltage	V _{IH}		2.0	—	—	V
	V _{IL}		—	—	0.8	V
Output voltage	V _{OH}	V _{CC} = 4.75V, V _{IH} = 2.7V, V _{IL} = 0.8V, I _{OH} = -400μA	2.7	—	—	V
	V _{OL}	V _{CC} = 4.75V, V _{IH} = 2V, I _{OL} = 8mA	—	—	0.5	V
		V _{IL} = 0.8V, I _{OL} = 4mA	—	—	0.4	
			—	—	—	
Input current	J, K	V _{CC} = 5.25V, V _I = 2.7V	—	—	20	μA
	Clear		—	—	120	
	Preset		—	—	60	
	Clock		—	—	160	
	J, K		—	—	-0.4	
	Clear	V _{CC} = 5.25V, V _I = 0.4V	—	—	-1.6	mA
	Preset		—	—	-0.8	
	Clock		—	—	-1.6	
	J, K		—	—	0.1	
	Clear		—	—	0.6	
Short circuit output current	I _{OS}	V _{CC} = 5.25V, V _I = 7V	—	—	0.3	mA
			—	—	0.8	
			—	—	—	
			—	—	—	
Supply current ***	I _{CC}	V _{CC} = 5.25V	-20	4	-100	mA
Input clamp voltage	V _{IK}	V _{CC} = 4.75V, I _{IK} = -18mA	—	—	6	mA

* V_{CC} = 5V, Ta = 25°C

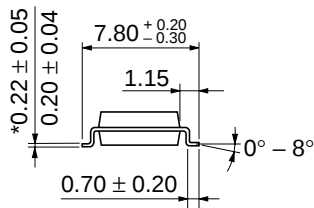
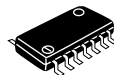
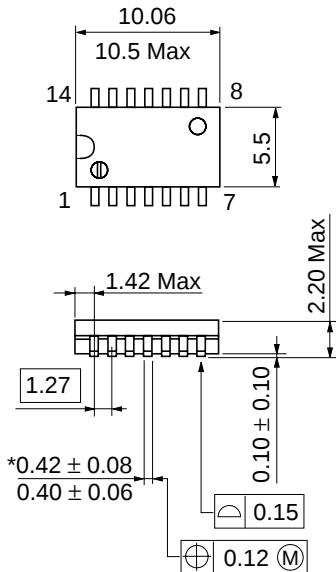
** I_{IL} should not be measured when preset and clear inputs are low at same time.

*** With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn.

At the time of measurement, the clock input is grounded.

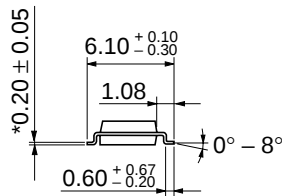
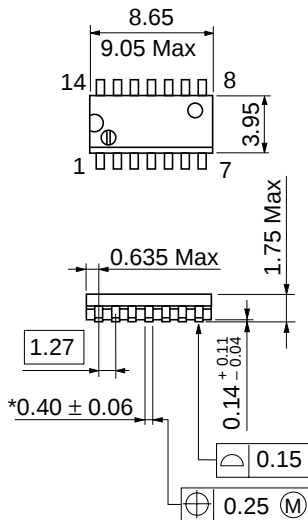


Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g



Hitachi Code	FP-14DN
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EIAJ	Conforms
Weight (reference value)	0.13 g

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