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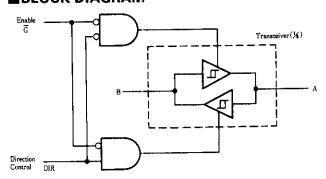
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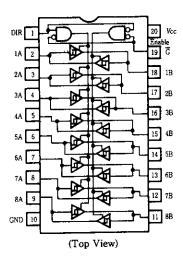
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This octal bus transceivers is designed for asynchronous two-way communication between data buses. The devices transmit data, from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input (\overline{G}) can be used to disable the device so that the buses are effectively isolated.

■BLOCK DIAGRAM



PIN ARRANGEMENT



TRECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply voltage	Vcc	4.75	5.00	5.25	v
Output voltage	Voн	_	_	5.5	V
Output current	IoL		-	48	mA
Operating temperature range	Topr	-20	25	75	°C

IFUNCTION TABLE

Enable	Direction Control	Operation		
Ğ	DIR			
L	L	B data to A bus		
L	Н	A data to B bus		
Н	×	Isolation		

Notes) H; high level, L; low level, X; irrelevant

ELECTRICAL CHARACTERISTICS $(Ta = -20 \sim +75^{\circ}C)$

Item	Symbol	Test Conditions		min	typ*	max	Unit
T	ViH			2.0	-	_	V
Input voltage	VIL			1 -	_	0.8	V
Hysteresis	$V_{T^+} - V_{T^-}$	$V_{CC} = 4.75 \text{V}$		0.2			V
Output current	Іон	$V_{CC} = 4.75 \text{V}, V_{IH} = 2 \text{V}, V_{IL} = 0.8 \text{V}, V_{OH} = 5.5 \text{V}$				100	μA
Output voltage			$I_{DL} = 12 \text{mA}$			0.4	V
	Voi	$V_{CC} = 4.75 \text{V}, V_{IH} = 2 \text{V}, V_{IL} = 0.8 \text{V}$	IoL = 24 mA		-	0.5	V
			Ica. = 48mA		_	0.5	V
IIн		$V_{CC} = 5.25 \text{V}, \ V_t = 2.7 \text{V}$				20	μA
Input current	IIL	$V_{CC} = 5.25 \text{V}, \ V_I = 0.4 \text{V}$				400	μ A
A or B		1/	$V_I = 5.5 \text{V}$	<u> </u>		0.1	mA
DIR or 0	Ī.	$V_{CC} = 5.25 \text{V}$	$V_I = 7V$		-	0.1	mA
	Іссн	Vcc=5.25V, output open			48	70	mΑ
Supply current	Icc I.				62	90	mA
	Iccz				64	95	mA
Input clamp voltage	Vik	$V_{CC} = 4.75 \text{V}, I_{IN} = -18 \text{mA}$				-1.5	V

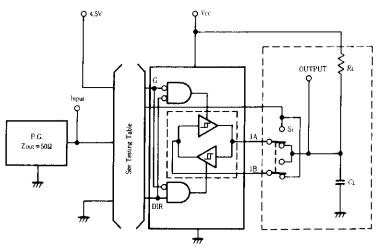
^{*} V_{CC} = 5V, Ta = 25°C

ESWITCHING CHARACTERISTICS (Vcc=5V, Ta=25°C)

Item	Symbol	INPUT	OUTPUT	Test Conditions	min	typ	max	Uni
Propagation delay time		A	В	$C_L = 45 \text{pF}, R_L = 667 \Omega$		17	25	ns
	tplн	В	Α			17	25	ns
		A	В			16	25	ns
	t _{PHL}	В	Α			16	25	ns
Output enable time	tplн	Ğ	Α		-	23	40	ns
		Ğ	В			25	40	ns
	4	Ğ	A			34	50	ns
	tPHL	Ē	В			37	50	ns

TESTING METHOD

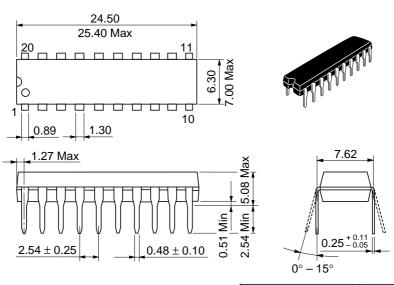
Test Circuit



Notes) 1. 2A-2B, 3A-3B, 4A-4B, 5A-5B, 6A-6B, 7A-7B, 8A-8B, are identical to above load circuit.

- C_L includes probe and jig capacitance.
 S₁ is a input-output switch.

Unit: mm



Hitachi Code	DP-20N
JEDEC	_
EIAJ	Conforms
Weight (reference value)	1.26 g

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