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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HD74LV1GT126A

Bus Buffer Gate with 3-state Output



ADE-205-333F (Z)

7th. Edition
Feb. 2003

Description

The HD74LV1GT126A has a bus buffer gate with 3-state output in a 5 pin package. Output is disabled when the associated output enable (OE) input is low. To ensure the high impedance state during power up or power down, OE should be connected to V_{cc} through a pull-down resistor; the minimum value of the resistor is determined by the current sourcing capability of the driver. Low voltage and high speed operation is suitable for the battery powered products (e.g., notebook computers), and the low power consumption extends the battery life.

Features

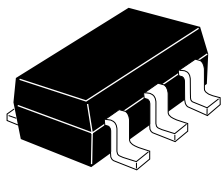
- The basic gate function is lined up as hitachi uni logic series.
- Supplied on emboss taping for high speed automatic mounting.
- TTL compatible input level.
Supply voltage range : 4.5 to 5.5 V
Operating temperature range : -40 to +85°C
- All inputs V_{IH} (Max.) = 5.5 V (@ V_{cc} = 0 V to 5.5 V)
All outputs V_O (Max.) = 5.5 V (@ V_{cc} = 0 V, Output : Z)
- Output current ± 12 mA (@ V_{cc} = 4.5 V to 5.5 V)
- All the logical input has hysteresis voltage for the slow transition.
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV1GT126ACME	CMPAK-5 pin	CMPAK-5V	CM	E (3,000 pcs/reel)
HD74LV1GT126AVSE	VSON-5 pin	TNP-5DV	VS	E (3,000 pcs/reel)

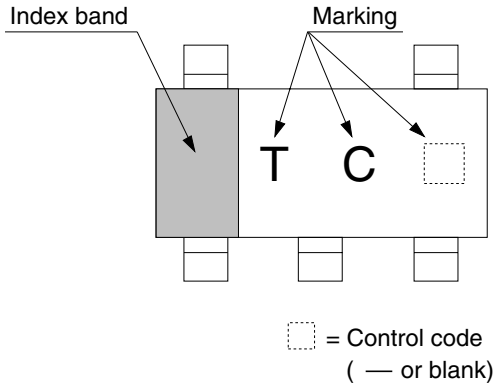
Note: Please consult the sales office for the above package availability.

Outline and Article Indication

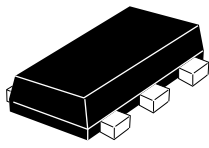
• HD74LV1GT126A



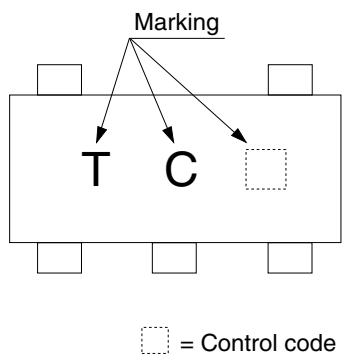
CMPAK-5



• HD74LV1GT126A



VSON-5



Function Table

Inputs		Output Y
OE	A	
H	H	H
H	L	L
L	X	Z

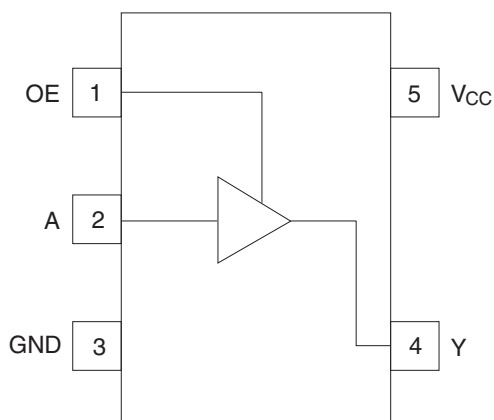
H : High level

L : Low level

X : Immaterial

Z : High impedance

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	−0.5 to 7.0	V	
Input voltage range ^{*1}	V_I	−0.5 to 7.0	V	
Output voltage range ^{*1,2}	V_O	−0.5 to $V_{CC} + 0.5$ −0.5 to 7.0	V	Output : H or L V_{CC} : OFF or Output : Z
Input clamp current	I_{IK}	−20	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ^{*3}	P_T	200	mW	
Storage temperature	T_{stg}	−65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	4.5	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC} 0 5.5	V	Output : Z
Output current	I_{OH}	—	12	mA	$V_{CC} = 4.5$ to 5.5 V
	I_{OL}	—	−12	mA	$V_{CC} = 4.5$ to 5.5 V
Input transition rise or fall rate	$\Delta t / \Delta v$	0	20	ns / V	$V_{CC} = 4.5$ to 5.5 V
Operating free-air temperature	T_a	−40	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.

Electrical Characteristic

- $T_a = -40$ to 85°C

Item	Symbol	V_{CC} (V) *	Min	Typ	Max	Unit	Test condition
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	—	V	
	V_{IL}	4.5 to 5.5	—	—	0.8		
Hysteresis voltage	V_H	5.0	—	0.15	—	V	$V_T^+ - V_T^-$
Output voltage	V_{OH}	Min to Max	$V_{CC} - 0.1$	—	—	V	$I_{OH} = -50\ \mu\text{A}$
		4.5	3.8	—	—		$I_{OH} = -12\ \text{mA}$
	V_{OL}	Min to Max	—	—	0.1		$I_{OL} = 50\ \mu\text{A}$
		4.5	—	—	0.55		$I_{OL} = 12\ \text{mA}$
Input current	I_{IN}	0 to 5.5	—	—	± 1	μA	$V_{IN} = 5.5\ \text{V}$ or GND
Quiescent supply current	I_{CC}	5.5	—	—	10	μA	$V_{IN} = V_{CC}$ or GND, $I_O = 0$
	ΔI_{CC}	5.5	—	—	1.5	mA	One input $V_{IN} = 3.4\ \text{V}$, other input V_{CC} or GND
Output leakage current	I_{OFF}	0	—	—	5	μA	V_{IN} or $V_O = 0$ to $5.5\ \text{V}$
Input capacitance	C_{IN}	5.0	—	3.0	—	pF	$V_{IN} = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- $V_{CC} = 5.0 \pm 0.5 \text{ V}$

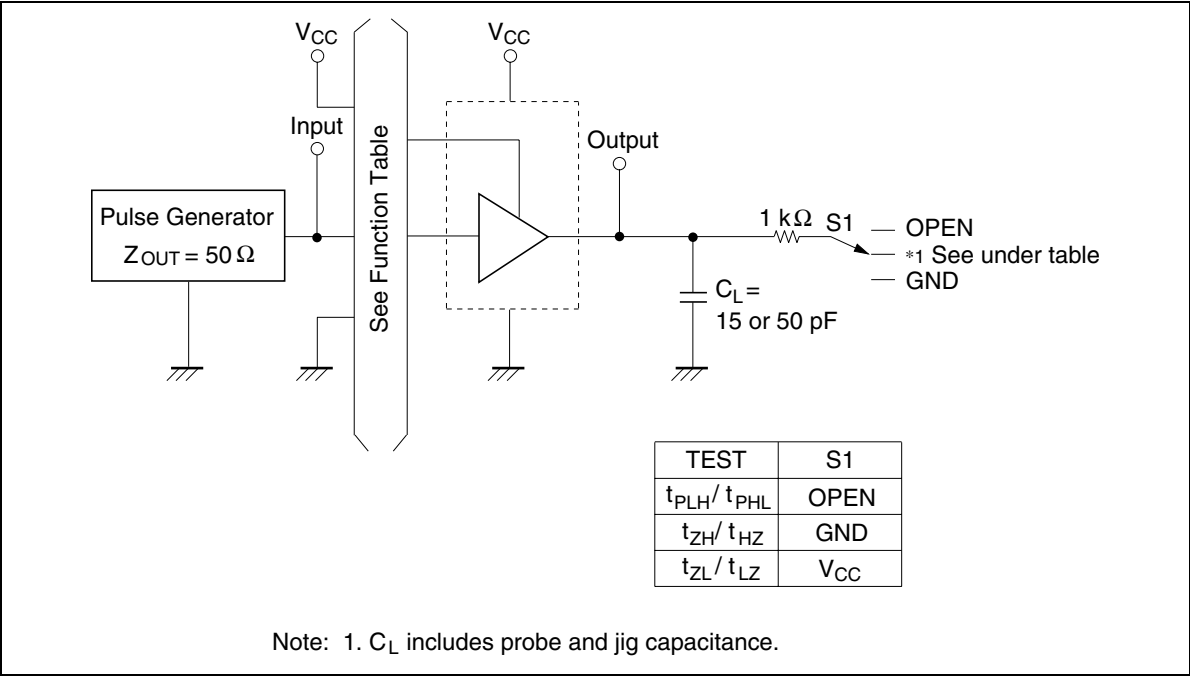
Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	3.5	5.5	1.0	6.5	ns	C _L = 15 pF	A	Y
	t _{PHL}	—	4.6	7.5	1.0	8.5		C _L = 50 pF		
Enable time	t _{ZH}	—	3.6	5.1	1.0	6.0	ns	C _L = 15 pF	OE	Y
	t _{ZL}	—	4.6	7.1	1.0	8.0		C _L = 50 pF		
Disable time	t _{HZ}	—	3.3	6.8	1.0	8.0	ns	C _L = 15 pF	OE	Y
	t _{LZ}	—	4.3	8.8	1.0	10.0		C _L = 50 pF		

Operating Characteristics

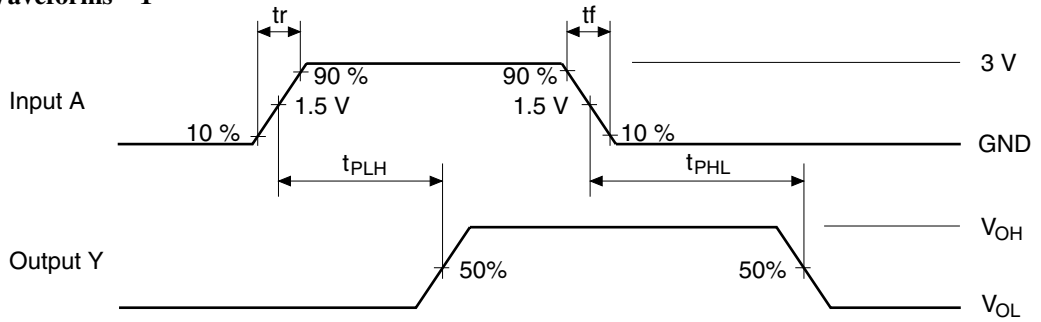
- C_L = 50 pF

Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C _{PD}	5.0	—	11.5	—	pF	f = 10 MHz

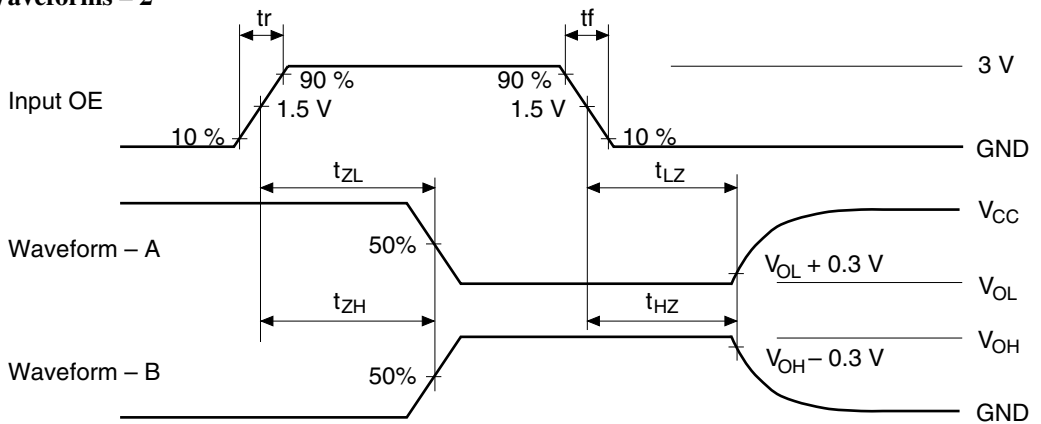
Test Circuit



• Waveforms – 1



• Waveforms – 2



Notes: 1. $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$

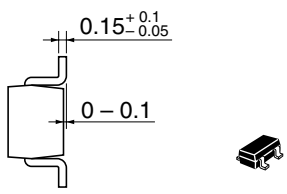
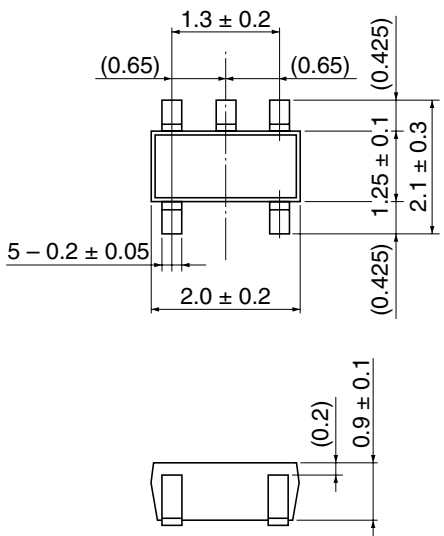
2. Input waveform : $\text{PRR} \leq 1 \text{ MHz}$, duty cycle 50%

3. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.

4. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.

Package Dimensions

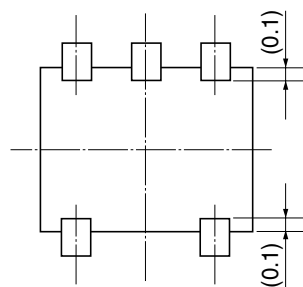
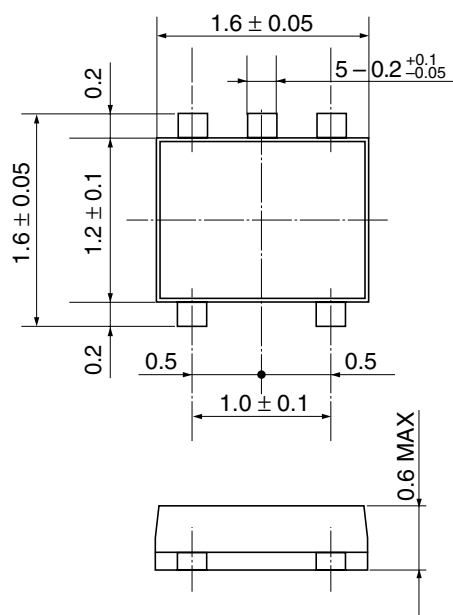
Unit: mm



*Sn-Bi plating

Hitachi Code	CMPAK-5V
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.006 g

Unit: mm



*Sn-Bi plating

Hitachi Code	TNP-5DV
JEDEC	—
JEITA	—
Mass (reference value)	0.002 g

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