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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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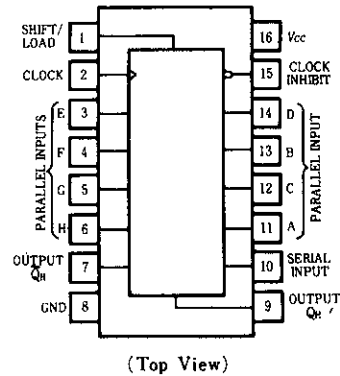
HD74LS165A

Parallel-Load 8-bit Shift Register

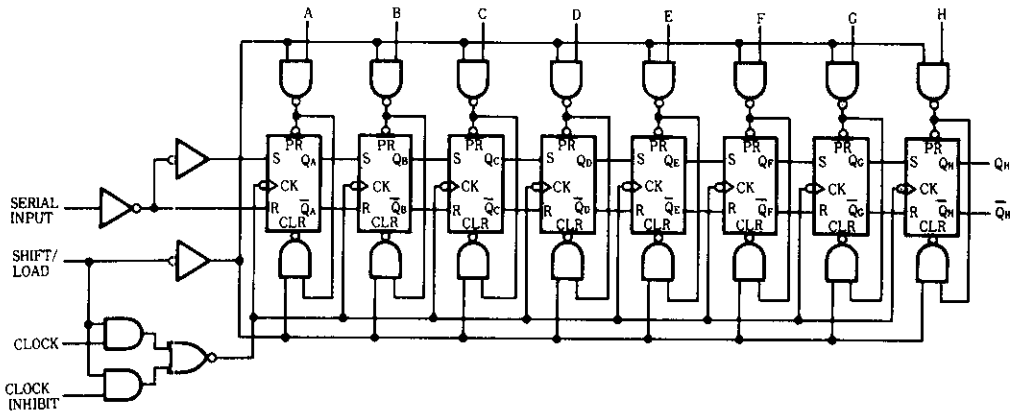
The LS165A are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

PIN ARRANGEMENT



BLOCK DIAGRAM



FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . H	Q_A	Q_B	
L	X	X	X	a . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Cn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

- Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. a ~ h; the level of steady-state input at inputs A to H respectively
4. $Q_{A0} \sim Q_{H0}$; the level of Q_A to Q_H , respectively, before the indicated steady-state input conditions were established.
5. $Q_{An} \sim Q_{Gn}$; the level of Q_A to Q_G , respectively, before the most recent ↓ transition of the clock.

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output current	I_{OH}	—	—	—400	μA
Low level output current	I_{OL}	—	—	8	mA
Clock frequency	f_{clock}	0	—	25	MHz
Clock pulse width	t_w (clock)	25	—	—	ns
Load pulse width	t_w (load)	15	—	—	ns
Clock-enable Setup time	t_{su}	30	—	—	ns
Parallel-input Setup time	t_{su}	10	—	—	ns
Serial input setup time	t_{su}	20	—	—	ns
Shift setup time	t_{su}	45	—	—	ns
Hold time at only input	t_h	0	—	—	ns

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ C$)

Item		Symbol	Test Conditions	min	typ*	max	Unit
Input voltage		V_{IH}		2.0	—	—	V
		V_{IL}		—	—	0.8	V
Output voltage		V_{OH}	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.8V$, $I_{OH} = -400\mu A$	2.7	—	—	V
		V_{OL}	$V_{CC} = 4.75V$, $V_{IH} = 2V$	—	—	0.4	V
			$V_{IL} = 0.8V$	—	—	0.5	V
Input current	Shift/Load	I_I	$V_{CC} = 5.25V$ $V_I = 7V$	—	—	0.3	mA
	Other inputs			—	—	0.1	mA
High level input current	Shift/Load	I_{IH}	$V_{CC} = 5.25V$ $V_I = 2.7V$	—	—	60	μA
	Other inputs			—	—	20	μA
Low level input current	Shift/Load	I_{IL}	$V_{CC} = 5.25V$ $V_I = 0.4V$	—	—	1.2	mA
	Other inputs			—	—	—0.4	mA
Short-circuit output current		I_{OS}	$V_{CC} = 5.25V$	—20	—	—100	mA
Supply current**		I_{CC}	$V_{CC} = 5.25V$	—	—	36	mA
Input clamp voltage		V_{IK}	$V_{CC} = 4.75V$, $I_{IN} = -18mA$	—	—	1.5	V

* $V_{CC} = 5V$, $T_a = 25^\circ C$

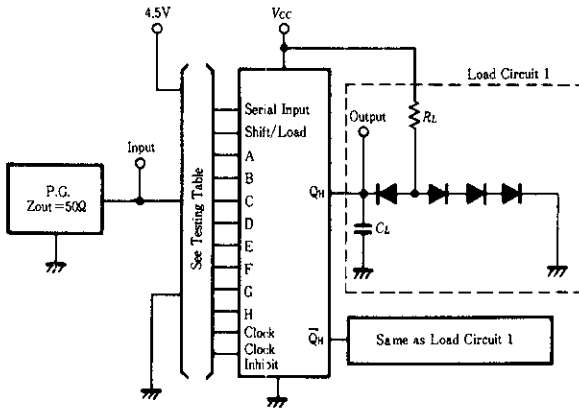
** With the outputs open, clock inhibit and clock at 4.5V, and a clock pulse applied to the shift/load, I_{CC} is measured with the parallel inputs at 4.5V, then with the parallel inputs grounded.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^\circ C$)

Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Maximum Clock frequency	f_{max}			$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$	25	35	—	MHz
Propagation Delay time	t_{PHL}	Load	Any		—	21	35	ns
	t_{PLH}				—	26	35	ns
	t_{PHL}	Clock	Any		—	14	25	ns
	t_{PLH}				—	16	25	ns
	t_{PHL}	H	Q_H		—	13	25	ns
	t_{PLH}				—	24	30	ns
	t_{PHL}	H	Q_H		—	19	30	ns
	t_{PLH}				—	17	25	ns

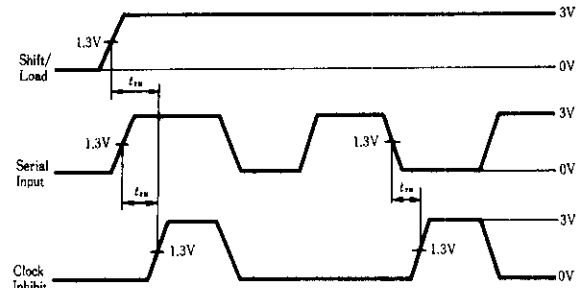
TESTING METHOD

Test Circuit



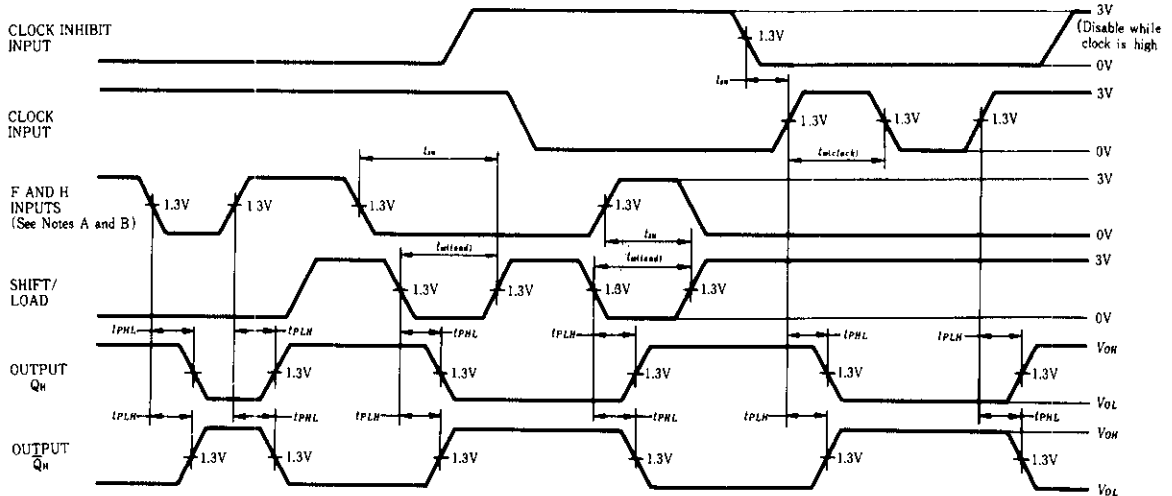
- Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 \oplus .

Waveform



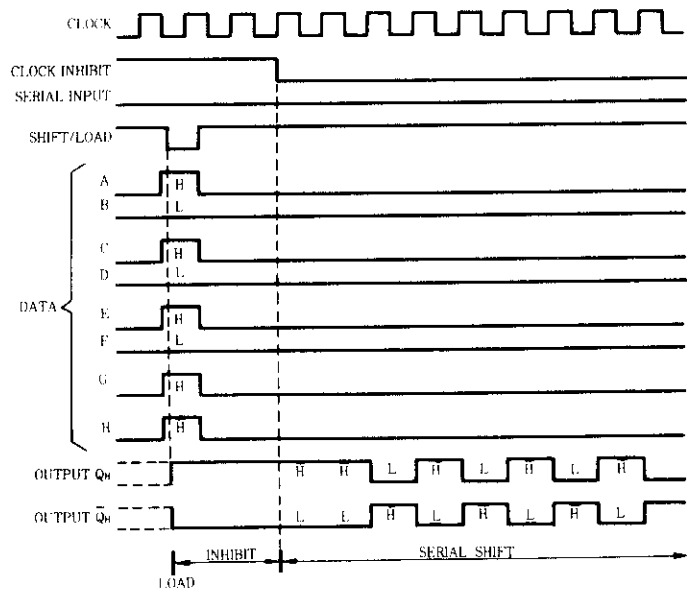
- Notes) A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_{n+7} .
B. The input pulse generators have the following characteristics: $PRR < 1 \text{ MHz}$, duty cycle $< 50\%$, $Z_{out} \approx 50\Omega$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

Waveform

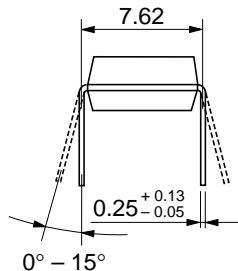
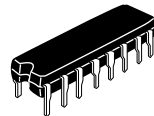
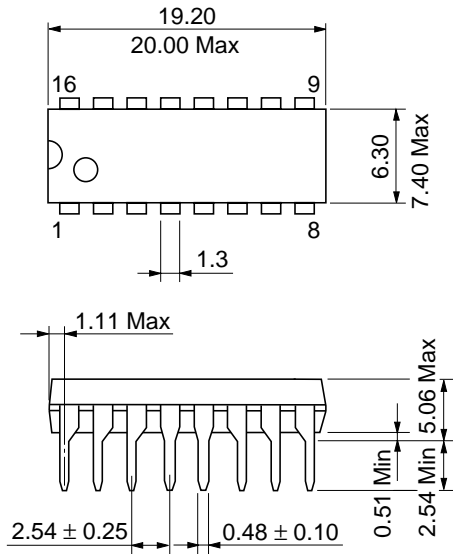


- Notes) A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_{out} \approx 50\Omega$, $t_r \leq 15 \text{ ns}$, $t_f \leq 6 \text{ ns}$.

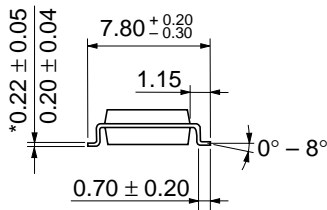
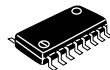
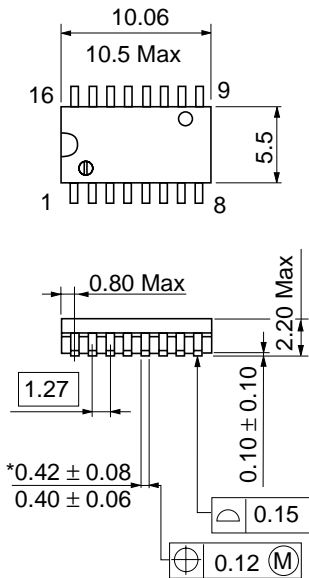
■ TYPICAL SHIFT, LOAD AND INHIBIT SEQUENCES



Unit: mm

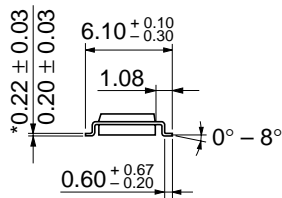
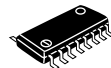
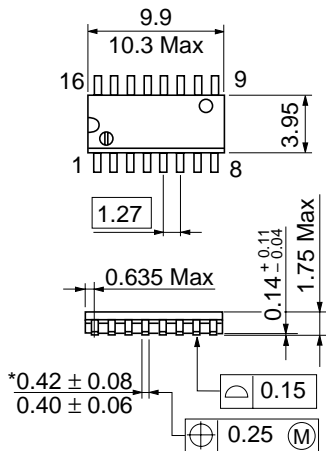


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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