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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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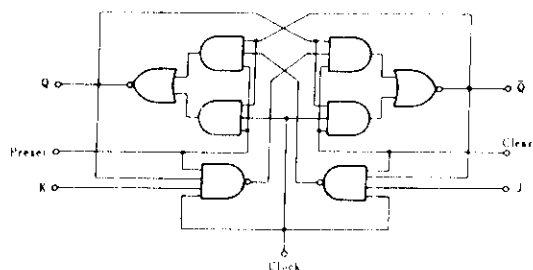
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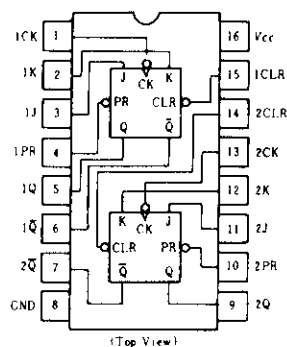
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HD74LS112 ● Dual J-K Negative-edge-triggered Flip-Flops (with Preset and Clear)

■ BLOCK DIAGRAM (1/2)



■ PIN ARRANGEMENT



■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	Clock High	20	—	—	ns
	Clear Preset Low	25	—	—	ns
Setup time	"H" Data	20↓	—	—	ns
	"L" Data	20↓	—	—	ns
Hold time	t_h	0↓	—	—	ns

Note) ↓: The arrow indicates the falling edge.

■ FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	\bar{Q}_0

Notes) H; high level, L; low level, X; irrelevant

↓; transition from high to low level

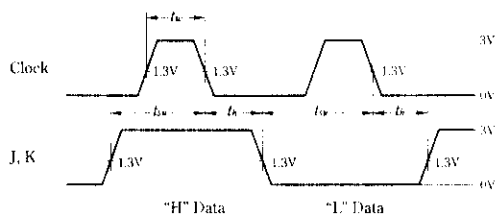
Q_0 ; level of Q before the indicated steady-state input conditions were established.

\bar{Q}_0 ; complement of Q_0 or level of \bar{Q} before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

■ TIMING DEFINITION



■ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item		Symbol	Test Conditions	min	typ*	max	Unit
Input voltage		V_{IH}		2.0	—	—	V
		V_{IL}		—	—	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-400\mu\text{A}$	2.7	—	—	V
		V_{OL}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}$	—	—	0.5	V
			$V_{IL}=0.8\text{V}$	—	—	0.4	
Input current		J, K	I_{IH} $V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	—	—	20	μA
		Clear		—	—	60	
		Preset		—	—	60	
		Clock		—	—	80	
		J, K	I_{IL}^{**} $V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	-0.4	mA
		Clear		—	—	-0.8	
		Preset		—	—	-0.8	
		Clock		—	—	-0.8	
		J, K	I_I $V_{CC}=5.25\text{V}, V_I=7\text{V}$	—	—	0.1	mA
		Clear		—	—	0.3	
		Preset		—	—	0.3	
		Clock		—	—	0.4	
Short-circuit output current		I_{OS}	$V_{CC}=5.25\text{V}$	-20	—	-100	mA
Supply current ***		I_{CC}	$V_{CC}=5.25\text{V}$	—	4	8	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V

* $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

** I_{IL} should not be measured when preset and clear inputs are low at same time.

*** With all outputs open, I_{CC} is measured with the Q and \bar{Q} outputs high in turn.
At the time of measurement, the clock input is grounded.

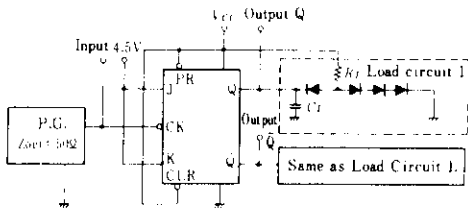
■SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}, T_a=25^\circ\text{C}$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L=15\text{pF}, R_L=2\text{k}\Omega$	30	45	—	MHz
Propagation delay time	t_{PLH}	Clear Preset Clock	Q, \bar{Q}		—	11	20	ns
	t_{PHL}				—	15	30	ns

■ TESTING METHOD

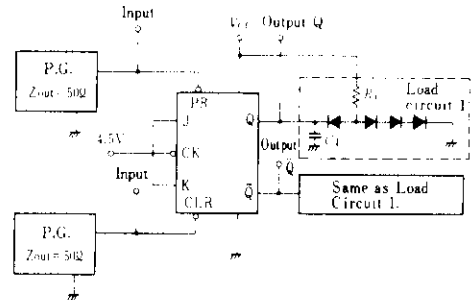
1) Test Circuit

1.1) f_{max} , t_{PLH} , t_{PHL} (Clock \rightarrow Q, \bar{Q})



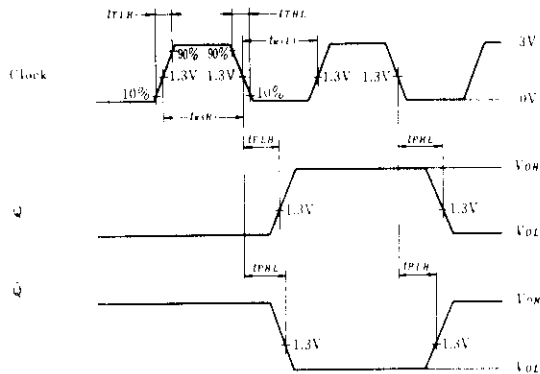
- Notes)
1. Test is put into the each flip-flop.
 2. All diodes are 1S2074 Φ .
 3. C_L includes probe and jig capacitance.

1.2) t_{PHL} , t_{PLH} (Clear, Preset \rightarrow Q, \bar{Q})

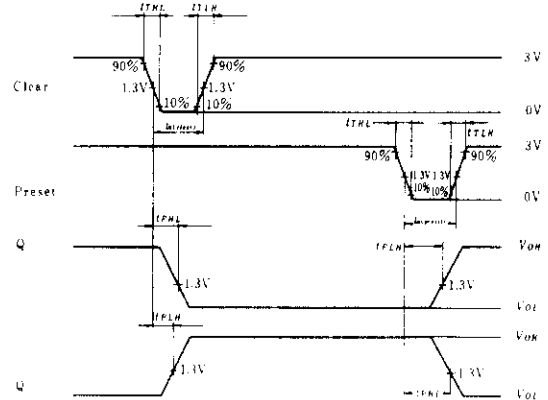


- Notes)
1. Test is put into the each flip-flop.
 2. All diodes are 1S2074 Φ .
 3. C_L includes probe and jig capacitance.

Waveform

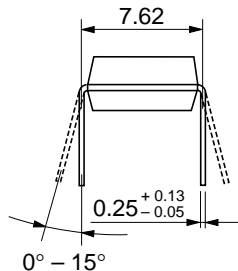
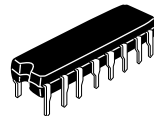
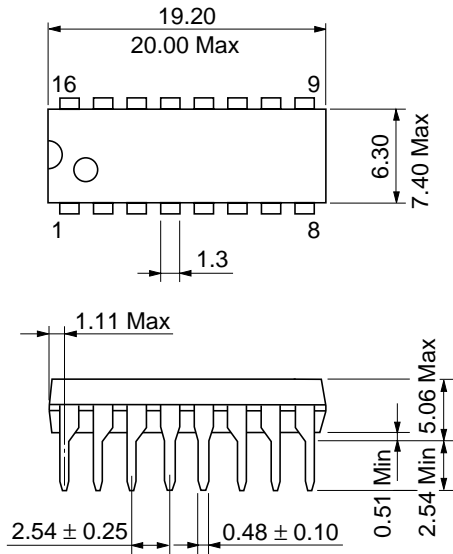


Note) Clock input pulse; $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$, $PRR=1\text{MHz}$, duty cycle=50% and: for f_{max} , $t_{TLH}=t_{THL} \leq 2.5\text{ns}$.

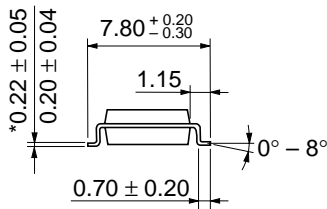
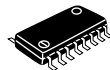
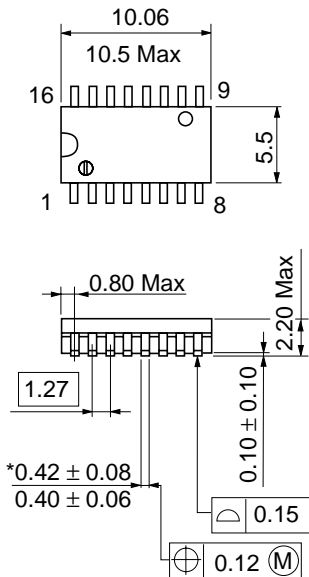


Note) Clear and preset input pulse; $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$, $PRR=1\text{MHz}$

Unit: mm

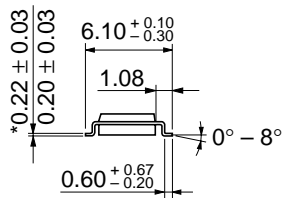
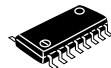
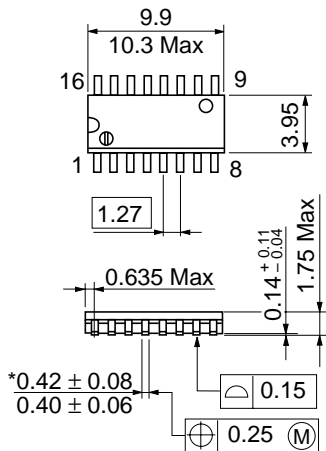


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322
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Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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