Hummingbird Device Set

For 900 MHz and 2.4 GHz diSSTance™ Technology Cordless Telephone

The **Hummingbird** continues Conexant's tradition of system-level solutions for 900 MHz and 2.4 GHz cordless telephones using Conexant's diSSTance™ (digital Spread Spectrum) technology. The Hummingbird offers higher integration, improved audio quality, lower power consumption, and increased flexibility for OEM features.

The device set is designed to operate with Conexant's Gen4 900 MHz RF chip set (RF105, RF106) or 2.4 GHz RF chip set (RF109, RF110), to achieve a complete system design for the lowest system cost.

With only six devices in the completed system design (Figure 1), the Hummingbird provides a highly integrated solution. It performs all diSSTance protocol, data formatting, spread spectrum, audio processing and peripheral functions in conformance with United States FCC regulation part 15.247. The device set is self-configurable for use in either a handset (HS) or base station (BS).

Hummingbird consists of: 1) an **ASIC**, into which are integrated a **baseband modem**, an **audio modem**, and a **controller**; and 2) a linear **audio codec**.

The ASIC and audio codec are packaged in a single 100-pin device to minimize system cost. The ASIC and audio codec are also available as separate devices (144-pin ASIC, 32-pin codec) to allow for more flexible OEM designs.

The **baseband modem** provides all modulation, encoding, spreading, scrambling, TDD control, AGC, AFC, decoding, and timing required for a diSSTance cordless telephone system.

The **audio modem** consists of an ITU G.726-compliant 40 kbps or 32 kbps ADPCM engine that interfaces to the audio codec. Built-in DTMF and ring tone with audio path control complete the interface for audio support functions.

The **controller**, an embedded MC19 (65C02) micro-controller core, performs all control and monitoring functions required for a digital spread spectrum (DSS) telephone. Interfaces are provided for all peripheral functions needed for a complete DSS telephone.

Power management algorithms and 3.6V operation provide optimum standby and talk time using a 3-cell battery.

The **audio codec** is ITU G.714-compliant. It converts analog signals from the PSTN and microphone to and from digital voice samples for the audio modem. It has built-in electret microphone interfaces and independent audio channels for line and speaker interfaces.

To reduce time to market, a royalty-free license is available for Conexant's fully functional spread-spectrum telephone software, which a user can customize to add unique phone features. Software and hardware design support is provided with each fully functional spread-spectrum telephone development system (handset and base), plus ROM emulators for software development.

Hummingbird supports the following configurations:

- Basic phone
- Basic Caller ID
- HDX speakerphone
- 2-line operation

Features

- Digital spread-spectrum communication engine
- Designed for North America
  - FCC part 15.247 compliant
  - 900 MHz and 2.4 GHz ISM bands (OEM-selectable)
- Supports Australia and New Zealand radio frequency bands (900 MHz only)
- Single baseband device provides lowest-cost solution for base station and handset
- Highly flexible solution
- 3.6 Volt, low-power operation
  - ~14-day standby (typical for 900 MHz and 2.4 GHz)
  - 5-hour talk time (typical for 900 MHz)
  - 4-hour talk time (typical for 2.4 GHz)
- Complete telephone firmware provided

(Features continued on next page)

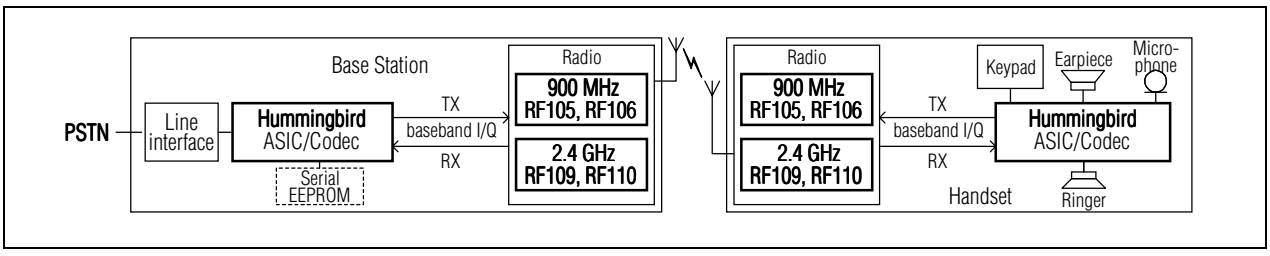

Figure 1. Typical Spread-Spectrum Telephone System Architecture – Lowest Cost Implementation

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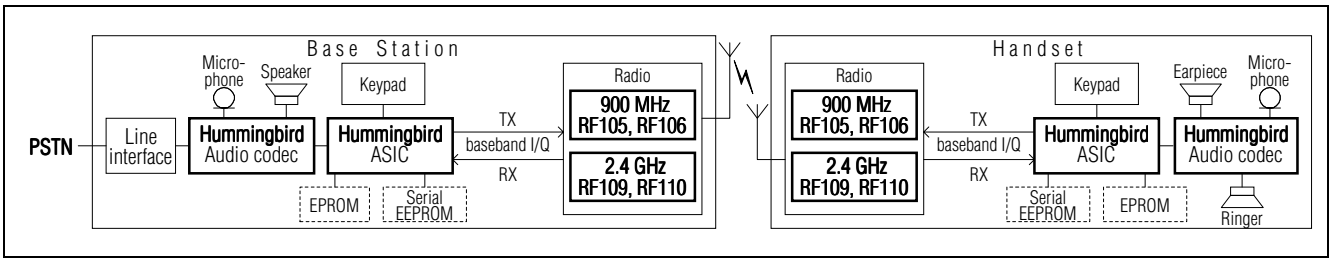


Figure 2. Typical Spread-Spectrum Telephone System Architecture – Flexible Implementation

Features (continued)

1. System Controller

- MC19 CPU (65C02 based)
- Single 9.6 MHz system clock with low power, on-chip oscillator
- On-chip 24 KB ROM, 1792 bytes RAM
- Watchdog/sleep/wake-up timer
- External parallel bus (external memory, emulation port, 144-pin ASIC only)
- Programmable wait states
- External interrupt

2. Controller Peripheral Functions

- Gen4 900 MHz RF (RF105, RF106) or 2.4 GHz RF (RF109, RF110) transceiver control (selectable by OEM)
- Interface to Mitel CID detector chip
- Interface and control to HDX speakerphone IC
- Multiplexed 4x8 keypad/GPIO switches/LCD data interface
- Battery level detector with programmable thresholds
- Serial link for base station to handset communication
- Serial port for I2C™ or 4-wire MICROWIRE™ serial EEPROM
- 4- or 8-bit parallel LCD interface port
- 6 maskable LED control ports with programmable on/off durations
- Programmable flash duration
- Off-hook control
- Audio codec serial port interface
- Ringer/buzzer control
- Integrated voltage detector for power-on reset

3. diSSTance Baseband Modem

- I/Q A/D modem input
- DBPSK DSS modulator/demodulator
- 12 chips/bit, 11 dB processing gain
- Additional security with 2^{24} ID and control channel scrambling codes
- Time Division Duplexing (TDD) control, 5ms round-trip echo delay
- Automatic acquisition and tracking
- Automatic Frequency Compensation (AFC)
- Automatic Gain Control (AGC)
- Automatic framing and rate adaptation
- 20 independent RF channels for 902-928 MHz band, 40 independent RF channels for 2.4 GHz band
- Gain imbalance compensation

4. Audio Modem

- ADPCM vocoder (ITU G.726 compliant)
- DTMF and ring tone generators
- OEM configurable alert tones
- Audio path and gain controls

5. Audio Codec

- Full ITU G.714-compliant standard voice frequency linear encoder/decoder
- Delta-sigma ADC/DAC with dynamic range >70 dB
- 8 kHz output sampling rate
- Differential microphone input with programmable gain and electret microphone bias generator
- Line input and output (600 Ω) for PSTN interfaces
- Differential speaker driver capable of 150 Ω loads
- Power-down modes

6. diSSTance Firmware

- Link establishment and maintenance protocols
- System state control logic
- Embedded transceiver control software for both 900 MHz and 2.4 GHz bands
- Audio and PSTN interfaces
- User-customizable phone control software
- OEM test mode
- Branch detect support
- OEM-selectable 40 kbps ADPCM or 32 kbps ADPCM with parity
- Fast Associated Control Channel (FACCH) – 20 kbps FDX with Automatic Repeat Request (ARQ)
- FCC Part 68 hearing aid compliance
- Programmable line echo suppressor
- Programmable audio gain table
- Link recovery for handset battery change

7. Power Requirements

- Single supply voltage, 2.7 – 5.25 V (ASIC & codec)
- Low active power consumption for 100-pin device, < 60 mW @ 3.6 V
- Super low-power standby mode for 100-pin device < 3 mW @ 3.6 V

8. Packages

- Hummingbird single-device ASIC/codec: 100-pin PQFP
- Hummingbird ASIC: 144-pin TQFP
- Hummingbird codec: 32-pin TQFP

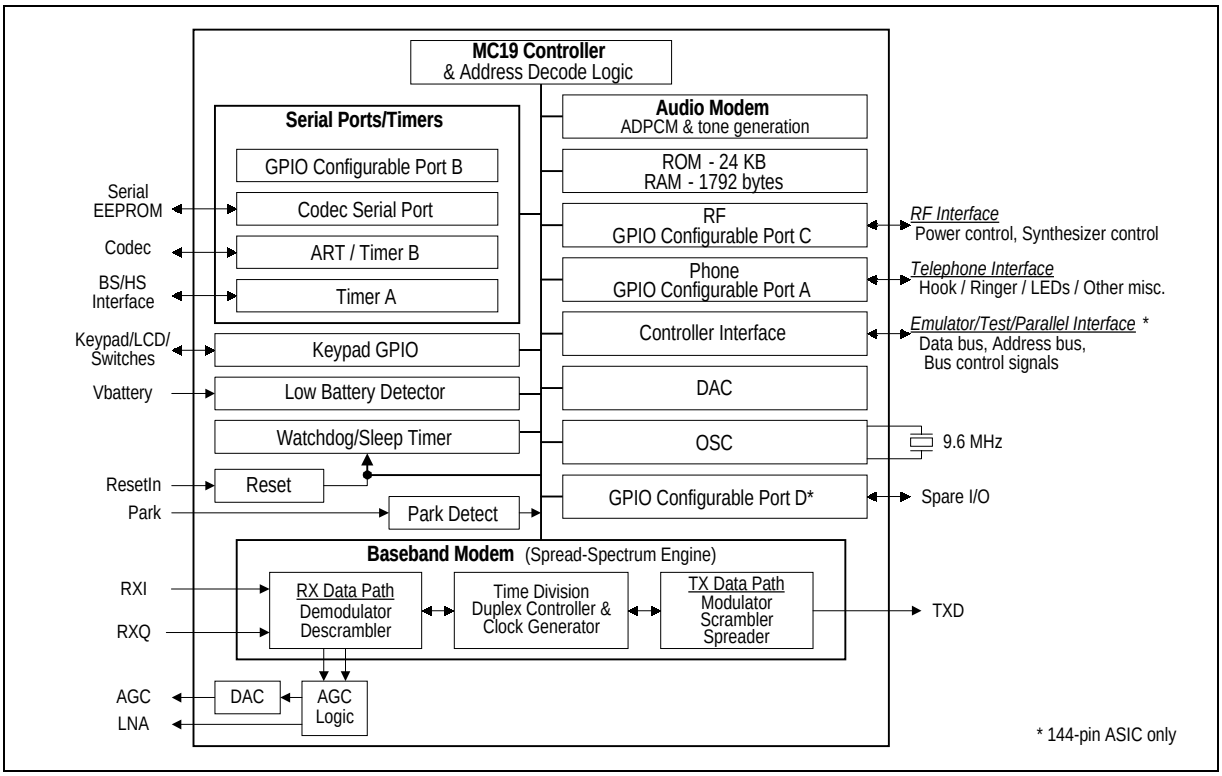


Figure 3. Hummingbird ASIC Block Diagram

Technical Overview

This section provides a technical description of how the Hummingbird diSSTance technology device set is used to handle all of the 900 MHz cordless phone features listed above. The device set is used both in the handset and the base station, as shown in Figure 1 and Figure 2.

System Controller

The system controller (Figure 3) handles all of the phone features, the DSS engine, the RF module settings, and the link between the base station and the handset.

The system controller provides a microcontroller with interrupt, wait-state, and system timer support. The system controller also provides General Purpose I/O (GPIO) and serial ports for peripheral control, a baseband modem (DSS engine) for signal processing of the received and transmitted data, and an audio modem for ADPCM conversion.

Microcontroller

The microcontroller is the 65C02-based MC19 CPU. It is supported by 1792 bytes of on-chip RAM and 24 KB of on-chip ROM. The CPU communicates via a 16-bit address/8-bit data bus and dedicated control lines.

Interrupt Controller

Interrupts are latched, prioritized, and passed to the microcontroller. Interrupts are used to interface with the codec, the DSS engine, serial ports and timers.

Wait State Generator

Slower access times for off-chip RAM and ROM are handled separately with programmable wait states. Off-chip reads/writes can be extended up to 7 clock cycles.

Watchdog/Sleep/Wake-up Timers

The timers perform two basic functions. The first is to provide a valid reset if the software malfunctions (watchdog). The second one is to minimize power consumption by keeping a low-frequency clock active to duty-cycle the system between normal mode and standby mode (sleep and wake-up timer).

Emulator/Test Interface

A standard 65C02-family parallel interface supports an external emulator for code development. ROM is mapped off-chip when operating with an emulator. Emulator functions are only provided with the 144-pin ASIC.

Peripheral Functions

Several peripheral phone functions are supported via the microcontroller registers or dedicated hardware.

General purpose timers are configured to provide the timing required for firmware execution. An asynchronous serial port and a dedicated codec serial port are also available. GPIOs are provided for peripheral control. Several GPIOs are dedicated to interface to peripherals such as the LEDs, keypad, LCD, RF control, serial EEPROM control, and external HDX speakerphone IC

control. GPIOs are also used as dedicated interfaces for phone functions such as ring detection and hook relay control.

General Purpose Timer A

Timer A is used for various firmware needs, such as link timing. It generates either single or continuous interrupts, and consists of an 8-bit interval register (TmrA) for the interval value, an 8-bit counter for generating the timer interrupt, and a divide-by-256 prescaler. Timer A uses the main 9.6 MHz clock divided by 256.

General Purpose Timer B

When operating as a timer, this logic functions almost identically to that of timer A. It has an 8-bit interval register (TmrB), a divide-by-5 prescaler, and an 8-bit counter.

Asynchronous Receiver/Transmitter (ART)

An asynchronous serial port with a programmable baud rate can be configured using timer B. The ART logic controls the two-pin asynchronous serial port of the ASIC. The ART port is used for base/handset data transfer, the test interface, and the CID detector device interface.

Keypad/Switch/LCD Interface

This interface is used to provide multiplexed control for a 4×8 keypad, up to 8 switches, and a parallel interface for an LCD (Figure 4). External diodes must be added to isolate the keys, switches, and LCD lines.

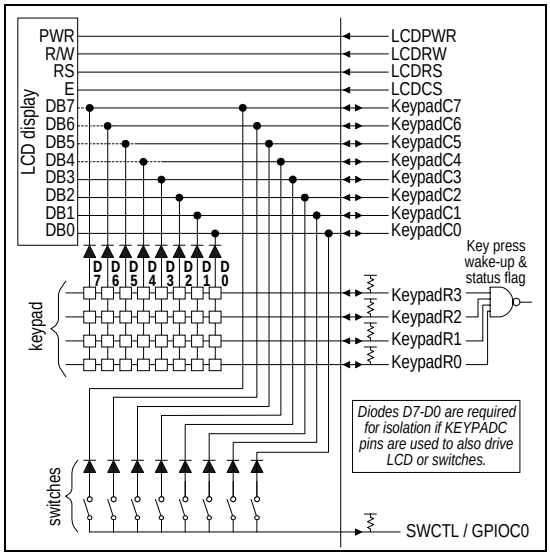


Figure 4. Keypad/Switch/LCD Interface

For a keypad interface, the eight KEYPADC[7:0] control signals are driven low, one at a time, and the four KEYPADR[3:0] inputs, with internal pull-up resistors, are read to see which key in the 32-key matrix is closed. The firmware scans the keypad at a 20ms interval and debounces the key presses.

For a switch interface, the eight KEYPADC[7:0] control signals are driven, one at a time, and GPIOC0, with an internal pull-up resistor, is read to determine if a switch is open or closed.

KEYPADC0 is used to select either 900 MHz or 2.4 GHz control. No connection between KEYPADC0 and SWCTL (GPIOC0) selects 900 MHz radio control. A diode connected between KEYPADC0 and SWCTL (GPIOC0) selects 2.4 GHz radio control.

An LCD interface can be implemented only with the 144-pin device and external ROM code. Figure 4 shows a recommended implementation. Keypad signals are used for the LCD data interface and GPIOs are used for the LCD control lines. The LCD driver and LCD management software must be written by the OEM.

Codec Serial Port

Digitized voice-band audio is supported through an interrupt-driven, 5-pin serial codec interface. Clock and frame timing for the codec are internally generated and externally fed to the device. The codec serial port interfaces to the Hummingbird codec. The codec serial port uses three memory-mapped locations for interfacing with the controller. They consist of high and low codec data bytes which are used to write out 16 bits of TX data and read 16 bits of RX data, and an 8-bit codec configuration/status register.

RF Transceiver Control

The ASIC allocates several GPIOs to control all necessary radio transceiver functions. Two pins control the PA output levels. Four pins make up the synthesizer serial port, clock data, strobe, and chip select. One pin is used as the LNA attenuation control and one pin is used for TR switch control. In addition, necessary enables for TX and RX are provided for power management control. The firmware protocol for programming the Conexant synthesizer in the RF105 and RF109, and the link parameter settings, are automatically configured with the selection of the 900 MHz or 2.4 GHz radio. The OEM can select the radio type using either the keypad switch control or OEM configuration settings in serial EEPROM or external ROM. If the radio type is selected using serial EEPROM or external ROM, the keypad switch radio type selection is overwritten. OEM configuration settings provide RF frequency band support for North America (20 channels at 902-928 MHz, 40 channels at 2400-2483.5 MHz), Australia (15 channels at 915-928 MHz), or New Zealand (7 channels at 921-929 MHz).

Battery Detector

This analog function performs A/D conversion on the battery voltage and makes it available to the microcontroller for battery quality estimation. External level shifting resistors set the input level to the ASIC. The low battery threshold can be set by the OEM in EEPROM.

General Purpose Inputs/Outputs (GPIOs)

24 GPIOs grouped into 3 ports (A, B, C) are available on the 100-pin device, and 26 GPIOs grouped into 4 ports (A,

B, C, D) are available on the 144-pin device. GPIOs are software bit-configurable as inputs or outputs. The embedded firmware uses some of the GPIOs as dedicated control signals for LED drivers, hook relay control, ring detection, RF control, CID device control, HDXSP device control, and serial EEPROM interface, depending on the system configuration. The GPIO assignments are specified in Table 1.

Caller ID Interface

The Hummingbird provides an interface to the Mitel MT8843 Calling Number Identification Circuit 2 device, configured to operate in MODE 0. The interface uses the ART serial port input to receive 1200 bps data, using the timing and logic of a standard RS-232 interface. GPIOA4 and GPIOA5 are used as discrete control I/O for the FSKEN and STD signals.

Ringer/Buzzer Control

A ringer/buzzer can be driven by either the codec LINEO, the ASIC AFC DAC, or a GPIO.

Baseband Modem

The baseband modem section of the Hummingbird ASIC performs all of the spread-spectrum modulation and demodulation, data timing recovery, AFC, AGC, framing, and rate adaptation required for a DSS system.

Transmit/Receive Data Paths

The transmit data path comprises a parallel-to-serial converter, scrambler, differential encoder, spreader, and modulator. The receive data path comprises analog-to-digital converters, matched filter with frequency compensation insertion, data demodulator, descrambler and serial-to-parallel converter.

Scrambler/Descrambler

The scrambler/descrambler is a 16-bit maximum length PN sequence generator. Its output is XOR'ed with TX data for scrambling and XOR'ed with RX data for descrambling. The voice and supervisory bits are scrambled. The PN sequence generator's starting location is programmable using one memory mapped register along with the two ID registers. This starting location is used to initialize the PN generator at the start of each link. The MSB of the PN generator is used to scramble/descramble. The first frame bit scrambled/descrambled uses the initialized value of the MSB. The scrambler/descrambler is enabled using the ScrambleEn bit of the TDDC configuration register.

Differential Encoder

When the differential encoder block is enabled, data is differentially encoded. The encoder is initialized to a zero during the TX frame's first "zero bit".

In DBPSK, a data symbol is inferred by the presence or absence of a 180° phase shift or inversion in the carrier signal at regular intervals. A phase shift thus indicates a change of state, from one to zero, or zero to one. To provide a means of determining which of these two possibilities was the intended one, the spread data is differentially encoded.

Spread Spectrum Spreader

A 12-chip spreading code is used to meet FCC part 15.247 requirements for a DSS system. The spreading code cyclic duration is 12 times that of the encoded data. The code starts and stops on encoded bit boundaries. The spreading code may be configured by the controller.

Modulation

The data from the differential encoder is input to the modulator. An analog block exists at the TX output which will maintain a constant voltage level independent of supply operation.

Receiver A/D Converters

Baseband I/Q signals from the radio are sampled at 1.92 MHz and converted to digital with 3-bit flash A/D converters.

AFC/Timing

Internal automatic frequency control (AFC) allows crystal tolerance of up to ±80 ppm for 900 MHz radio or 40 ppm for 2.4 GHz radio. This allows for a total system clock error of 160 ppm for 900 MHz radio or 80 ppm for 2.4 GHz radio. The modem uses a standard early-late mechanism to maintain timing locks.

Matched Filters

The spreading code is removed (despread) from the received digitized I/Q signals with matched filters.

Data Demodulation

This block determines the value for the received bit and determines a frequency error estimate that is used for the AFC. Data is demodulated by using I/Q matched filter data which is exactly 1 bit time apart.

Signal Quality

A signal quality metric is accumulated over each frame, and can be read by the microcontroller at any time.

AGC and Gain Imbalance

The signal energy is compared to a programmable threshold and scaled with programmable gain. The digital AGC value is output to the radio by an 8-bit D/A converter. The gain imbalance of the I/Q system is automatically calculated and removed during calibration of the system.

ID Detector

A 32-bit ID word (16-bit programmable) is used during acquisition to verify the RF link and initialize frame timing.

Time Division Duplex Controller

The Time Division Duplex Controller (TDDC) handles the spread spectrum protocol.

Table 1. GPIO Assignments for Handset and Base Station Configurations

GPIO	Handset	Base Station with (note 1)		
		CID	SP	CID, SP
A0	Phone LED	Phone LED	Phone LED	Phone LED
A1	Page/NewCall LED	New Call LED	Page/Intcom LED	NewCall LED
A2	LowBat LED	Mute/Hold LED	Mute/Hold LED	Mute/Hold LED
A3	Remote LED	Page/Intcom LED	LED4	Page/Intcom LED
A4	Key LED	Mitel FSKEN	Not assigned	Mitel FSKEN
A5	LED6	Mitel STD	Not assigned	Mitel STD
A6	Aud_Pwr/Ringer	OHP	OHP	OHP
A7	RingOn/Off	RIP/BRANCHP	RIP/BRANCHP	RIP/BRANCHP
B0 (note 2, 3)	a. NVCS b. I2C_DATA	a. NVCS b. I2C_DATA	a. NVCS b. I2C_DATA	a. NVCS b. I2C_DATA
B1 (note 2)	a. NVCLK b. I2C_CLK	a. NVCLK b. I2C_CLK	a. NVCLK b. I2C_CLK c. EEPOT_INC	a. NVCLK b. I2C_CLK c. EEPOT_INC
B2 (note 2)	NVDI	NVDI	a. NVDI c. EEPOT_U/D	a. NVDI c. EEPOT_U/D
B3	NVDO	NVDO	NVDO	NVDO
B4	Not assigned	Not assigned	SPEN	SPEN
B5 (note 4)	Not assigned	Not assigned	SPMUTE	SPMUTE
B6	Not assigned	Not assigned	EEPOT_CS	EEPOT_CS
B7	Not assigned	Not assigned	Not assigned	Not assigned
C0	SWCTL	SWCTL	SWCTL	SWCTL
C1	LNAATN	LNAATN	LNAATN	LNAATN
C2	TXPWR0	TXPWR0	TXPWR0	TXPWR0
C3	TXPWR1	TXPWR1	TXPWR1	TXPWR1
C4	SYNEN	SYNEN	SYNEN	SYNEN
C5	SYNSTB	SYNSTB	SYNSTB	SYNSTB
C6	SYNDATA	SYNDATA	SYNDATA	SYNDATA
C7	SYNCLK	SYNCLK	SYNCLK	SYNCLK
D0 (note 5)	Not assigned	Not assigned	Not assigned	Not assigned
D1 (note 5)	Not assigned	Not assigned	Not assigned	Not assigned

Notes:
1. CID = Caller ID; SP = speakerphone
2. Either a, b, or c applies, depending on the application, as follows:
   a. MICROWIRE serial EEPROM
   b. I^2C serial EEPROM
   c. Digital potentiometer for speakerphone volume control
3. A pull-up resistor on GPIOB0 selects I^2C serial EEPROM. A pull-down resistor on GPIOB0 selects MICROWIRE serial EEPROM.
4. On GPIOB5: a pull-up resistor selects base station configuration; a pull-down resistor selects handset configuration.
5. 144-pin package only.

Clock Oscillator

An efficient 9.6 MHz crystal oscillator generates the system reference clock and is also used for standby operations: sleep, wake-up, and watchdog functions.

Audio Modem

The audio modem is a coprocessor connected to the microcontroller via the data bus and memory mapped registers. Its functions are to convert ADPCM data to/from 16-bit linear codec data, and to generate tones that can be added to the voice or sent out with muted voice.

The controller interfaces with the audio modem through the audio engine's register file. The controller only has access to these registers while the audio engine is in sleep mode. A second interface is through the audio engine control register, which the controller can read or write at any time.

The audio engine has 16-bit registers while the controller has only an 8-bit wide bus. When the controller reads the audio engine, the LSB of the address word will be used to multiplex out the proper memory mapped byte for the 16 LSBs of the register file. The 8-bit wide bus from the controller will be used for interfacing to the audio engine.

ADPCM Coder

The ADPCM Coder is the audio engine's main block. This block performs the processing that encodes linear speech data, passes it to the radio as ADPCM compressed speech, and decodes ADPCM data received from the radio into linear speech data. One of the audio engine registers is the data interface to this function.

The audio engine reads nibbles to decode from this register, and writes encoded values to this register. Using the ITU G.726 40 kbps or 32 kbps ADPCM audio compression algorithm, 14-bit linear samples are compressed to 5 or 4 bits at an 8k sample rate.

Another audio engine register is used as the codec interface. When the audio engine completes processing, the 16-bit linear data word to be output to the D/A is in this register. This same register must be written with the 16-bit linear speech data received from the A/D before the audio engine begins processing.

Dual Tone Generator

The audio modem also contains the tone generator. The TONE1 and TONE2 blocks are two signal generators that make sine waves. These tone generators are used to create DTMF signaling as required by the phone system. Also, miscellaneous acknowledge beeps or tones are created using this portion of the system.

Audio Codec

The audio codec is a monolithic CMOS integrated circuit. It is packaged with the ASIC into a single 100-pin device. It consists of an A/D and D/A converter path, with digital filtering and analog signal processing circuits to realize a complete ITU G.714-compatible voice frequency linear coder/decoder. The user word rate to and from the device is 8k words per second (Figure 5).

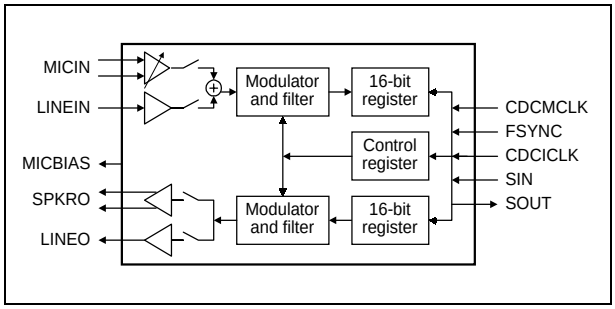


Figure 5. Hummingbird Codec Block Diagram

ASIC Interface Port

Six interface lines are used to link the audio codec and ASIC. Two lines are utilized for clocks (CDCMCLK and CDCICLK) and a third creates an 8 kHz framing pulse. The remaining lines are for data in and data out lines as well as a reset line. The clocks and framing pulse are synchronous to each other. The data I/O port will be time-multiplexed between data and control words.

Microphone Input

The microphone input is a differential input to reduce common mode noise pickup. An electret microphone may be AC-coupled into the MICINP and MICINN inputs. The microphone can be biased from the supplied MICBIAS source, which provides a quiet, clean reference as required by electret microphones. Programmable gains of 30, 25, 20, or 0 dB allow customizing microphones of various types of sensitivity. This input is summed with the line input signal, prior to the A/D conversion.

Line Input

An auxiliary input is provided for use as an alternative analog interface. This interface can be used to interface the base station codec to the PSTN. This input is summed with the microphone input signal.

Speaker Output

The SPKPO and SPKMO signals form a differential output capable of driving a 150 Ω resistive load or a highly capacitive (100 nF) ceramic receiver via dual 150 Ω series resistors. This output is used to drive either the PSTN or the earpiece on the handset.

Line Output

LINEO is a single-ended output capable of driving a 350 Ω load.

Electrostatic Discharge (ESD) Sensitivity

All Hummingbird devices (100-pin ASIC/codec, 144-pin ASIC, 32-pin codec) are static-sensitive electronic devices. Do not operate or store near strong electrostatic fields. Take proper ESD precautions.

Hardware Interface Description

Hardware interface diagrams of a sample system design using the 100-pin package and the 144-pin package are shown in Figure 6 and Figure 7, respectively.

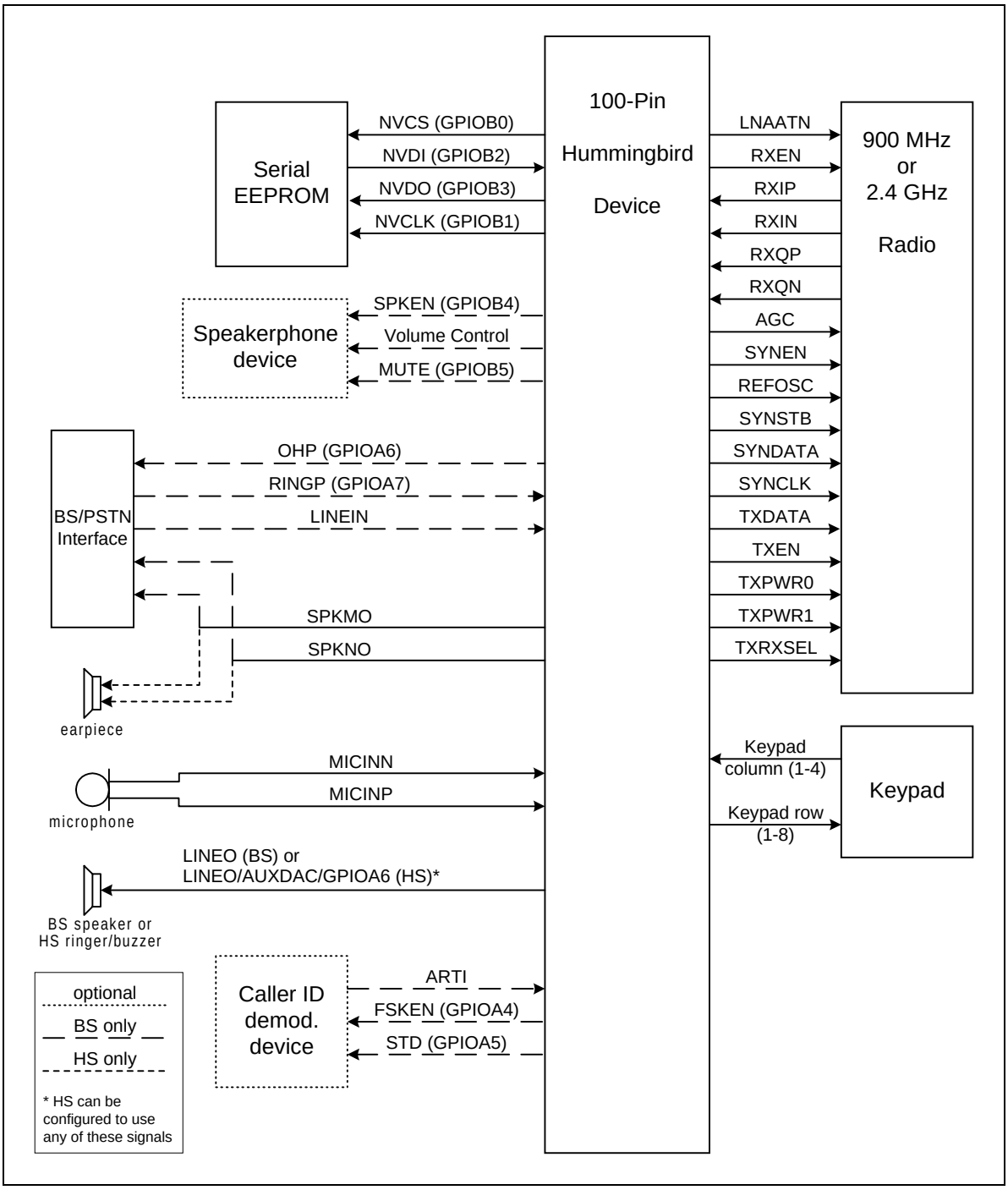


Figure 6. System Block Diagram for 100-pin Hummingbird Device

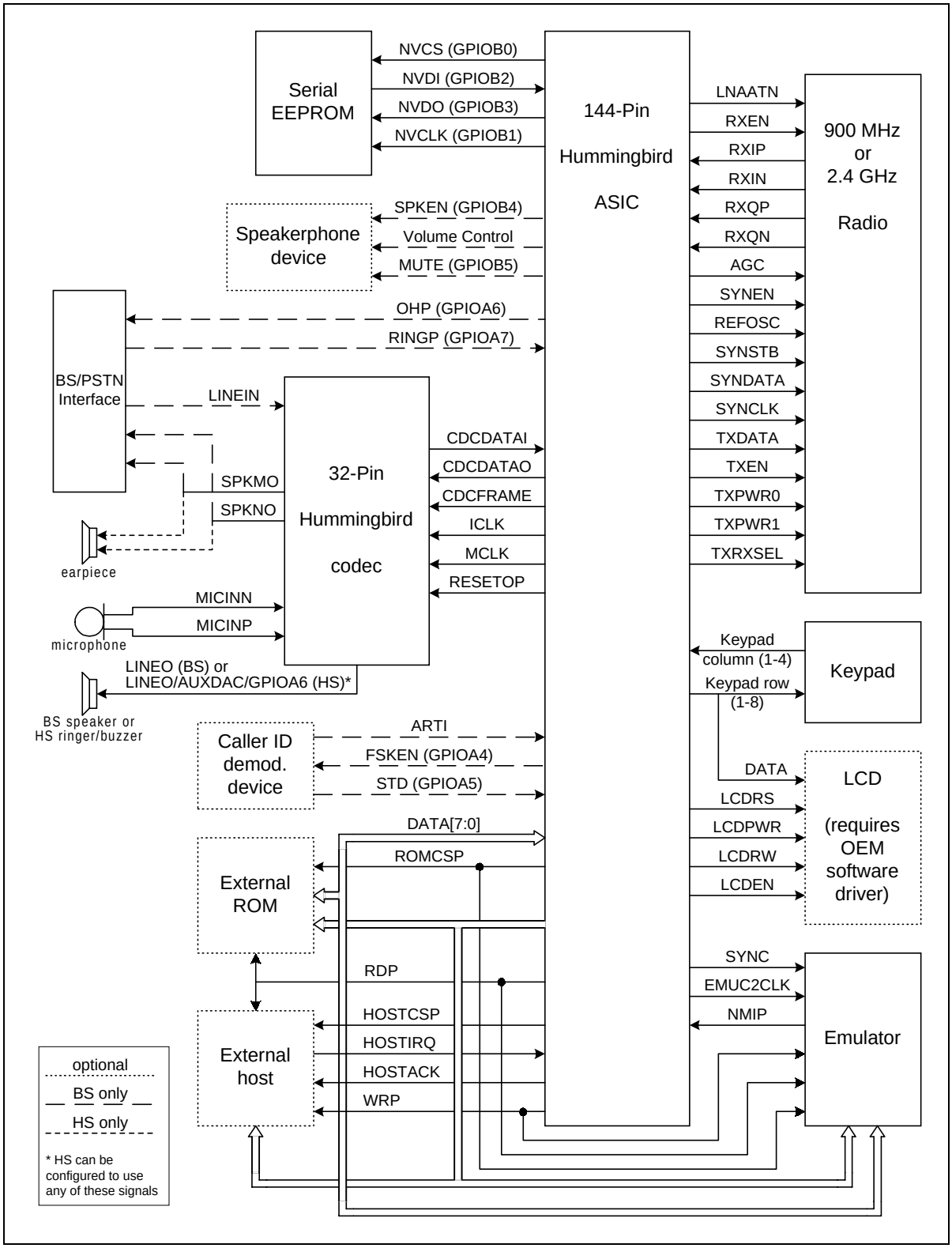


Figure 7. System Block Diagram for 144-pin Hummingbird Device

Hardware Interface Description

The Hummingbird single-device ASIC/codec is available in a 100-pin PQFP.

A pin assignment diagram for the single-device ASIC/codec is shown in Figure 8. The signals for this device are described in detail by functional group in Table 2.

For custom OEM designs, the Hummingbird ASIC and codec are available separately, with the ASIC in a 144-pin TQFP, and the codec in a 32-pin TQFP.

The 144-pin ASIC pin assignment diagram is shown in Figure 9. The 144-pin ASIC signals are described in detail by functional group in Table 3. The 32-pin codec pin assignment diagram is shown in Figure 10. The 32-pin codec signals are described in detail in Table 4.

Single-Device ASIC/Codec Signal Description

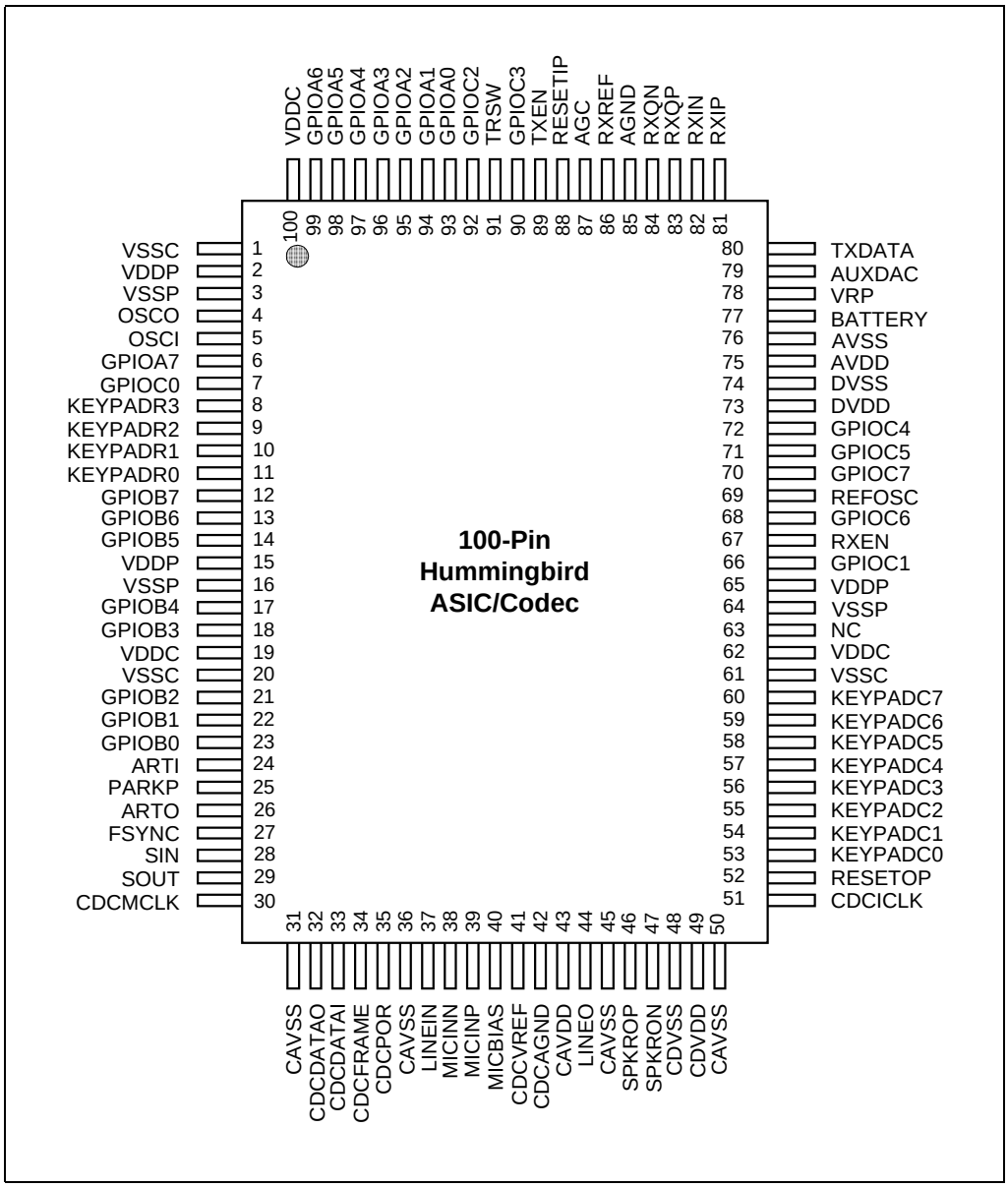


Figure 8. Pin Assignments – Hummingbird 100-Pin ASIC/Codec

Table 2. Hummingbird Signal Description – 100-pin ASIC/Codec (1 of 3)

Pin No.	Pin Name	Type (Note 1)	Description
RF Interface			
69	REFOSC	B4	9.6 MHz clock used by synthesizer.
82	RXIN	I-A	Receiver I negative differential input.
81	RXIP	I-A	Receiver I positive differential input.
84	RXQN	I-A	Receiver Q negative differential input.
83	RXQP	I-A	Receiver Q positive differential input.
86	RXREF	B-A	Receiver ADC reference.
80	TXDATA	O-A	Transmitter data.
87	AGC	O-A	AGC control.
91	TRSW	O4	Transmit=1/receive=0 select.
89	TXEN	O4	Transmit enable.
67	RXEN	O4	Receive enable.
66	GPIOC1/LNAATN	O4	LNA select.
92	GPIOC2/TXPWR0	O4	PA power level select.
90	GPIOC3/TXPWR1	O4	PA power level select.
72	GPIOC4/SYNEN	O2	Synthesizer power.
71	GPIOC5/SYNSTB	O2	Synthesizer strobe.
68	GPIOC6/SYNDATA	O2	Synthesizer data.
70	GPIOC7/SYNCLK	O2	Synthesizer clock.
Codec Interface			
27	FSYNC	B4	Frame sync.
28	SIN	I	Serial data input.
29	SOUT	O	Serial data output.
30	CDCMCLK	I	Main clock input
31	CAVSS	I-A	Analog 0V power supply.
32	CDCDATAO	B2	Codec data output.
33	CDCDATAI	I-PDN	Codec data input.
34	CDCFRAME	T-PDN	Codec frame.
35	CDCPOR	I	Reset input, active low.
36	CAVSS	I-A	Analog 0V power supply.
37	LINEIN	I-A	Analog input to line pre-amp, ADC channel.
38	MICINN	I-A	Negative differential analog input to microphone pre-amp, ADC channel.
39	MICINP	I-A	Positive differential analog input to microphone pre-amp, ADC channel.
40	MICBIAS	O-A	2.2V nominal DC bias source for electret microphone.
41	CDCVREF	O-A	Analog reference voltage output. Bypass to AVSS with 0.1µF capacitor.
42	CDCAGND	O-A	Analog ground bias output. Bypass to AVSS with 0.1µF capacitor.
43	CAVDD	I-A	Analog power supply.
44	LINEO	O-A	Line driver output, DAC channel.
45	CAVSS	I-A	Analog 0V power supply.
46	SPKROP	O-A	Positive speaker driver output, DAC channel.
47	SPKRON	O-A	Negative speaker driver output, DAC channel.
48	CDVSS	I	Digital 0V power supply.
49	CDVDD	I	Digital power supply, 2.7-5.5 Volts.
50	CAVSS	I-A	Analog 0V power supply.
51	CDCICLK	I	Bit clock input/output for digital serial interface.
62	RESETOP	O4	Codec reset.

Table 2. Hummingbird Signal Description – 100-pin ASIC/Codec (2 of 3)

Pin No.	Pin Name	Type (Note 1)	Description
GPIO Interface			
93	GPIOA0	B4	General purpose I/O.
94	GPIOA1	B4	General purpose I/O.
95	GPIOA2	B4	General purpose I/O.
96	GPIOA3	B4	General purpose I/O.
97	GPIOA4	B4	General purpose I/O.
98	GPIOA5	B4	General purpose I/O.
99	GPIOA6	B4	General purpose I/O.
6	GPIOA7	B4	General purpose I/O.
23	GPIOB0	B4	General purpose I/O.
22	GPIOB1	B4	General purpose I/O.
21	GPIOB2	B4	General purpose I/O.
18	GPIOB3	B4	General purpose I/O.
17	GPIOB4	B4	General purpose I/O.
14	GPIOB5	B4	General purpose I/O.
13	GPIOB6	B4	General purpose I/O.
12	GPIOB7	B4	General purpose I/O.
7	GPIOC0/SWCTL	B4-PUP	General purpose I/O. Switch control read input.
Keypad Interface			
53	KEYPADC0	BIS	Keypad bidirectional control.
54	KEYPADC1	BIS	Keypad bidirectional control.
55	KEYPADC2	BIS	Keypad bidirectional control.
56	KEYPADC3	BIS	Keypad bidirectional control.
57	KEYPADC4	BIS	Keypad bidirectional control.
58	KEYPADC5	BIS	Keypad bidirectional control.
59	KEYPADC6	BIS	Keypad bidirectional control.
60	KEYPADC7	BIS	Keypad bidirectional control.
11	KEYPADR0	BIS-PUP	Keypad read input.
10	KEYPADR1	BIS-PUP	Keypad read input.
9	KEYPADR2	BIS-PUP	Keypad read input.
8	KEYPADR3	BIS-PUP	Keypad read input.
Phone Interface			
25	PARKP	IS	Park input; active low on base station, active high on handset
Analog Support			
78	VRP	O-A	Analog voltage reference output.
85	AGND	O-A	Analog ground.

Table 2. Hummingbird Signal Description – 100-pin ASIC/Codec (3 of 3)

Pin No.	Pin Name	Type (Note 1)	Description
Miscellaneous			
26	ARTO	O-OD-PUP	ART output.
24	ARTI	I-PUP	ART input.
79	AUXDAC	O-A	AFC DAC output.
88	RESETIP	I-PUP	Power-on reset RC input; active low.
5	OSCI	I	9.6 MHz crystal oscillator input.
4	OSCO	O4	9.6 MHz crystal oscillator output.
77	BATTERY	I-A	Battery voltage input.
63	NC (Note 2)		
Supply Pins			
2	VDDP	VDD	VDD supply to pad ring.
15	VDDP	VDD	VDD supply to pad ring.
65	VDDP	VDD	VDD supply to pad ring.
3	VSSP	VDD	VSS supply to pad ring.
16	VSSP	VSS	VSS supply to pad ring.
64	VSSP	VSS	VSS supply to pad ring.
19	VDDC	VDD	VDD supply to core.
62	VDDC	VDD	VDD supply to core.
100	VDDC	VDD	VDD supply to core.
1	VSSC	VSS	VSS supply to core.
20	VSSC	VSS	VSS supply to core.
61	VSSC	VSS	VSS supply to core.
73	DVDD	VDD-D	VDD supply to A/D converters.
74	DVSS	VSS-D	VSS supply to A/D converters.
75	AVDD	VDD-A	VDD supply to analog.
76	AVSS	VSS-A	VSS supply to analog.

Notes:

1. Pin type:

B2	Digital	Bidirectional: 2 mA driver and CMOS receiver
B4	Digital	Bidirectional: 4 mA driver and CMOS receiver
B4-PUP	Digital	Bidirectional: 4 mA driver and CMOS receiver with pull-up
BIS	Digital	Bidirectional: 4 mA driver and CMOS Schmitt receiver
BIS-PUP	Digital	Bidirectional: 4 mA driver with pull-up and CMOS Schmitt receiver
B-A	Analog	Bidirectional: Analog receiver/driver
B-PUP	Digital	Bidirectional: 2 mA driver with pull-up and CMOS receiver
I	Digital	Input: CMOS receiver
I-A	Analog	Input: Analog receiver
I-PDN	Digital	Input: CMOS receiver with pull-down
I-PUP	Digital	Input: CMOS receiver with pull-up
IS	Digital	Input: CMOS Schmitt receiver
IS-PDN	Digital	Input: CMOS Schmitt receiver with pull-down
IS-PUP	Digital	Input: CMOS Schmitt receiver with pull-up
O	Digital	Output: 4 mA driver
O2	Digital	Output: 2 mA driver
O4	Digital	Output: 4 mA driver
O-A	Analog	Output: Analog driver
O-OD-PUP	Digital	Output: Open drain with pull-up
T	Digital	Tristate: 2 mA driver
T-PDN	Digital	Tristate: 2 mA driver with pull-down
T-PUP	Digital	Tristate: 4 mA driver with pull-up

2. Do not connect (for Conexant use only).

144-pin ASIC Signal Description

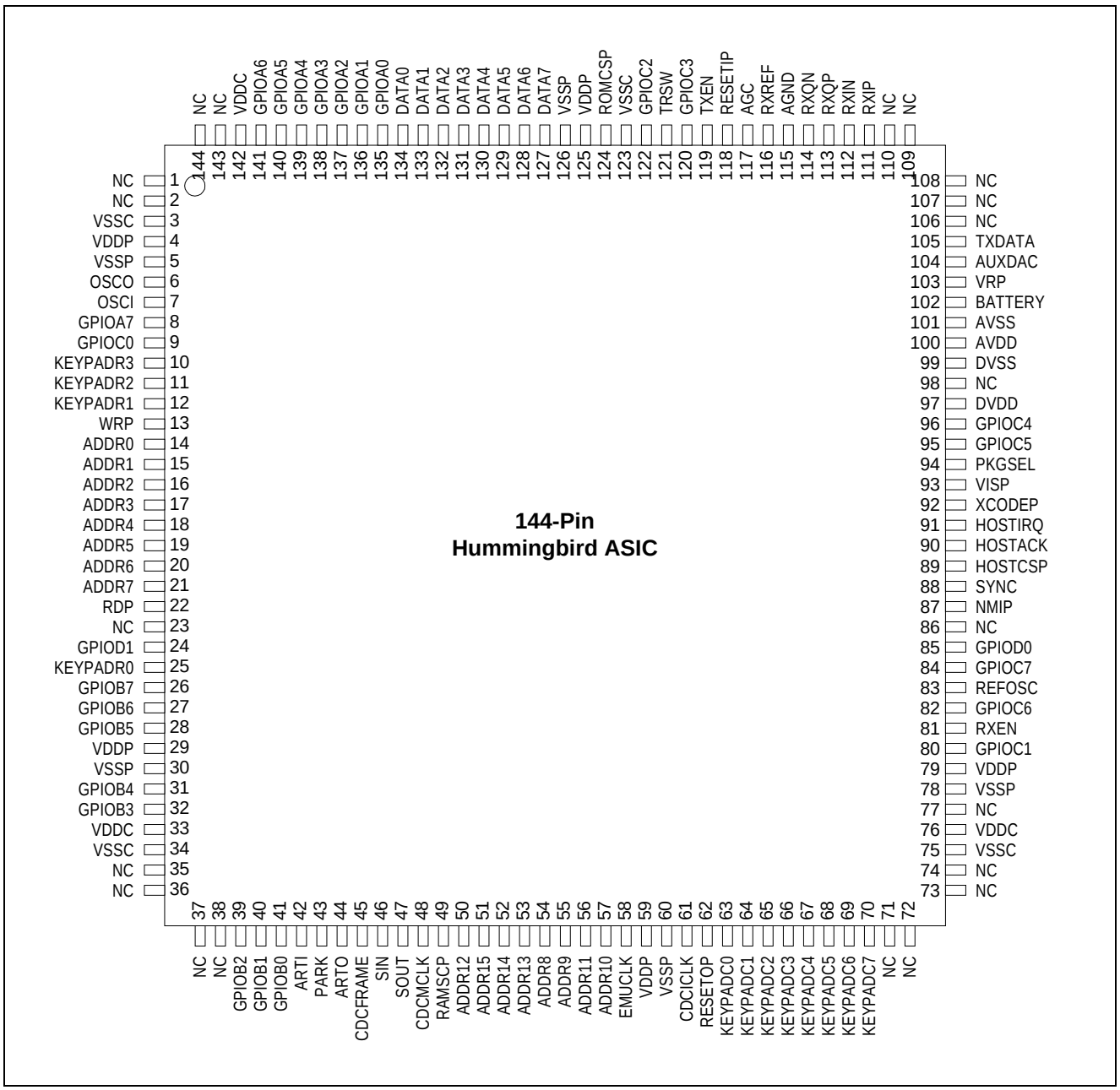


Figure 9. Pin Assignments – Hummingbird 144-Pin ASIC

Table 3. Signal Description – 144-pin ASIC (1 of 4)

Pin No.	Pin Name	Type (Note 1)	Description
Controller Interface			
134	DATA0	B-PUP	Data bit 0.
133	DATA1	B-PUP	Data bit 1.
132	DATA2	B-PUP	Data bit 2.
131	DATA3	B-PUP	Data bit 3.
130	DATA4	B-PUP	Data bit 4.
129	DATA5	B-PUP	Data bit 5.
128	DATA6	B-PUP	Data bit 6.
127	DATA7	B-PUP	Data bit 7.
14	ADDR0	T	Address bit 0.
15	ADDR1	T	Address bit 1.
16	ADDR2	T	Address bit 2.
17	ADDR3	T	Address bit 3.
18	ADDR4	T	Address bit 4.
19	ADDR5	T	Address bit 5.
20	ADDR6	T	Address bit 6.
21	ADDR7	T	Address bit 7.
54	ADDR8	T	Address bit 8.
55	ADDR9	T	Address bit 9.
57	ADDR10	T	Address bit 10.
56	ADDR11	T	Address bit 11.
50	ADDR12	T	Address bit 12.
53	ADDR13	T	Address bit 13.
52	ADDR14	T	Address bit 14.
51	ADDR15	T	Address bit 15.
13	WRP	T	Write; active low.
22	RDP	T	Read; active low.
124	ROMCSP	O2	ROM chip select; active low.
49	RAMCSP	O2	RAM chip select; active low.
89	HOSTCSP	O2	Host chip select; active low.
91	HOSTIRQ	O2	Host interrupt.
90	HOSTACK	IS-PDN	Host input acknowledge.
88	SYNC	O2	Synchronize, CPU fetching OP code.
87	NMIP	IS-PUP	Non-maskable interrupt; active low.
94	PKGSEL	I-PUP	Package configuration select; tie low.
92	XCODEP	I-PUP	Emulator select; active low.
58	EMUCLK	O2	Phase 2 clock output from MC19.

Table 3. Signal Description – 144-pin ASIC (2 of 4)

Pin No.	Pin Name	Type (Note 1)	Description
RF Interface			
83	REFOSC	B4	9.6 MHz clock used by synthesizer.
112	RXIN	I-A	Receiver I negative differential input.
111	RXIP	I-A	Receiver I positive differential input.
114	RXQN	I-A	Receiver Q negative differential input.
113	RXQP	I-A	Receiver Q positive differential input.
116	RXREF	B-A	Receiver ADC reference.
105	TXDATA	O-A	Transmitter data.
117	AGC	O-A	AGC control.
121	TRSW	O4	Transmit=1/receive=0 select.
119	TXEN	O4	Transmit enable.
81	RXEN	O4	Receive enable.
80	GPIOC1/LNAATN	O4	LNA select.
122	GPIOC2/TXPWR0	O4	PA power level select.
120	GPIOC3/TXPWR1	O4	PA power level select.
96	GPIOC4/SYNEN	O2	Synthesizer power.
95	GPIOC5/SYNSTB	O2	Synthesizer strobe.
82	GPIOC6/SYNDATA	O2	Synthesizer data.
84	GPIOC7/SYNCLK	O2	Synthesizer clock.
Codec Interface			
47	CDCDATAO	B2	Codec data output.
46	CDCDATAI	I-PDN	Codec data input.
45	CDCFRAME	T-PDN	Codec frame.
61	ICLK	T-PDN	Codec serial port clock.
48	MCLK	T-PDN	Codec clock.
62	RESETOP	O4	Codec reset.
GPIO Interface			
135	GPIOA0	B4	General purpose I/O.
136	GPIOA1	B4	General purpose I/O.
137	GPIOA2	B4	General purpose I/O.
138	GPIOA3	B4	General purpose I/O.
139	GPIOA4	B4	General purpose I/O.
140	GPIOA5	B4	General purpose I/O.
141	GPIOA6	B4	General purpose I/O.
8	GPIOA7	B4	General purpose I/O.
41	GPIOB0	B4	General purpose I/O.
40	GPIOB1	B4	General purpose I/O.
39	GPIOB2	B4	General purpose I/O.
32	GPIOB3	B4	General purpose I/O.
31	GPIOB4	B4	General purpose I/O.
28	GPIOB5	B4	General purpose I/O.
27	GPIOB6	B4	General purpose I/O.
26	GPIOB7	B4	General purpose I/O.
9	GPIOC0/SWCTL	B4-PUP	General purpose I/O. Switch control read input.
85	GPIOD0	B4	General purpose I/O.
24	GPIOD1	B4	General purpose I/O.

Table 3. Signal Description – 144-pin ASIC (3 of 4)

Pin No.	Pin Name	Type (Note 1)	Description
Keypad Interface			
63	KEYPADC0	BIS	Keypad bidirectional control.
64	KEYPADC1	BIS	Keypad bidirectional control.
65	KEYPADC2	BIS	Keypad bidirectional control.
66	KEYPADC3	BIS	Keypad bidirectional control.
67	KEYPADC4	BIS	Keypad bidirectional control.
68	KEYPADC5	BIS	Keypad bidirectional control.
69	KEYPADC6	BIS	Keypad bidirectional control.
70	KEYPADC7	BIS	Keypad bidirectional control.
25	KEYPADR0	BIS-PUP	Keypad read input.
12	KEYPADR1	BIS-PUP	Keypad read input.
11	KEYPADR2	BIS-PUP	Keypad read input.
10	KEYPADR3	BIS-PUP	Keypad read input.
Phone Interface			
43	PARKP	IS	Park input; active low on base station, active high on handset.
Analog Support			
103	VRP	O-A	Analog voltage reference output.
115	AGND	O-A	Analog ground.
Miscellaneous			
44	ARTO	O-OD-PUP	ART output.
42	ARTI	I-PUP	ART input.
104	AUXDAC	O-A	AFC DAC output.
118	RESETIP	I-PUP	Power-on reset RC input; active low.
7	OSCI	I	9.6 MHz crystal oscillator input.
6	OSCO	O4	9.6 MHz crystal oscillator output.
102	BATTERY	I-A	Battery voltage input.
77	NC (Note 2)		
93	VISP	I-PUP	Visibility mode select; active low.
1-2	NC (Note 2)		
23	NC (Note 2)		
35-38	NC (Note 2)		
71-74	NC (Note 2)		
86	NC (Note 2)		
98	NC (Note 2)		
106-110	NC (Note 2)		
143-144	NC (Note 2)		

Table 3. Signal Description – 144-pin ASIC (4 of 4)

Pin No.	Pin Name	Type (Note 1)	Description
Supply Pins			
4	VDDP	VDD	VDD supply to pad ring.
29	VDDP	VDD	VDD supply to pad ring.
59	VDDP	VDD	VDD supply to pad ring.
79	VDDP	VDD	VDD supply to pad ring.
125	VDDP	VDD	VDD supply to pad ring.
5	VSSP	VSS	VSS supply to pad ring.
30	VSSP	VSS	VSS supply to pad ring.
60	VSSP	VSS	VSS supply to pad ring.
78	VSSP	VSS	VSS supply to pad ring.
126	VSSP	VSS	VSS supply to pad ring.
33	VDDC	VDD	VDD supply to core.
76	VDDC	VDD	VDD supply to core.
142	VDDC	VDD	VDD supply to core.
3	VSSC	VSS	VSS supply to core.
34	VSSC	VSS	VSS supply to core.
75	VSSC	VSS	VSS supply to core.
123	VSSC	VSS	VSS supply to core.
97	DVDD	VDD-D	VDD supply to A/D converters.
99	DVSS	VSS-D	VSS supply to A/D converters.
100	AVDD	VDD-A	VDD supply to analog.
101	AVSS	VSS-A	VSS supply to analog.

Notes:

1. Pin type:

B2	Digital	Bidirectional: 2 mA driver and CMOS receiver
B4	Digital	Bidirectional: 4 mA driver and CMOS receiver
B4-PUP	Digital	Bidirectional: 4 mA driver and CMOS receiver with pull-up
BIS	Digital	Bidirectional: 4 mA driver and CMOS Schmitt receiver
BIS-PUP	Digital	Bidirectional: 4 mA driver with pull-up and CMOS Schmitt receiver
B-A	Analog	Bidirectional: Analog receiver/driver
B-PUP	Digital	Bidirectional: 2 mA driver with pull-up and CMOS receiver
I	Digital	Input: CMOS receiver
IS	Digital	Input: CMOS Schmitt receiver
IS-PDN	Digital	Input: CMOS Schmitt receiver with pull-down
IS-PUP	Digital	Input: CMOS Schmitt receiver with pull-up
I-A	Analog	Input: Analog receiver
I-PDN	Digital	Input: CMOS receiver with pull-down
I-PUP	Digital	Input: CMOS receiver with pull-up
O	Digital	Output: 4 mA driver
O2	Digital	Output: 2 mA driver
O4	Digital	Output: 4 mA driver
O-A	Analog	Output: Analog driver
O-OD-PUP	Digital	Output: Open drain with pull-up
T	Digital	Tristate: 2 mA driver
T-PDN	Digital	Tristate: 2 mA driver with pull-down
T-PUP	Digital	Tristate: 4 mA driver with pull-up

2. Do not connect (for Conexant use only).

32-pin Codec Signal Description

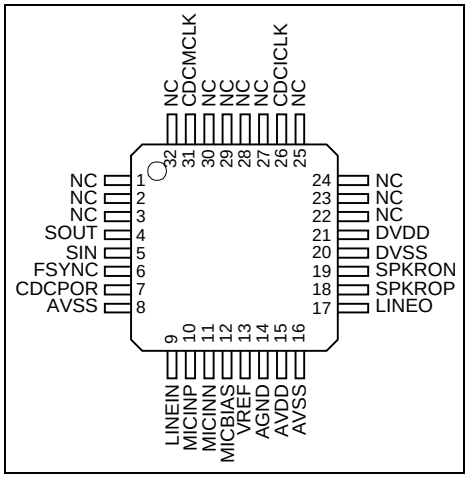


Figure 10. Pin Assignments – Hummingbird 32-Pin Codec

Table 4. Signal Description – 32-pin Codec

Pin #	Pin Name	Type (Note 1)	Description
1-3	NC		No connect
4	SOUT	O	Serial data output.
5	SIN	I	Serial data input.
6	FSYNC	I/O	Frame sync.
7	CDCPOR	I	Reset input, active low.
8	AVSS	I	Analog 0V power supply.
9	LINEIN	I-A	Analog input to line pre-amp, ADC channel.
10	MICINP	I-A	Positive differential analog input to microphone pre-amp, ADC channel.
11	MICINN	I-A	Negative differential analog input to microphone pre-amp, ADC channel.
12	MICBIAS	O-A	2.2V nominal DC bias source for electret microphone.
13	VREF	O-A	Analog reference voltage output. Bypass to AVSS with 0.1µF capacitor.
14	AGND	O-A	Analog ground bias output. Bypass to AVSS with 0.1µF capacitor.
15	AVDD	I-A	Analog power supply.
16	AVSS	I-A	Analog 0V power supply.
17	LINEO	O-A	Line driver output, DAC channel.
18	SPKROP	O-A	Positive speaker driver output, DAC channel.
19	SPKRON	O-A	Negative speaker driver output, DAC channel.
20	DVSS	I	Digital 0V power supply.
21	DVDD	I	Digital power supply, 2.7-5.5 Volts.
22-25	NC		No connect
26	CDCICLK	I	Bit clock input/output for digital serial interface.
27-30	NC		No connect
31	CDCMCLK	I	Main clock input
32	NC		No connect

Notes:
1. Pin Type:

I	Digital	Input: CMOS receiver
O	Digital	Output: 4 mA driver
I-A	Analog	Input: Analog receiver
O-A	Analog	Output: Analog driver

Firmware Interface Description

General Overview

The Hummingbird device set contains embedded code for the full functionality of a 900 MHz or 2.4 GHz digital cordless telephone. In addition, the customer can modify and customize the software to add unique phone features/functions. The software includes base station to handset link protocols, embedded transceiver control, and phone functions.

ASIC Firmware Interface

The following is an overview of the firmware interface built into the ASIC for development of the digital cordless phone.

Controller Interfaces

The microcontroller communicates with on-chip and off-chip hardware functions via a mapped memory interface. The microcontroller uses its 8-bit parallel bus to read and write interface memory.

24 KB of on-chip code is mapped to address space $A000-$FFFF. 20 KB of off-chip code is mapped to address space $5000-$9FFF. ROMCSP is used as the external memory chip select for off-chip code. 16 KB of off-chip data is mapped to address space $1000-$4FFF. RAMCSP is used as the external data memory chip select for off-chip data.

When operating with an emulator (XCODEP pin active), the 24 KB of on-chip program ROM ($A000-$FFFF) are bypassed to emulator memory or off-chip ROM. This emulator mode is only available with the 144-pin package.

Memory Map

Details of the ASIC interface memory map are provided in Table 6. The individual bits and fields in the interface memory are defined in Table 7.

Codec Firmware Interface

The codec has embedded logic to allow configuration of its device for full utilization of the digital cordless telephone. The capability of configuring the codec allows for optimal interfaces for both the handset and base station.

The following is an overview of the firmware interface used in the digital cordless phone. Control of the interface register is built into the Hummingbird chip set. The following information is provided for reference purposes only.

Description

The microcontroller communicates with the codec via a dedicated serial port. The codec has an 8-bit register that is used to configure the device. The register is defined below in Table 5.

This register may be written to or read from via the serial digital interface. An 8-bit address word is used, consisting of 3 address bits, 1 bit to indicate whether reading or writing, and 4 unassigned bits.

Table 5. Audio Codec Memory Map

Register Name	Hex Address	Bit							
		7	6	5	4	3	2	1	0
CR2	010	DACGn	MicGn1	MicGn0	LineOen	SpkOen	ADCGn	LineIen	MicEn

Table 6. Hummingbird ASIC Memory Map (1 of 2)

Register Function	Reg. Addr. (hex)	Bit 7	6	5	4	3	2	1	0
Codec Configuration/Status	0000	CdcIrqS	CdcFrDis	CdcAsync	CdcOe	CdcMode		CdcOem	CdcEn
Codec Data;	0001	CdcDataLow							
(TX-write, RX-read)	0002	CdcDataHigh							
Miscellaneous F	0003	Wait4Irq	reserved	ParkMsk	reserved				
Reserved	0004-000B	reserved							
GPIO Configuration A	000C	GpioAE7	GpioAE6	GpioAE5	GpioAE4	GpioAE3	GpioAE2	GpioAE1	GpioAE0
GPIO Data A	000D	GpioAD7	GpioAD6	GpioAD5	GpioAD4	GpioAD3	GpioAD2	GpioAD1	GpioAD0
GPIO Configuration B	000E	GpioBE7	GpioBE6	GpioBE5	GpioBE4	GpioBE3	GpioBE2	GpioBE1	GpioBE0
GPIO Data B	000F	GpioBD7	GpioBD6	GpioBD5	GpioBD4	GpioBD3	GpioBD2	GpioBD1	GpioBD0
GPIO Configuration C	0010	GpioCE7	GpioCE6	GpioCE5	GpioCE4	GpioCE3	GpioCE2	GpioCE1	GpioCE0
GPIO Data C	0011	GpioCD7	GpioCD6	GpioCD5	GpioCD4	GpioCD3	GpioCD2	GpioCD1	GpioCD0
Interrupt Mask	0012	IrqMsk8	IrqMsk7	IrqMsk6	IrqMsk5	IrqMsk4	IrqMsk3	IrqMsk2	IrqMsk1
Interrupt Pending	0013	IrqPend8	IrqPend7	IrqPend6	IrqPend5	IrqPend4	IrqPend3	IrqPend2	IrqPend1
Timer A Configuration	0014	reserved				TaShort	TaMode	TaEn	TaRbSel
Timer A Period	0015	TimerAPeriod							
Timer B / ART Configuration	0016	ArtRxClk		ArtTxOC	TbSel	TbShort	TbMode	TbEn	TbRbSel
Timer B Period	0017	TimerBPeriod							
ART Data (TX-write, RX-read)	0018	ArtData							
Keypad Column Data	0019	KeyCD7	KeyCD6	KeyCD5	KeyCD4	KeyCD3	KeyCD2	KeyCD1	KeyCD0
Keypad Column Enable	001A	KeyCE7	KeyCE6	KeyCE5	KeyCE4	KeyCE3	KeyCE2	KeyCE1	KeyCE0
Keypad Row Data and Enable	001B	KeyRE3	KeyRE2	KeyRE1	KeyRE0	KeyRD3	KeyRD2	KeyRD1	KeyRD0
Sleep/Watchdog Timer Config.	001C	SlpMode	WdogInit	WRetrig	WdogEn	ResetOut	SlpRbSel	reserved	
Sleep/Watchdog Timer Period	001D	SleepTimer							
Wait States	001E	reserved	RomWait			reserved	RamWait		
Link ID	001F	IdLow							
	0020	IdHigh							
Scramble Word	0021	Scramble							
Spreader Code	0022	SpreadLow							
	0023	SpreadEn	reserved			SpreadHigh			
reserved	0024-0032	reserved							
Controller Status	0033	reserved		HostAck	Park	KeyDet	SlpRst	WdogRst	MstrRst
reserved	0034-0038	reserved							
Battery ADC (read-only)	0039	reserved				BattAdc			
Analog Configuration	003A	TxDacOe	AMstSlp	reserved		BattSlp	RxSlp	AgcSlp	AuxSlp
ART/Timer B Prescaler	003B	N				M			
reserved	003C-003D	reserved							
GPIO Config. D and GPIO Data D	003E	GpioDE1	GpioDE0	reserved				GpioDD1	GpioDD0
reserved	003F	reserved							

Table 6. Hummingbird ASIC Memory Map (2 of 2)

Register Function	Reg. Addr. (hex)	Bit 7	6	5	4	3	2	1	0
Page 0 RAM	0040-00FF								
Page 1 RAM	0100-0101								
Interrupt 8 Branch Vector	0102	Irq8Low							
	0103	Irq8High							
Page 1 RAM	0104-0105								
Interrupt 7 Branch Vector	0106	Irq7Low							
	0107	Irq7High							
Page 1 RAM	0108-01FF								
Audio Engine	0200-02FF								
Host Scratchpad (128 bytes)	0300-037F								
Host Interrupt Generation (write-only)	0380-03BF	HostIrqPuls							
reserved	03C0-03FF	reserved							
Page 4 RAM (16 bytes)	0400-040F	TDDC RX FIFO							
Page 4 RAM (16 bytes)	0400-041F	TDDC TX FIFO							
Page 4 RAM (32 bytes)	0420-043F								
reserved	0440-05FF	reserved							
Page 6, 7 RAM	0600-07FF								
reserved	0800-0BFF	reserved							
Page 12,13,14 RAM	0C00-0EFF								
reserved	0F00-0FFF	reserved							
Off-Chip RAM CS Memory (16 KB)	1000-4FFF								
Off-Chip ROM CS Memory (20 KB)	5000-9FFF								
On-Chip Program Memory (24 KB)	A000-FFEF								
Interrupt 6 Branch Vector	FFF0	Irq6Low							
	FFF1	Irq6High							
Interrupt 5 Branch Vector	FFF2	Irq5Low							
	FFF3	Irq5High							
Interrupt 4 Branch Vector	FFF4	Irq4Low							
	FFF5	Irq4High							
Interrupt 3 Branch Vector	FFF6	Irq3Low							
	FFF7	Irq3High							
Interrupt 2 Branch Vector	FFF8	Irq2Low							
	FFF9	Irq2High							
Interrupt 1 Branch Vector	FFFA	Irq1Low							
	FFFB	Irq1High							
NMI Interrupt Branch Vector	FFFC	IrqNmiLow							
	FFFD	IrqNmiHigh							
Reset Interrupt Branch Vector	FFFE	IrqResetLow							
	FFFF	IrqResetHigh							

Table 7. Memory Map Bit Definitions (1 of 3)

Mnemonic (note 1)	Address (note 2)	Name and Description
CdcEn	0000:0	**Codec Enable.** When set, the codec serial port interface is enabled, provided that CdcClkEn has also been set. Default is 0.
CdcOem	0000:1	**Codec OEM Configuration.** When the codec is not enabled, this bit can be read to determine the pull-up/pull-down value on the CDCDATAO pin.
CdcMode	0000:3-2	**Codec Mode Select.** Selects which of the 4 codec serial port commands is implemented. Code default is 00.
CdcOe	0000:4	**Codec Output Enable.** When reset, the codec serial port outputs are high impedance. When set, the serial port outputs are driven if CdcEn is set. Default is 0.
CdcAsync (write-only; reads as 0)	0000:5	**Codec Immediate Asynchronous Transfer.** This mode is used to initiate a codec serial port transaction without waiting for the 8 kHz strobe to occur. The bit is reset by the codec serial port logic after the transfer has been initiated. If the 8 kHz strobe occurs during the transfer, it will be ignored.
CdcFrDis	0000:6	**Codec Frame Disable.** When set to 1, the 8 kHz frame pulse will not generate a codec serial port transfer. When the frame is disabled, an interrupt will not be generated when the 8 kHz pulse occurs. An interrupt will be generated after asynchronous transfer. Default is 0.
CdcIrqS	0000:7	**Codec Interrupt Source Select.** When set to 1, the codec pending bit is controlled using the codec CDCDATAI pin. When reset to 0, the codec pending bit is controlled by the codec serial port. Default is 0.
CodecDataLow	0001	**Codec Data Buffer Low.** When read, this buffer provides the least significant byte of received codec data. When written, this buffer provides the least significant byte of transmit data.
CodecData-High	0002	**Codec Data Buffer High.** When read, this buffer provides the most significant byte of received codec data. When written, this buffer provides the most significant byte of transmit data.
ParkMsk	0003:5	**Park Mask.** When set to 1, transitions on the park pin will cause the ASIC to wake up early. When set to 0, transitions on the park pin will cause the ASIC to wake up early. Default is 0.
Wait4Irq	0003:7	**Wait for Interrupt.** When a 1 is written to this bit, the MC19 macro is held inactive until an unmasked interrupt occurs. The bit is cleared when the unmasked interrupt occurs. Default is 0.
GpioAE[7:0] GpioAD[7:0] GpioBE[7:0] GpioBD[7:0] GpioCE[7:0] GpioCD[7:0]	000C 000D 000E 000F 0010 0011	**General Purpose I/O**. These registers control the 24 GPIO pins, which are separated into 3 groups of 8 pins, designated A, B, and C. (The 144-pin ASIC contains a fourth group of 2 pins, designated D; see location \$003E). Each pin is configured as either an input or an output by the associated output enable bit in a GPIO configuration register (GpioXE registers). Data is read from or written to each pin using the associated data bit in a GPIO data register (GpioXD registers). Resetting a pin's output enable bit to 0 configures the pin as an input; setting the bit to 1 configures the pin as an output. Reading a pin's data bit will provide the pin's logic value; writing to a pin's data bit will drive the specified logic value to the pin.
IrqMsk[8:1]	0012	**Interrupt Mask.** This register masks the controller interrupt signals. If a mask bit is set to 1, the MC19 controller will not receive the corresponding interrupt signal. Default is all bits set to 1.
IrqPend[8:1]	0013	**Interrupt Pending.** A bit in this location is set to 1 if the corresponding interrupt has occurred. The bit is reset to 0 by the MC19 controller by writing a 1 to the corresponding location.
TaRbSel	0014:0	**Timer A Readback Select.** This bit selects the value returned to the controller when the Timer A period register is read. When set to 1, the current state of the timer (counter) is returned. When reset to 0, the currently specified timer period (TimerAPeriod) is returned. Default is 0.
TaEn	0014:1	**Timer A Enable.** When set to 1, this bit enables Timer A to start decrementing. When reset to 0, the timer is disabled and reset. Default is 0.
TaMode	0014:2	**Timer A Mode.** Timer A can operate in either a single countdown mode (bit reset to 0) or a repeat countdown mode (bit set to 1). Default is 0.
TaShort	0014:3	**Timer A Short.** Setting this bit bypasses Timer A's divide-by-256 prescaler. Used for test. Default is 0.
TimerAPeriod	0015	**Timer A Period.** This value specifies the Timer A period. The delay between enabling the timer and the first timer interrupt is calculated using the following formula: Delay = (TimerAPeriod + 1) × (256 / 9.6 MHz).
TbRbSel	0016:0	**Timer B Readback Select.** Selects the value returned when the controller reads the Timer B period register. When set to 1, the current state of the timer (counter) is returned. When reset to 0, the currently specified timer period (TimerBPeriod) is returned. Default is 0.
TbEn	0016:1	**Timer B Enable.** When set to 1, this bit enables Timer B to start decrementing, or enables the ART interface. When reset to 0, the timer and ART are disabled and reset. The function is selected by ArtTbSel. Default is 0.

Table 7. Memory Map Bit Definitions (2 of 3)

Mnemonic (note 1)	Address (note 2)	Name and Description
TbMode	0016:2	**Timer B Mode.** When the TbSel bit is set to 1, Timer B can operate in either a single countdown mode (bit reset to 0) or a repeat countdown mode (bit set to 1). Default is 0.
TbShort	0016:3	**Timer B Short.** Setting this bit bypasses Timer B's divide-by-(M/N) prescaler. Used for test. Default is 0.
TbSel	0016:4	**Timer B Select.** Selects how Timer B is configured. When reset to 0, the serial ART interface is enabled, and Timer B is used to generate the ART's baud rate clock. When set to 1, Timer B functions as a standard timer.
ArtTxOC	0016:5	**ART Tx Open Collector.** When set (1) to 1, the ART TX pin is an open collector output. Default is 0.
ArtRxClk	0016:7-6	**ART Rx Clock.** This location is used to set the RX ART port to a slower rate than the TX port. Default value is 00 = TX rate equal to RX rate.
TimerBPeriod	0017	**Timer B Period.** This value specifies either the Timer B period or the ART baud rate. The delay between enabling the timer and the first timer interrupt is calculated by: Delay = (TimerBPeriod + 1) × (M/N)/9.6 MHz where M is TmrBM and N is TmrBN (locations $003B:3-0, $003B:7-4, respectively)
ArtData (TX-write, RX-read)	0018	**ART Data Buffer.** Data to be transmitted out of the ART serial port is written to this location. Received data is read from this location. Data is shifted in/out LSB first.
KeyCD[7:0] KeyCE[7:0]	0019:7-0 001A:7-0	**Keypad Column Data/Keypad Column Enable.** These locations configure the ASIC's KEYPADC pins. When set, the KeyCE bit enables the KeyCD bit to drive the KEYPADC pin. When the KeyCE bit is reset to 0, the KEYPADC pin is configured as an input. Reading the KeyCD location provides the value at the KEYPADC pins. Writing a value to KeyCD drives that value to those KEYPADC pins whose KeyCE bits are set to 1.
KeyRD[3:0] KeyRE[3:0]	001B:3-0 001B:7-4	**Keypad Row Data/Keypad Row Enable.** These locations configure the KEYPADR pins of the ASIC. When set, the KeyRE bit enables the KeyRD bit to drive the KEYPADR pin. When the KeyRE bit is reset to 0, the KEYPADR pin is configured as an input. Reading the KeyRD location provides the value at the KEYPADR pins. Writing a value to KeyRD drives that value to those KEYPADR pins whose KeyRE bits are set to 1.
SlpRbSel	001C:2	**Sleep/Watchdog Timer Readback Select.** This bit selects the data read when the sleep timer locations are accessed. When reset to 0, the sleep/watchdog timer's programmed period is read back. When set to 1, the sleep/watchdog counter's value is read back.
ResetOut	001C:3	**Reset Out.** This bit is OR'ed with the ASIC RESETIP pin and drives the ASIC RESETOP pin. Default is 1.
WdogEn	001C:4	**Watchdog Enable.** When set to 1, this bit enables the sleep/watchdog timer to reset the ASIC if two sleep/watchdog timer interrupts occur without a watchdog retrigger occurring. When reset to 0, this feature is disabled. Default is 0.
WRetrig	001C:5	**Watchdog Retrigger.** Writing a 1 to this location reinitializes the watchdog reset counter and prevents an ASIC reset from occurring from the sleep/watchdog timer. This bit should be written to after every sleep/watchdog interrupt to prevent an ASIC reset from occurring.
WdogInit	001C:6	**Watchdog Force Timer Load.** Writing a 1 and then a 0 to this location forces the sleep/watchdog timer to load the sleep timer period immediately. This bit should not be written to unless the sleep timer counter's value is greater than 1.
SlpMode	001C:7	**Sleep Mode Initiate.** Writing a 1 and then a 0 to this location will put the ASIC to sleep. The ASIC will wake up after the sleep period has expired.
SleepTimer	001D	**Sleep Timer Period.** This period is used to specify the sleep period of the ASIC. While the ASIC is awake, it specifies the rate at which the sleep/watchdog timer interrupt occurs. This can be used to implement a real-time clock. The delay = (count+1) × (1/9.6 MHz) × (1/256) × (1/256).
RamWait	001E:2-0	**RAM Wait State.** This location is used to set the number of wait states for host address locations $0300-$03FF, and external RAM locations $1000-$4FFF, to a value between 7 and 0. Default is 7.
RomWait	001E:6-4	**ROM Wait State.** Used to set the wait states for the external ROM locations $5000-$9FFF. Default is 7.
IdLow IdHigh	001F 0020	**ID.** Together, these ID locations form the 16-bit programmable ID portion of the A-frame.
Scramble	0021	**Scramble Code.** This specifies 8 bits of the starting value of the 16-bit scrambler used by the ASIC.
SpreadLow SpreadHigh	0022 0023:3-0	**Spread Code.** The ASIC uses a 12-bit spread code which is specified by this location.
SpreadEn	0023:7	**Spread Code Enable.** When set to 1, this bit enables the transmitted data to become mixed with the spread code. When reset to 0, the data is transmitted without spreading. Default is 0.

Table 7. Memory Map Bit Definitions (3 of 3)

Mnemonic (note 1)	Address (note 2)	Name and Description
MstrRst	0033:0	**Master Reset Flag.** Set if the ASIC's reset pin has been active. Reset by writing 1 to this location.
WdogRst	0033:1	**Watchdog Reset Flag.** Set if the ASIC has been reset by the watchdog timer. Reset by writing 1 to this location.
SlpRst	0033:2	**Sleep Reset Flag.** Set when the ASIC wakes up from the sleep mode. Reset by writing 1 to this location.
KeyDet	0033:3	**Key Pressed Detector Flag.** When set to 1, this location specifies that at least one of the KEYPADR pins of the ASIC is high and indicates that a key is being pressed.
Park	0033:4	**Park Status.** This location provides the value of the ASIC's park pin. When set to 1, the system is parked and the handset and base station can communicate using the ART.
HostAck	0033:5	**Host Acknowledge Flag.** Set if the ASIC's HostIrq input has been active. Reset by writing 1 to this location.
BattAdc	0039:3-0	**Battery ADC.** Reading this location provides the value from the battery ADC.
AuxSlp	003A:0	**Analog Auxiliary DAC Sleep.** When set to 1, the auxiliary DAC is put into a sleep mode. When reset to 0, the DAC is enabled. Default is 1.
AgcSlp	003A:1	**Analog AGC DAC Sleep.** When set to 1, the AGC DAC is put into a sleep mode. When reset to 0, the DAC is enabled. Default is 1.
RxSlp	003A:2	**Analog RX Sleep.** When set to 1, the RX ADCs and RX reference DACs are put into a sleep mode. When reset to 0, the RX cells are enabled. Default is 1.
BattSlp	003A:3	**Analog Battery ADC Sleep.** When set to 1, the battery ADC is put into a sleep mode. When reset to 0, the ADC is enabled. Default is 1.
AMstSlp	003A:6	**Analog Master Sleep.** When set to 1, the analog reference circuits are put into sleep mode. When reset to 0, the analog reference signals are generated. This bit must be enabled in order to use any of the analog circuits. Default is 1.
TxDacOe	003A:7	**Analog TX DAC Output Enable.** When set to 1, the TX DAC output is always driven to either 1.2V or 0.6V. When reset to 0, the TX DAC output enable is controlled by the TDDC logic. In this condition, the output is high-impedance during RX frames and is driven during TX frames. Default is 1.
TmrBM	003B:0-3	**Timer B M.** This sets the M value of Timer B's prescaler divide ratio. The actual value loaded into this register must be M' where M' = 16-M+N. Timer B prescaler clock output = 9.6MHz × (N/M). Default is $C.
TmrBN	003B:4-7	**Timer B N.** This location sets the N value of Timer B's prescaler divide ratio. Timer B prescaler clock output = 9.6MHz × (N/M). Default is $1.
GpioDE[1:0] GpioDD[1:0]	003E:7-6 003E:1-0	**General Purpose I/O.** These registers control the 2 GPIO D pins (144-pin ASIC only). Each pin can be configured as an input or an output, and is associated with an output enable bit in a GPIO configuration register and a data bit in a GPIO data register. To configure a pin as an input, the corresponding output enable bit is reset to 0. Reading the corresponding data bit will provide the logic value at the GPIO pin. To configure a pin as an output, the corresponding output enable bit is set to 1. Writing to the corresponding data bit will drive that logic value to the GPIO pin. Reading the corresponding data bit will provide the logic value at the GPIO pin, which will be the same as that written to the data bit if no pin conflict exists.

Notes:
1. "A[m:n]" denotes a series of bits where each bit's name is "Am" through "An" (m:n is a range of numbers). For example, "IrqMsk[8:1]" denotes bits IrqMsk8, IrqMsk7, . . . , IrqMsk1.
2. Memory bit location is designated "A:B", where A is the hex address ($0000-$FFFF), B is the bit position (0-7, 0 = least significant bit).

Electrical Characteristics

The ASIC's absolute maximum ratings, recommended operating conditions, current and power requirements, and digital and analog interface electrical characteristics are listed in Table 8 through Table 12, respectively.

The codec's absolute maximum ratings, recommended operating conditions, current and power requirements, and digital interface electrical characteristics are listed in Table 13 through Table 23, respectively.

Table 8. Absolute Maximum Ratings (ASIC)

Parameter	Symbol	Limits	Units
Supply voltage	V_{DD}	–0.5 to +6.0	V
Input voltage	V_{IN}	–0.5 to (V_{DD} + 0.5)	V
Analog inputs	V_{IN}	–0.3 to (V_{DD} + 0.3)	V
Voltage applied to outputs in high impedance (OFF) state	V_{HZ}	–0.5 to (V_{DD} + 0.5)	V
DC input clamp current	I_{IK}	±20	mA
DC output clamp current	I_{OK}	±20	mA
Static discharge voltage (25 °C)	V_{ESD}	±2500	V
Latch-up current (25 °C)	I_{TRIG}	±200	mA
Operating temperature range	T_A	0 to +70	°C
Storage temperature range	T_{STG}	–65 to +150	°C
Relative humidity	H_{REL}	Up to 90% non-condensing, or a wet bulb temperature up to 35°C, whichever is less.	

Note: Voltages referenced to ground (V_{SS}).

Table 9. Recommended Operating Conditions (ASIC)

Parameter	Symbol	Limits	Units
Supply voltage	V_{DD}	+2.7 to +5.25	V
Operating ambient temperature range	T_A	–10 to +70	°C

Note: Voltages referenced to ground (V_{SS}).

Table 10. Current Requirements (ASIC)

Mode	Typical Current @ 25°C (mA)	
	3.6V	5V
Operating	12	20
Sleep	0.8	1.5

Table 11. Digital Interface Electrical Characteristics (ASIC)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input high voltage	V_{IH}	V_{DD} = 2.7 V – 5.25 V	0.7 × V_{DD}		V
Input low voltage	V_{IL}	V_{DD} = 2.7 V – 5.25 V		0.2 × V_{DD}	V
Input leakage current	I_{IN}	V_{IN} = 0 – V_{DD}		±10	µA
Output high voltage	V_{OH}	V_{DD} = 2.7 V, I_{OH} = 4 mA	2.4		V
Output low voltage	V_{OL}	V_{DD} = 5.25 V, I_{OL} = 4 mA		0.4	V
Capacitive drive	C_D	I_O = 2 mA I_O = 4 mA		25 50	pF pF

Notes:
1. Applies to types: I, IS-PUP, I-PUP, IS-PDN, O, B, B-PUP unless otherwise indicated.
2. Test conditions: V_{DD} = 5.25 V unless otherwise indicated.
3. All voltages referenced to ground (V_{SS}). Currents are positive when flowing into the device.

Table 12. Analog Interface Electrical Characteristics (ASIC)

Name	Type	Parameter	Min	Typ	Max	Unit
[RXIP, RXIN],	I-A	DC input resistance to ground	100			kΩ
[RXQP, RXQN]		Input voltage	0		V_{DD}	V
(Note 1)		Nominal differential input voltage		0.3		V_{PP}
		Common mode input voltage	V_{SS}+0.8	V_{DD}–2	V_{DD}–1.3	V
		Bandwidth, <1 dB	1			MHz
BATTERY	I-A	Input load impedance	1			MΩ
		Input voltage (Note 7)	1.2		2	V
		Bandwidth, 3 dB	10			Hz
AGC	O-A	Output voltage range		1.2 to 2.0		V
		Output voltage range error			±0.1	V
		Ban32dwidth, 3 dB	25			kHz
		Noise power (1 kHz – 10 kHz) (Note 2)			–25	dB
		DC offset voltage			50	mV
		DC load	10			kΩ
		AC capacitive load (Note 3)			16	pF
		AC resistive load (Note 3)	1			kΩ
AUX DAC	O-A	Output voltage range		0.4 to 2.0		V
		Output voltage range error			±0.1	V
		Bandwidth, 3 dB	25			kHz
		Noise power (1 kHz – 10 kHz) (Note 2)			–25	dB
		DC offset voltage			50	mV
		DC load	10			kΩ
		AC capacitive load (Note 4)			16	pF
		AC resistive load (Note 4)	1			kΩ
TXDATA	O-A	Output voltage range		1.70		Vp-p
		Output voltage range error			±10	%
		Rise/fall slew rate (Note 5)			50/1.2	ns/V
		DC load	2			kΩ
		AC resistive load (Note 6)	2			kΩ

Notes:
1. Differential inputs: RXIP, RXQP are positive polarity; RXIN, RXQN are negative polarity.
2. Relative to 1 LSB.
3. At greater than 25 kHz.
4. At greater than 1 kHz.
5. With 10 pF capacitive load.
6. At greater than 600 kHz.
7. V_{IN} < 1.2 produces A/D value of 1.2 V input; V_{IN} > 2 V produces A/D value of 2 V.

Table 13. Absolute Maximum Ratings (Codec)

Parameter	Symbol	Limits	Units
Supply voltage	V_{DD}	+7.0	V
Input voltage	V_{IN}	$-0.3 \le V_{IN} < V_{DD} + 0.3$ V	V
Analog inputs	V_{IN}	$-0.3 \le V_{IN} < V_{DD} + 0.3$ V	V
DC input clamp current	I_{IK}	±10	mA
DC output clamp current	I_{OK}	±10	mA
Static discharge voltage (25 °C)	V_{ESD}	±2500	V
Latch-up current (25 °C)	I_{TRIG}	±150	mA
Operating temperature range	T_A	0 to +70	°C
Storage temperature range	T_{STG}	–55 to +150	°C
Relative humidity	H_{REL}	Up to 90% non-condensing, or a wet bulb temperature up to 35 °C, whichever is less.	

Note: Voltages referenced to ground (Vss).

Table 14. Recommended Operating Conditions (Codec)

Parameter	Symbol	Limits	Units
Supply voltage	V_{DD}	+2.7 to +5.25	V
Operating ambient temperature range	T_A	0 to +70	°C

Note: Voltages referenced to ground (Vss).

Table 15. Current and Power Requirements (Codec)

Mode	Typical Current @ 25°C (mA)
Operating (+5V)	4.7
Sleep (+5V)	< 0.5
Operating (+3V)	4.6
Sleep (+3V)	< 0.5

Note: Test conditions: V_{DD} = +5V, +3.6V.

Table 16. Digital Interface Electrical Characteristics (Codec)

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input high voltage (Logic 1)	V_{IH}	DV_{DD} = 2.7 V	2		V
Input low voltage (Logic 0)	V_{IL}	DV_{DD} = 2.7 V		1	V
Output high voltage (Logic 1)	V_{OH}	DV_{DD} = 2.7 V	2.3		V
Output low voltage (Logic 0)	V_{OL}	DV_{DD} = 2.7 V		0.4	V
Input leakage current	I_{IN}	DV_{DD} = 2.7 V		±10	µA
Input high voltage (Logic 1)	V_{IH}	DV_{DD} = 5 V	3.5		V
Input low voltage (Logic 0)	V_{IL}	DV_{DD} = 5 V		1	V
Output high voltage (Logic 1)	V_{OH}	DV_{DD} = 5 V	4		V
Output low voltage (Logic 0)	V_{OL}	DV_{DD} = 5 V		0.4	V
Output leakage current	I_{LO}	DV_{DD} = 5 V		±10	µA

Notes:
1. Applies to types: I, IS-PUP, I-PUP, IS-PDN, O, B, B-PUP unless otherwise indicated.
2. Test conditions: V_{DD} = 5.00 V unless otherwise indicated.
3. All voltages referenced to ground (V_{SS}). Currents are positive when flowing into the device.

Table 17. Codec ADC Channel Electrical Characteristics Using 2.7V Power

Parameter	Min	Typ	Max	Units
Microphone gain (CR2 register, bits 5 and 6)				
Microphone gains 0 & 1 = 00 dB		0		dB
= 01 dB		20		dB
= 10 dB		25		dB
= 11 dB		30		dB
Microphone differential input signal level				
Microphone gain = 0 dB			1.0	Vpk
Microphone gain = 20 dB			0.1	Vpk
Microphone gain = 25 dB			0.056	Vpk
Microphone gain = 30 dB			0.0315	Vpk
Microphone differential input signal level for peak SINAD				
ADCGn (CR2 bit 2) = 0 (–4 dB gain)				
Microphone gain = 0 dB		0.796		Vpk
Microphone gain = 20 dB		0.0796		Vpk
Microphone gain = 25 dB		0.0447		Vpk
Microphone gain = 30 dB		0.0252		Vpk
ADCGn (CR2 bit 2) = 1 (0 dB gain)				
Microphone gain = 0 dB		0.502		Vpk
Microphone gain = 20 dB		0.0502		Vpk
Microphone gain = 25 dB		0.0282		Vpk
Microphone gain = 30 dB		0.0159		Vpk
Microphone anti-aliasing filter (AAF) –3 dB BW (0 dB gain)			69	kHz
Microphone input impedance (single-ended)				
Microphone gain = 0 dB	216	265	314	kΩ
Microphone gain = 20 dB	31	38	45	kΩ
Microphone gain = 25 dB	31	38	45	kΩ
Microphone gain = 30 dB	31	38	45	kΩ
Microphone input gain accuracy	–0.5	0	0.5	dB
Microphone input impedance variation	–15	0	15	%
Microphone input total harmonic distortion			–83	dB
Microphone input referred noise (Note 1)				
Microphone gain = 0 dB			–81	dBVrms
Microphone gain = 20 dB			–81	dBVrms
Microphone gain = 25 dB			–76	dBVrms
Microphone gain = 30 dB			–71	dBVrms
Line input signal level			1.0	Vpk
Line input signal level for peak SINAD				
ADCGn = 0 (–4 dB gain)		1.2		Vpk
ADCGn = 1 (0 dB gain)		0.757		Vpk
Line AAF –3 dB BW	18	25	32	kHz
Line input impedance	122	150	177	kΩ
Line input gain		0		dB
Line input gain accuracy	–0.5	0	0.5	dB
Line input impedance variation			±15	%
Line input total harmonic distortion			–83	dB
Line input referred noise (Note 2)			–78	dBVrms

Notes:
1. For this noise the 4 dB attenuation in the ADC should be disabled. The noise is measured in the circuit configuration shown in Figure 11.
2. For this noise, the 4 dB attenuation in the ADC should be disabled. The line input can be either disconnected and disabled or can be terminated to AVSS with a 2k ohm resistor.

Table 18. Codec ADC Channel Electrical Characteristics Using 5V Power

Parameter	Min	Typ	Max	Units
Microphone gain (CR2 register, bits 5 and 6)				
Microphone gains 0 & 1 = 00 dB		0		dB
= 01 dB		20		dB
= 10 dB		25		dB
= 11 dB		30		dB
Microphone differential input signal level				
Microphone gain = 0 dB			1.6	Vpk
Microphone gain = 20 dB			0.16	Vpk
Microphone gain = 25 dB			0.09	Vpk
Microphone gain = 30 dB			0.0505	Vpk
Microphone differential input signal level for peak SINAD				
ADCGn = 0 (–4 dB gain)				
Microphone gain = 0 dB		0.796		Vpk
Microphone gain = 20 dB		0.079		Vpk
Microphone gain = 25 dB		0.0447		Vpk
Microphone gain = 30 dB		0.0252		Vpk
ADCGn = 1 (0 dB gain)				
Microphone gain = 0 dB		0.8		Vpk
Microphone gain = 20 dB		0.08		Vpk
Microphone gain = 25 dB		0.045		Vpk
Microphone gain = 30 dB		0.0253		Vpk
Microphone AAF –3 dB BW (0 dB gain)			69	kHz
Microphone input impedance				
Microphone gain = 0 dB	216	265	314	kΩ
Microphone gain = 20 dB	31	38	45	kΩ
Microphone gain = 25 dB	31	38	45	kΩ
Microphone gain = 30 dB	31	38	45	kΩ
Microphone input gain accuracy	–0.5	0	0.5	dB
Microphone input impedance variation	–15	0	15	%
Microphone input total harmonic distortion			–83	dB
Microphone input referred noise (Note 1)				
Microphone gain = 0 dB			–81	dBVrms
Microphone gain = 20 dB			–81	dBVrms
Microphone gain = 25 dB			–76	dBVrms
Microphone gain = 30 dB			–71	dBVrms
Line input signal level			1.6	Vpk
Line input signal level for peak SINAD				
ADCGn = 0 (–4 dB gain)		1.2		Vpk
ADCGn = 1 (0 dB gain)		1.0		Vpk
Line AAF –3 dB BW	18	25	32	kHz
Line input impedance	122	150	177	kΩ
Line input gain		0		dB
Line input gain accuracy	–0.5	0	0.5	dB
Line input impedance variation			±15	%
Line input total harmonic distortion			–83	dB
Line input referred noise (Note 2)			–78	dBVrms

Notes:
1. For this noise the 4 dB attenuation in the ADC should be disabled. The noise is measured in the circuit configuration shown in Figure 11.
2. For this noise, the 4 dB attenuation in the ADC should be disabled. The line input can be either disconnected and disabled or can be terminated to AVSS with a 2k ohm resistor.

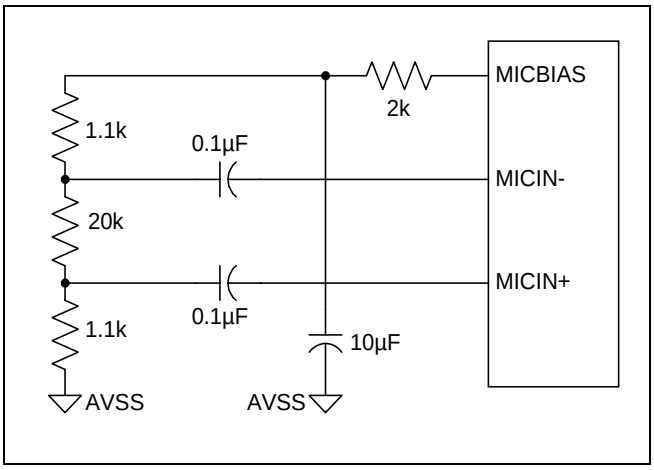


Figure 11. Codec Noise Test Circuit

Table 19. Codec ADC Channel Signal to Noise and Distortion Ratio (SINAD)
(Numbers are miminum with any ADC gain setting @ input frequency of 1 kHz)

Parameter	Min	Typ	Max	Units
Peak SINAD for microphone input				
Microphone gain = 0 dB	54	72.4		dB
Microphone gain = 20 dB	54	62.5		dB
Microphone gain = 25 dB	54			dB
Microphone gain = 30 dB	54			dB
SINAD for Microphone input of –40 dB				
Microphone gain = 0 dB	29	47		dB
Dynamic range for microphone input, Gain = 0 dB	70	84		dB
Peak SINAD for line input	54	75		dB
SINAD for line input of –40 dB	29	46		dB
Dynamic range for line input	70	83		dB

Table 20. Codec Microphone Bias Output

Parameter	Min	Typ	Max	Units
Output voltage		2.2		V
Output current			1	mA
Output noise 150 Hz to 3.6 kHz			–84	dBVrms

Table 21. Codec DAC Channel Electrical Characteristics Using 2.7V Power

Parameter	Min	Typ	Max	Units
Speaker differential output signal level			2.0	Vpk
Speaker total harmonic distortion (Note 1)			–71	dB
Speaker input referred noise (Note 2)			–81	dBVrms
Speaker differential output level for peak SINAD DACGn (CR2, bit 7) = 1 (6 dB gain) load = 600 Ω || 20 pF load = 300 Ω + 100 nF DACGn = 0 (0 dB gain) TxiCtrl = 10 (–6 dB gain) load = 600 Ω || 20 pF load = 300 Ω + 100 nF		 0.8 0.8 0.5 0.5		 Vpk Vpk Vpk Vpk
Line output signal level			1.0	Vpk
Line output total harmonic distortion			–71	dB
Line output referred noise (Note 2)			–81	dBVrms
Line output level for peak SINAD load = [600 Ω + 10 µF] || 20 pF DACGn = 0 (0 dB gain)		 0.36		 Vpk

Notes:
1. ZL > 120 ohm.
2. This noise is to be measured with a constant, zero amplitude, digital signal into the decoder. The noise should be measured with a CCITT phosphometric filter.

Table 22. Codec DAC Channel Electrical Characteristics Using 5V Power

Parameter	Min	Typ	Max	Units
Speaker differential output signal level			3.2	Vpk
Speaker total harmonic distortion (Note 1)			–71	dB
Speaker input referred noise (Note 2)			–81	dBVrms
Speaker differential output level for peak SINAD DACGn = 0 (0 dB gain) (CR2, bit 7) load = 600 Ω || 20 pF load = 300 Ω + 100 nF		 0.9 0.9		 Vpk Vpk
Line output signal level			1.6	Vpk
Line output total harmonic distortion			–71	dB
Line output referred noise (Note 2)			–81	dBVrms
Line output level for peak SINAD load = [600 Ω + 10 µF] || 20 pF DACGn = 0 (0 dB gain)		 0.56		 Vpk

Notes:
1. ZL > 120 ohm.
2. This noise is to be measured with a constant, zero amplitude, digital signal into the decoder. The noise should be measured with a CCITT phosphometric filter.

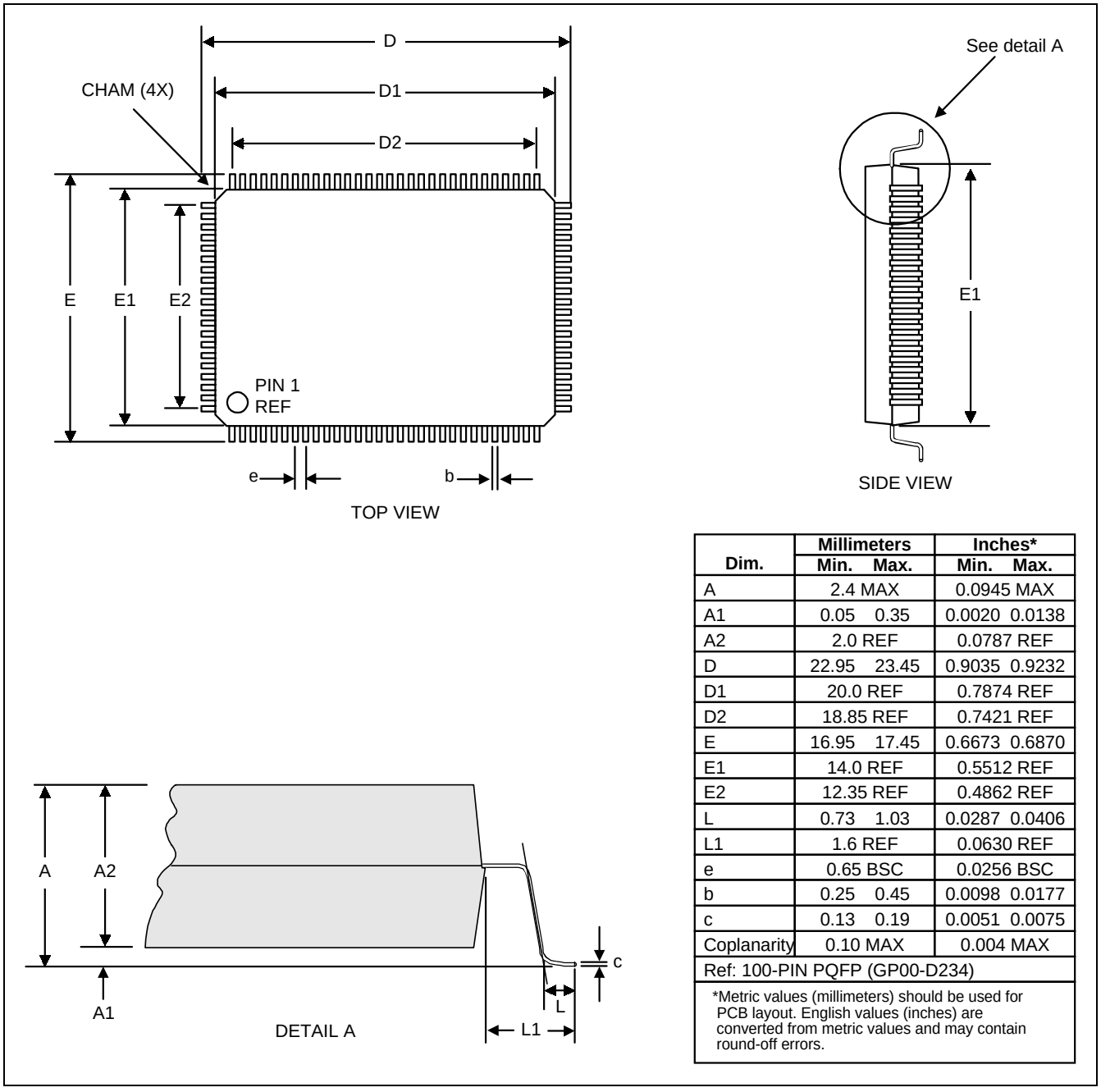
Table 23. Codec DAC Channel Signal to Noise and Distortion Ratio (SINAD)
(Numbers are miminum with any DAC gain setting @ input frequency of 1 kHz)

	Min	Typ	Max	Units
Peak SINAD for speaker output	68			dB
Peak SINAD for line output	65			dB

Device Set Dimensions

Package dimensions for the Hummingbird single-device 100-pin package (ASIC and audio codec) are given in Figure 12.

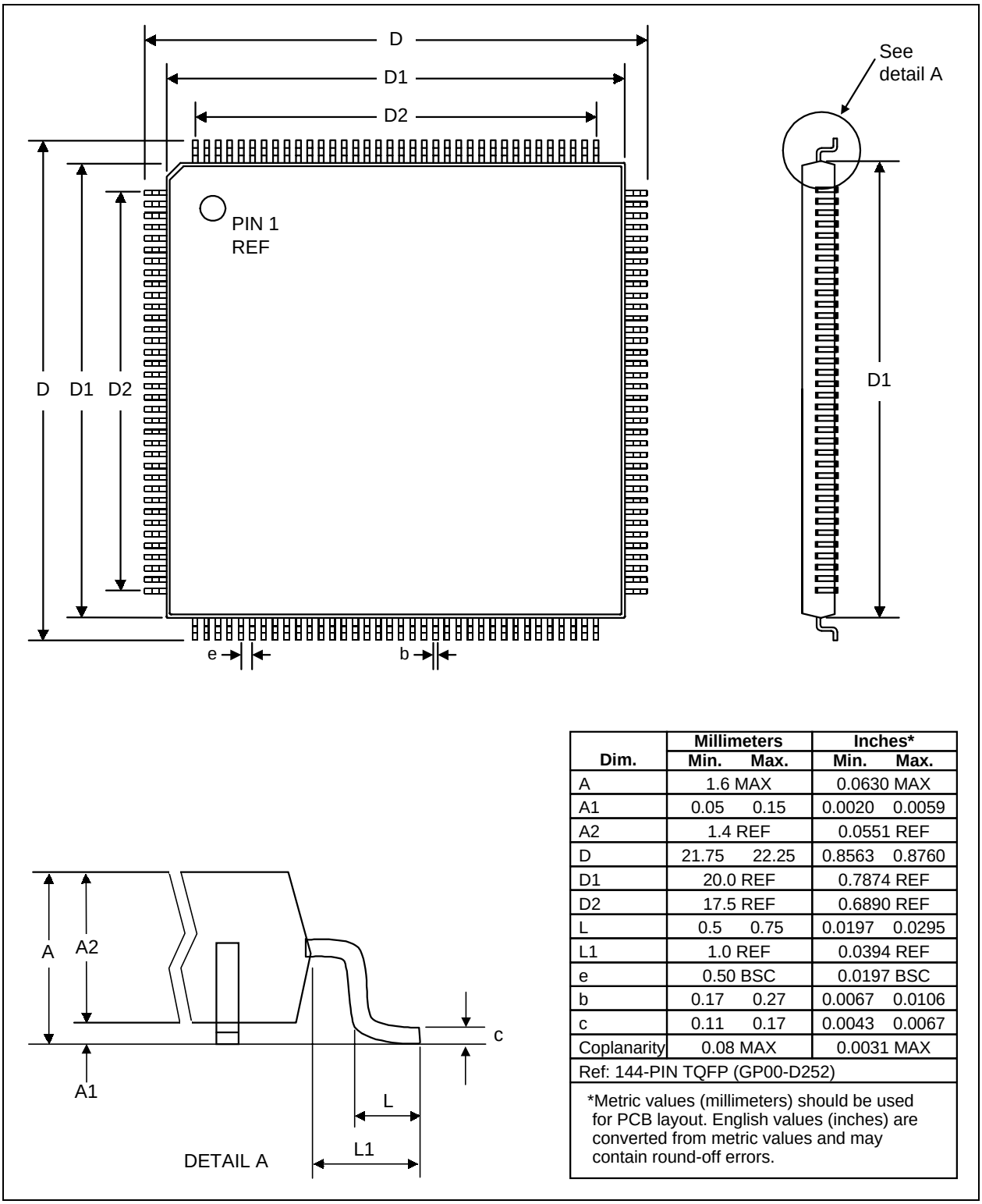
Package dimensions for the Hummingbird 144-pin ASIC are given in Figure 13, while Figure 14 gives package dimensions for the Hummingbird audio codec.



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		2.4 MAX		0.0945 MAX
A1	0.05	0.35	0.0020	0.0138
A2		2.0 REF		0.0787 REF
D	22.95	23.45	0.9035	0.9232
D1		20.0 REF		0.7874 REF
D2		18.85 REF		0.7421 REF
E	16.95	17.45	0.6673	0.6870
E1		14.0 REF		0.5512 REF
E2		12.35 REF		0.4862 REF
L	0.73	1.03	0.0287	0.0406
L1		1.6 REF		0.0630 REF
e		0.65 BSC		0.0256 BSC
b	0.25	0.45	0.0098	0.0177
c	0.13	0.19	0.0051	0.0075
Coplanarity		0.10 MAX		0.004 MAX
Ref: 100-PIN PQFP (GP00-D234)				

*Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may contain round-off errors.

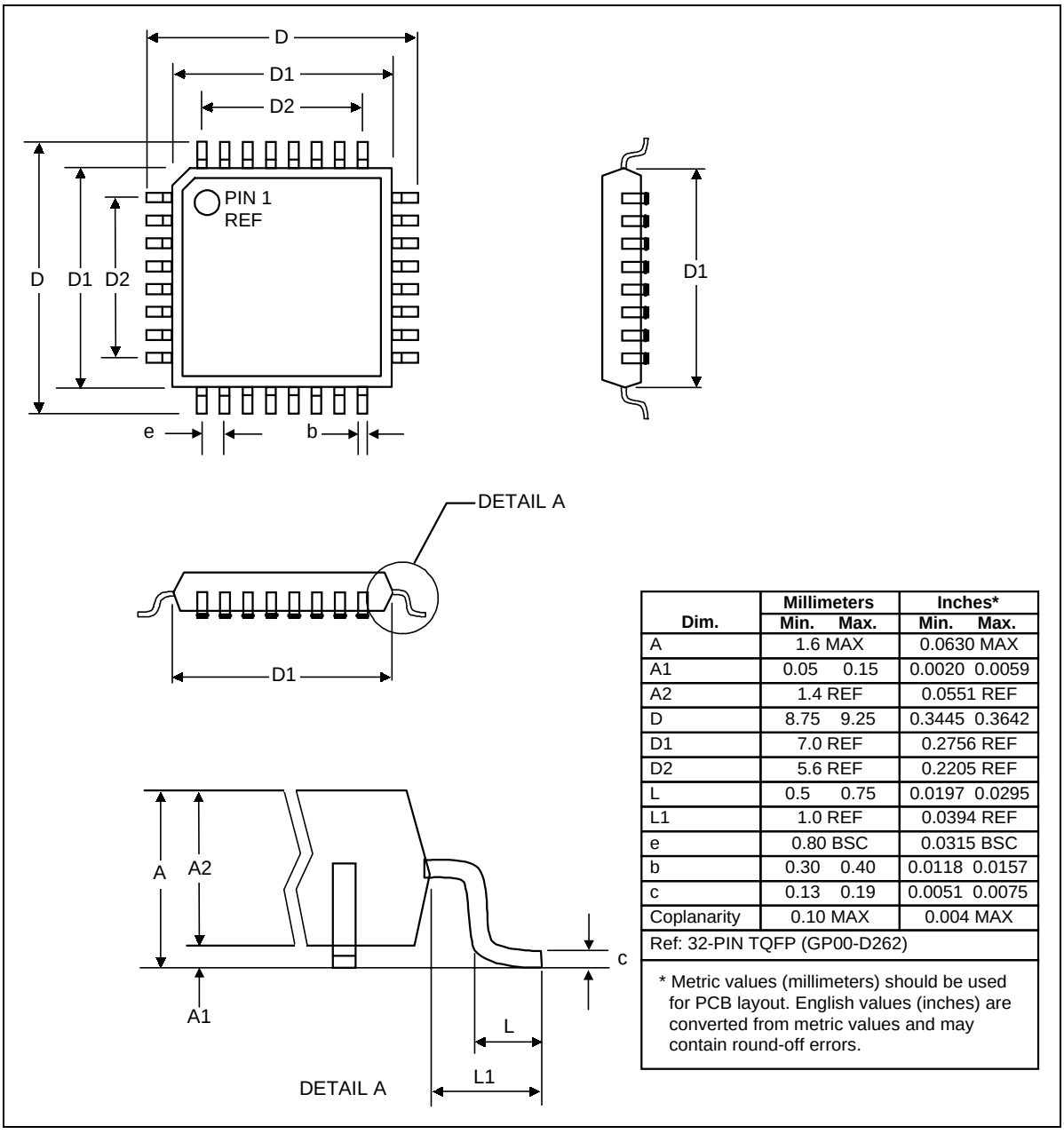
Figure 12. Package Dimensions for Hummingbird ASIC & Audio Codec – 100-Pin PQFP



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.6 MAX		0.0630 MAX	
A1	0.05	0.15	0.0020	0.0059
A2	1.4 REF		0.0551 REF	
D	21.75	22.25	0.8563	0.8760
D1	20.0 REF		0.7874 REF	
D2	17.5 REF		0.6890 REF	
L	0.5	0.75	0.0197	0.0295
L1	1.0 REF		0.0394 REF	
e	0.50 BSC		0.0197 BSC	
b	0.17	0.27	0.0067	0.0106
c	0.11	0.17	0.0043	0.0067
Coplanarity	0.08 MAX		0.0031 MAX	
Ref: 144-PIN TQFP (GP00-D252)				

*Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may contain round-off errors.

Figure 13. Package Dimensions for Hummingbird ASIC – 144-Pin TQFP



Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A		1.6 MAX		0.0630 MAX
A1	0.05	0.15	0.0020	0.0059
A2		1.4 REF		0.0551 REF
D	8.75	9.25	0.3445	0.3642
D1		7.0 REF		0.2756 REF
D2		5.6 REF		0.2205 REF
L	0.5	0.75	0.0197	0.0295
L1		1.0 REF		0.0394 REF
e		0.80 BSC		0.0315 BSC
b	0.30	0.40	0.0118	0.0157
c	0.13	0.19	0.0051	0.0075
Coplanarity		0.10 MAX		0.004 MAX
Ref: 32-PIN TQFP (GP00-D262)				

* Metric values (millimeters) should be used for PCB layout. English values (inches) are converted from metric values and may contain round-off errors.

Figure 14. Package Dimensions for Hummingbird Audio Codec – 32-Pin TQFP

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