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# HA16114P/PJ/FP/FPJ, HA16120FP/FPJ

## Switching Regulator for Chopper Type DC/DC Converter



ADE-204-020A (Z)

Rev.1  
Dec. 2000

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### Description

The HA16114P/FP/FPJ and HA16120FP/FPJ are single-channel PWM switching regulator controller ICs suitable for chopper-type DC/DC converters. Integrated totem-pole output circuits enable these ICs to drive the gate of a power MOSFET directly. The output logic of the HA16120 is designed to control a DC/DC step-up (boost) converter using an N-channel power MOS FET. The output logic of the HA16114 is designed to control a DC/DC step-down (buck) converter or inverting converter using a P-channel power MOS FET.

These ICs can operate synchronously with external pulse, a feature that makes them ideal for power supplies that use a primary-control AC/DC converter to convert commercial AC power to DC, then use one or more DC/DC converters on the secondary side to obtain multiple DC outputs. Synchronization is with the falling edge of the 'sync' pulse, which can be the secondary output pulse from a flyback transformer. Synchronization eliminates the beat interference that can arise from different operating frequencies of the AC/DC and DC/DC converters, and reduces harmonic noise. Synchronization with an AC/DC converter using a forward transformer is also possible, by inverting the 'sync' pulse.

Overcurrent protection features include a pulse-by-pulse current limiter that can reduce the width of individual PWM pulses, and an intermittent operating mode controlled by an on-off timer. Unlike the conventional latched shutdown function, the intermittent operating function turns the IC on and off at controlled intervals when pulse-by-pulse current limiting continues for a programmable time. This results in sharp vertical settling characteristics. Output recovers automatically when the overcurrent condition subsides.

Using these ICs, a compact, highly efficient DC/DC converter can be designed easily, with a reduced number of external components.

### Functions

- 2.5 V voltage reference
- Sawtooth oscillator (Triangle wave)
- Overcurrent detection
- External synchronous input
- Totem-pole output

# HA16114P/PJ/FP/FPJ, HA16120FP/FPJ

- Undervoltage lockout (UVL)
- Error amplifier
- Vref overvoltage protection (OVP)

## Features

- Wide supply voltage range: 3.9 V to 40 V\*
- Maximum operating frequency: 600 kHz
- Able to drive a power MOS FET ( $\pm 1$  A maximum peak current) by the built-in totem-pole gate pre-driver circuit
- Can operate in synchronization with an external pulse signal, or with another controller IC
- Pulse-by-pulse overcurrent limiting (OCL)
- Intermittent operation under continuous overcurrent
- Low quiescent current drain when shut off by grounding the ON/OFF pin  
 HA16114:  $I_{OFF} = 10 \mu\text{A}$  (max)  
 HA16120:  $I_{OFF} = 150 \mu\text{A}$  (max)
- Externally trimmable reference voltage (Vref):  $\pm 0.2$  V
- Externally adjustable undervoltage lockout points (with respect to  $V_{IN}$ )
- Stable oscillator frequency
- Soft start and quick shut function

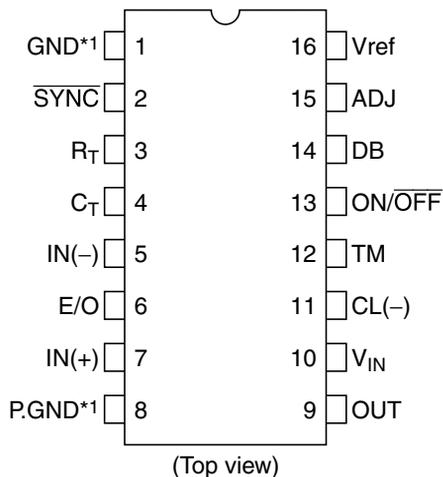
Note: The reference voltage 2.5 V is under the condition of  $V_{IN} \geq 4.5$  V.

## Ordering Information

### Hitachi Control ICs for Chopper-Type DC/DC Converters

Channels	Product Number	Channel No.	Control Functions			Output Circuits	Overcurrent Protection
			Step-Up	Step-Down	Inverting		
Dual	HA17451	Ch 1	—	—	—	Open collector	SCP with timer (latch)
		Ch 2	—	—	—		
Single	HA16114	—	—	—	—	Totem pole power MOS FET driver	Pulse-by-pulse current limiter and intermittent operation by on/off timer
	HA16120	—	—	—	—		
Dual	HA16116	Ch 1	—	—	—		
		Ch 2	—	—	—		
	HA16121	Ch 1	—	—	—		
		Ch 2	—	—	—		

## Pin Arrangement

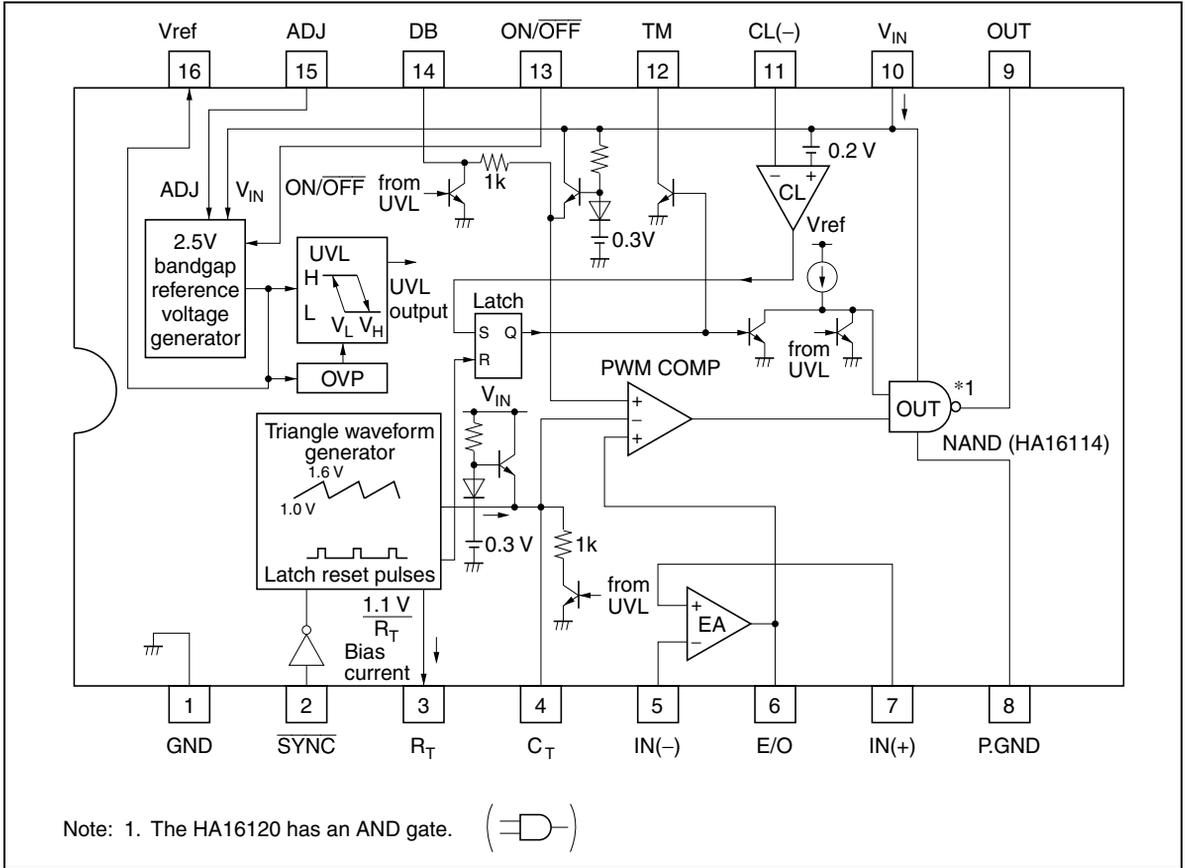


Note: 1. Pin 1 (GND) and Pin 8 (P.GND) must be connected each other with external wire.

## Pin Description

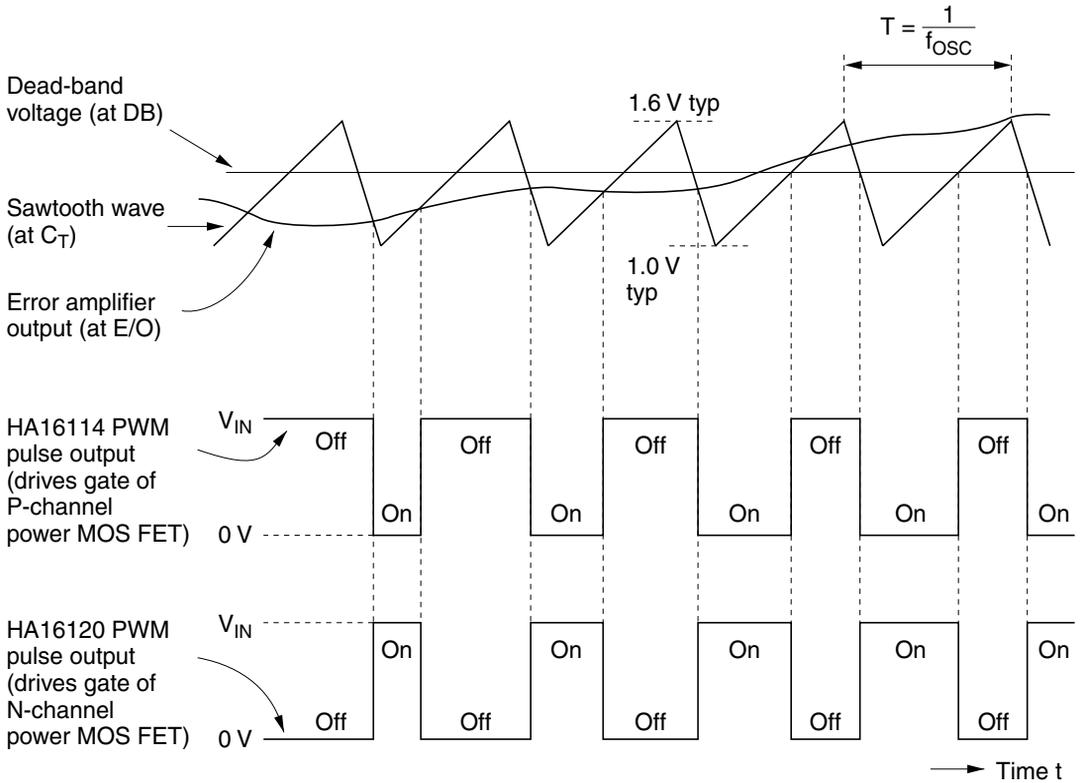
Pin No.	Symbol	Function
1	GND	Signal ground
2	$\overline{\text{SYNC}}$	External sync signal input (synchronized with falling edge)
3	$R_T$	Oscillator timing resistor connection (bias current control)
4	$C_T$	Oscillator timing capacitor connection (sawtooth voltage output)
5	IN(-)	Inverting input to error amplifier
6	E/O	Error amplifier output
7	IN(+)	Non-inverting input to error amplifier
8	P.GND	Power ground
9	OUT	Output (pulse output to gate of power MOS FET)
10	$V_{IN}$	Power supply input
11	CL(-)	Inverting input to current limiter
12	TM	Timer setting for intermittent shutdown when overcurrent is detected (sinks timer transistor current)
13	$\overline{\text{ON/OFF}}$	IC on/off control (off below approximately 0.7 V)
14	DB	Dead-band duty cycle control input
15	ADJ	Reference voltage (Vref) adjustment input
16	Vref	2.5 V reference voltage output

## Block Diagram



Timing Waveforms

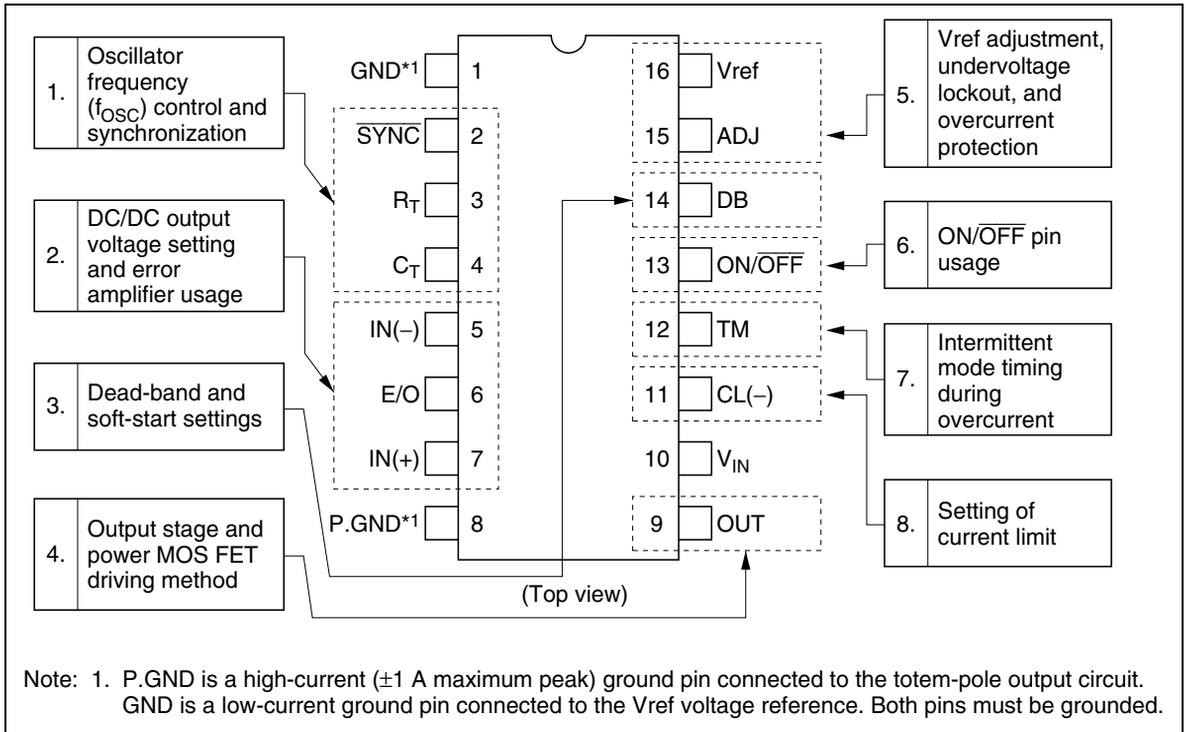
Generation of PWM pulse output from sawtooth wave (during steady-state operation)



Note: On duty =  $\frac{t_{ON}}{T}$

## Guide to the Functional Description

The description covers the topics indicated below.



### 1. Sawtooth Oscillator (Triangle Wave)

#### 1.1 Operation and Frequency Control

The sawtooth wave is a voltage waveform from which the PWM pulses are created (See figure 1). The sawtooth oscillator operates as follows. A constant current  $I_0$  determined by an external timing resistor  $R_T$  is fed continuously to an external timing capacitor  $C_T$ . When the  $C_T$  pin voltage exceeds a comparator threshold voltage  $V_{TH}$ , the comparator output opens a switching transistor, allowing a  $3I_0$  discharge current to flow from  $C_T$ . When the  $C_T$  pin voltage drops below a threshold voltage  $V_{TL}$ , the comparator output closes the switching transistor, stopping the  $3I_0$  discharge. Repetition of these operations generates a sawtooth wave.

The value of  $I_0$  is  $1.1 \text{ V}/R_T \text{ } \Omega$ . The  $I_0$  current mirror has a limited current capacity, so  $R_T$  should be at least  $5 \text{ k}\Omega$  ( $I_0 \leq 220 \text{ } \mu\text{A}$ ).

Internal resistances  $R_A$ ,  $R_B$ , and  $R_C$  set the peak and valley voltages  $V_{TH}$  and  $V_{TL}$  of the sawtooth waveform at approximately  $1.6 \text{ V}$  and  $1.0 \text{ V}$ .



## 1.2 External Synchronization

These ICs have a sync input pin so that they can be synchronized to a primary-control AC/DC converter. Pulses from the secondary winding of the switching transformer should be dropped through a resistor voltage divider to the sync input pin. Synchronization takes place at the falling edge, which is optimal for multiple-output power supplies that synchronize with a flyback AC/DC converter.

The sync input pin ( $\overline{\text{SYNC}}$ ) is connected internally through a synchronizing circuit to the sawtooth oscillator to synchronize the sawtooth waveform (see figure 1.2).

- Synchronization is with the falling edge of the external sync signal.
- The frequency of the external sync signal must be in the range  $f_{\text{osc}} < f_{\overline{\text{SYNC}}} < f_{\text{osc}} \times 2$ .
- The duty cycle of the external sync signal must be in the range  $5\% < t_1/t_2 < 50\%$  ( $t_1 = 300 \text{ ns Min}$ ).
- With external synchronization,  $V_{\text{TH}}'$  can be calculated as follows.

$$V_{\text{TH}}' = (V_{\text{TH}} - V_{\text{TL}}) \times \frac{f_{\text{OSC}}}{f_{\overline{\text{SYNC}}}} + V_{\text{TL}}$$

Note: When not using external synchronization, connect the  $\overline{\text{SYNC}}$  pin to the Vref pin.

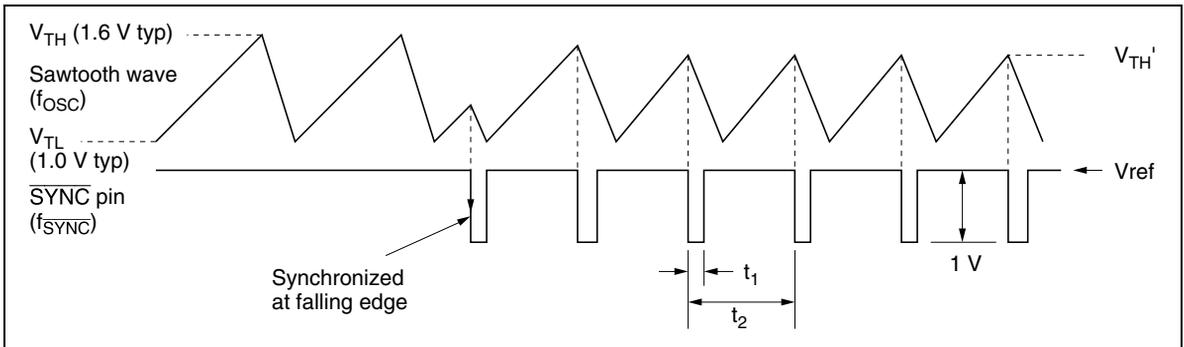
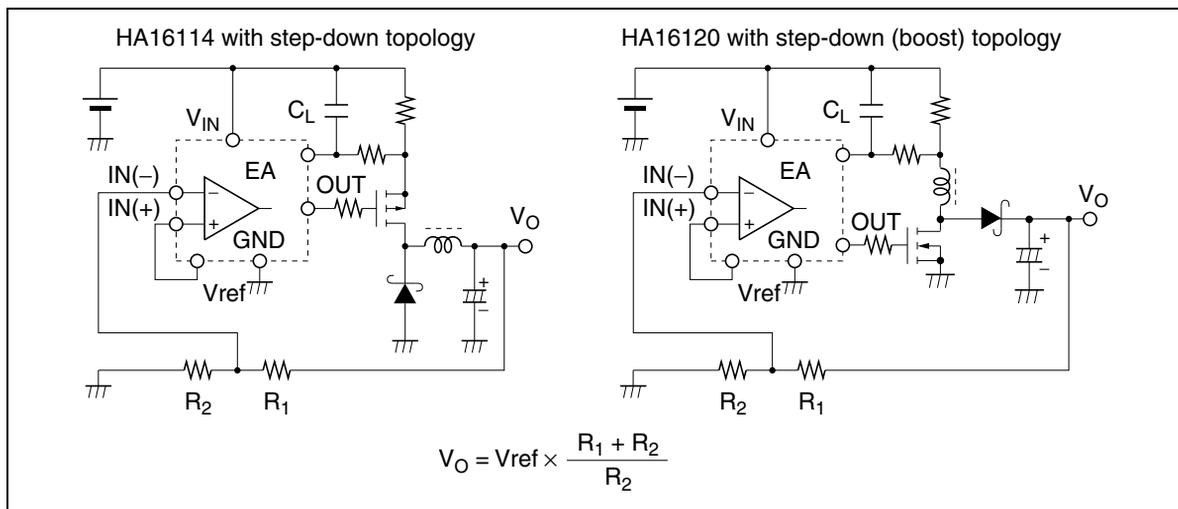


Figure 1.2 External Synchronization

## 2. DC/DC Output Voltage Setting and Error Amplifier Usage

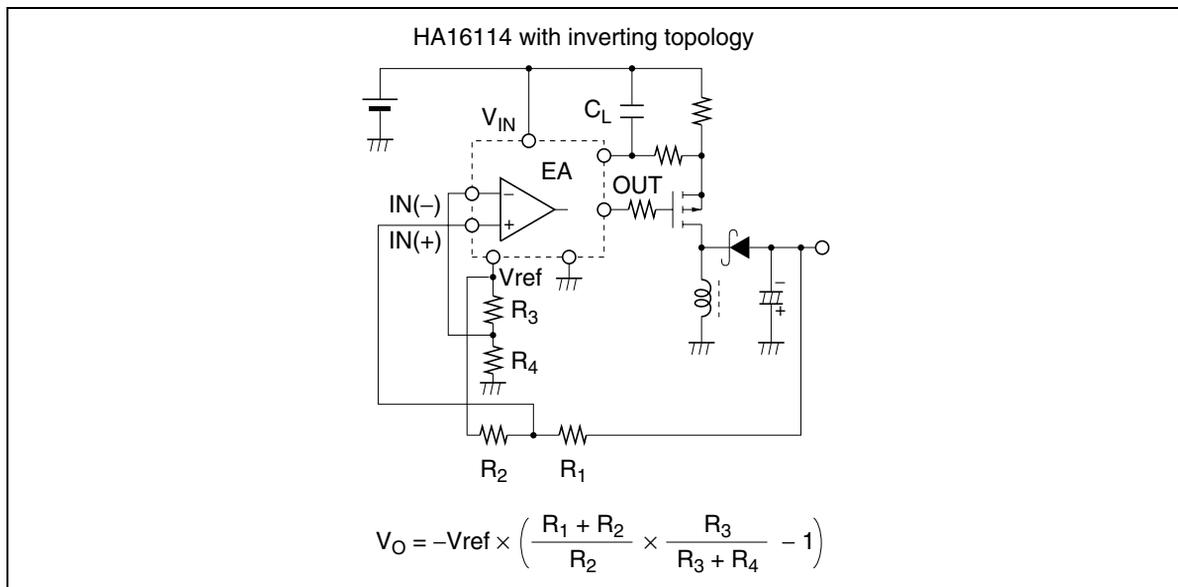
### 2.1 DC/DC Output Voltage Setting

#### 1. Positive Output Voltage ( $V_o > V_{ref}$ )



**Figure 2.1 Output Voltage Setting (1)**

#### 2. Negative Output Voltage ( $V_o < 0$ V)

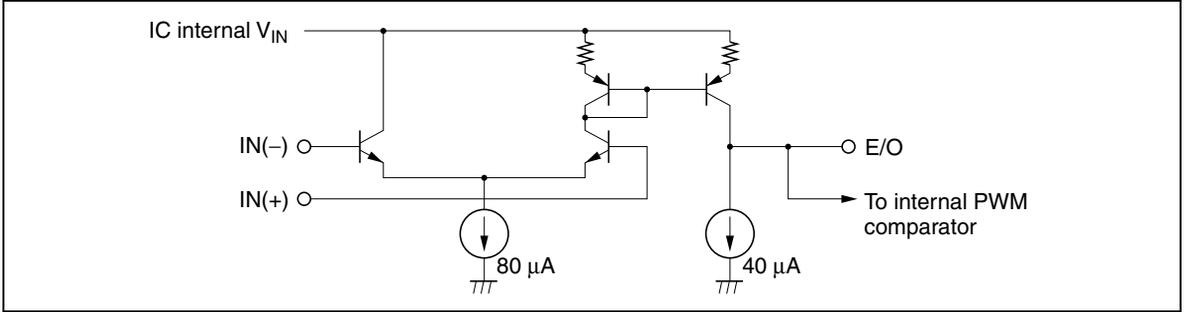


**Figure 2.2 Output Voltage Setting (2)**

## 2.2 Error Amplifier Usage

Figure 2.3 shows an equivalent circuit of the error amplifier. The error amplifier in these ICs is a simple NPN-transistor differential amplifier with a constant-current-driven output circuit.

The amplifier combines a wide bandwidth ( $f_T = 4 \text{ MHz}$ ) with a low open-loop gain (50 dB Typ), allowing stable feedback to be applied when the power supply is designed. Phase compensation is also easy.



**Figure 2.3 Error Amplifier Equivalent Circuit**

## 3. Dead-Band Duty Cycle and Soft-Start Settings

### 3.1 Dead-Band Duty Cycle Setting

The dead-band duty cycle (the maximum duty cycle of the PWM pulse output) can be programmed by the voltage  $V_{DB}$  at the DB pin. A convenient way to obtain  $V_{DB}$  is to divide the IC's  $V_{ref}$  output by two external resistors. The dead-band duty cycle (DB) and  $V_{DB}$  can be calculated as follows.

$$DB = \frac{V_{TH} - V_{DB}}{V_{TH} - V_{TL}} \times 100 (\%) \quad \dots \text{ This applies when } V_{DB} > V_{TL}.$$

If  $V_{DB} < V_{TL}$ , there is no PWM output.

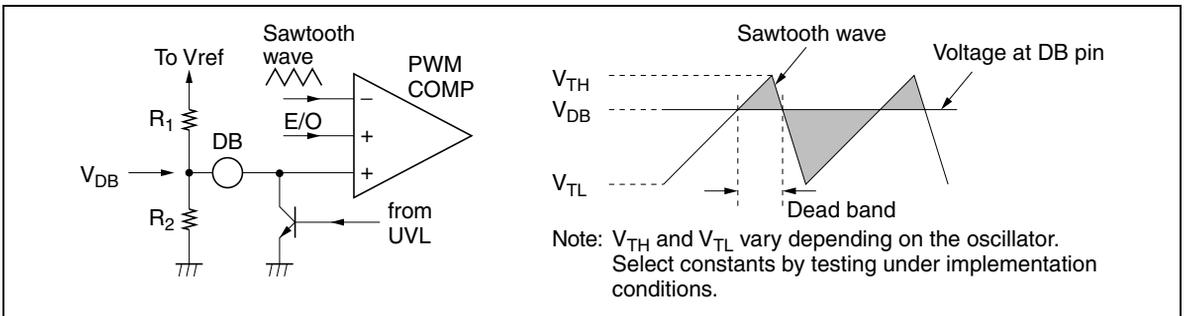
$$V_{DB} = V_{ref} \times \frac{R_2}{R_1 + R_2}$$

Note:  $V_{DB}$  is the voltage at the DB pin.

$V_{TH}$ : 1.6 V (Typ)

$V_{TL}$ : 1.0 V (Typ)

$V_{ref}$  is typically 2.5 V. Select  $R_1$  and  $R_2$  so that  $1.0 \text{ V} \leq V_{DB} \leq 1.6 \text{ V}$ .



**Figure 3.1 Dead-Band Duty Cycle Setting**

### 3.2 Soft-Start Setting

Soft-start avoids overshoot at power-up by widening the PWM output pulses gradually, so that the converted DC output rises slowly. Soft-start is programmed by connecting a capacitor between the DB pin and ground. The soft-start time is determined by the time constant of this capacitor and the resistors that set the voltage at the DB pin.

$$t_{\text{soft}} = -C_1 \times R \times \ln \left( 1 - \frac{V_x}{V_{\text{DB}}} \right)$$

$$R = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$V_{\text{DB}} = V_{\text{ref}} \times \frac{R_2}{R_1 + R_2}$$

Note:  $V_x$  is the voltage at the DB pin after time  $t$  ( $V_x < V_{\text{DB}}$ ).

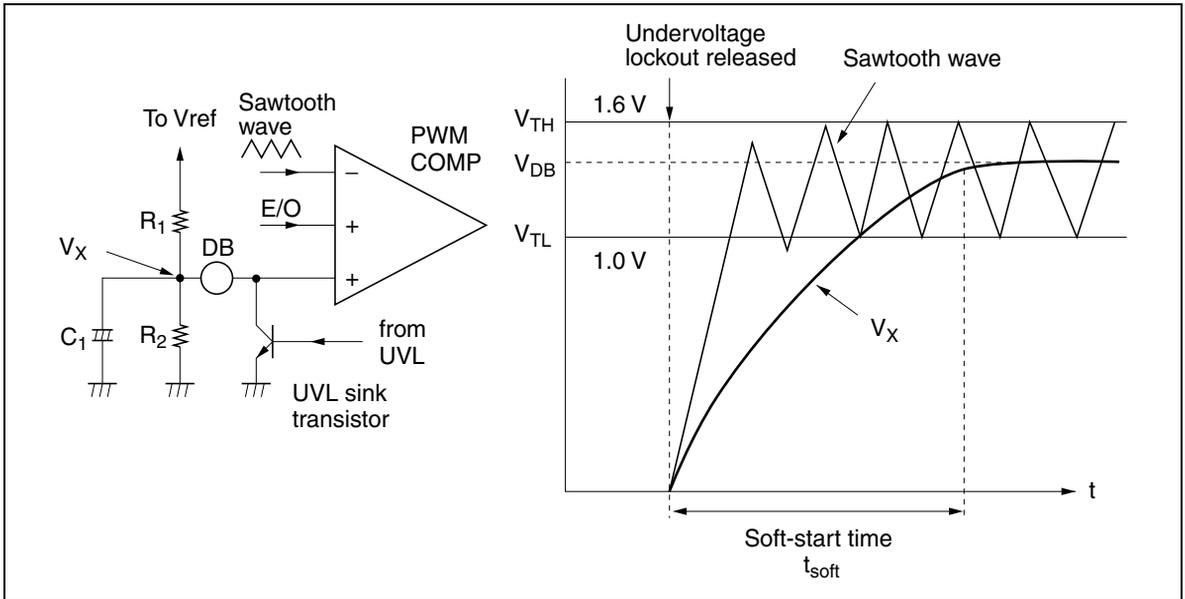


Figure 3.2 Soft-Start Setting

### 3.3 Quick Shutdown

The quick shutdown function resets the voltages at all pins when the IC is turned off, to assure that PWM pulse output stops quickly. Since the UVL pull-down resistor in the IC remains on even when the IC is turned off, the sawtooth wave output, error amplifier output, and DB pin are all reset to low voltage.

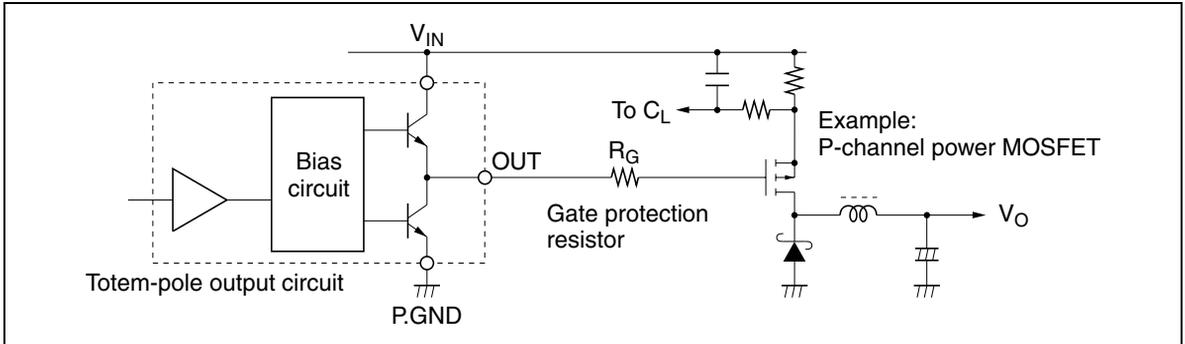
This feature helps in particular to discharge capacitor  $C_1$  in figure 3.2, which has a comparatively large capacitance. In intermittent mode (explained on a separate page), this feature enables the IC to soft-start in each on-off cycle.

## 4. PWM Output Circuit and Power MOSFET Driving Method

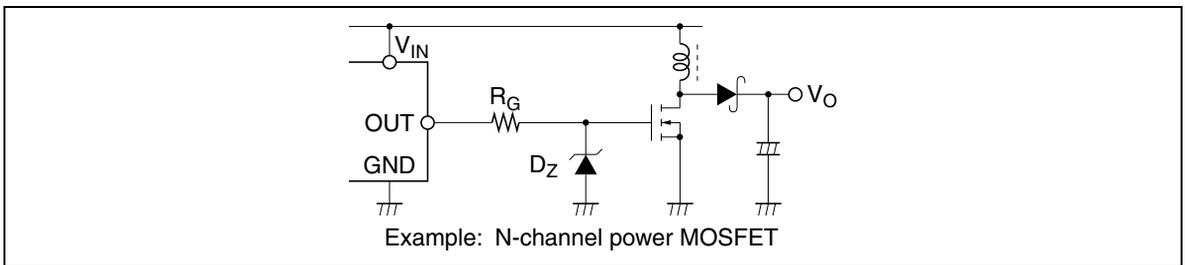
These ICs have built-in totem-pole push-pull drive circuits that can drive a power MOS FET as shown in figure 4.1. The power MOS FET can be driven directly through a gate protection resistor.

If  $V_{IN}$  exceeds the gate breakdown voltage of the power MOS FET additional protective measures should be taken, e.g. by adding Zener diodes as shown in figure 4.2.

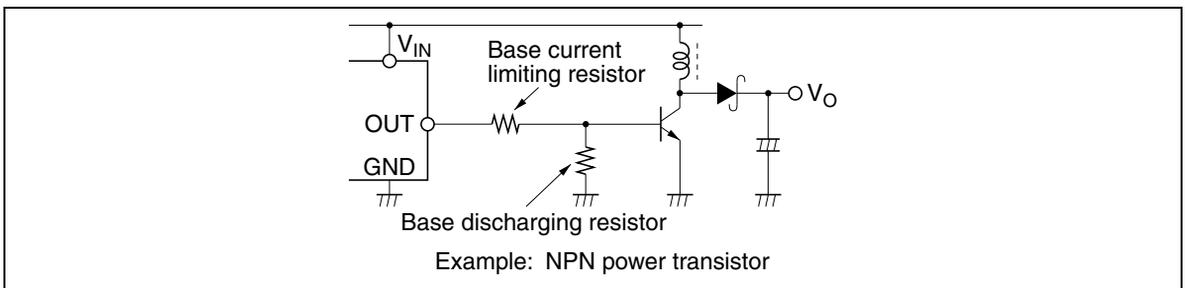
To drive a bipolar power transistor, the base should be protected by voltage and current dividing resistors as shown in figure 4.3.



**Figure 4.1 Connection of Output Stage to Power MOS FET**



**Figure 4.2 Gate Protection by Zener Diodes**



**Figure 4.3 Driving a Bipolar Power Transistor**

5. Voltage Reference (Vref = 2.5 V)

5.1 Voltage Reference

A bandgap reference built into the IC (see figure 5.1) outputs 2.5 V ± 50 mV. The sawtooth oscillator, PWM comparator, latch, and other internal circuits are powered by this 2.5 V and an internally-generated voltage of approximately 3.2 V.

The voltage reference section shut downs when the IC is turned off at the ON/OFF pin as described later, saving current when the IC is not used and when it operates in intermittent mode during overcurrent.

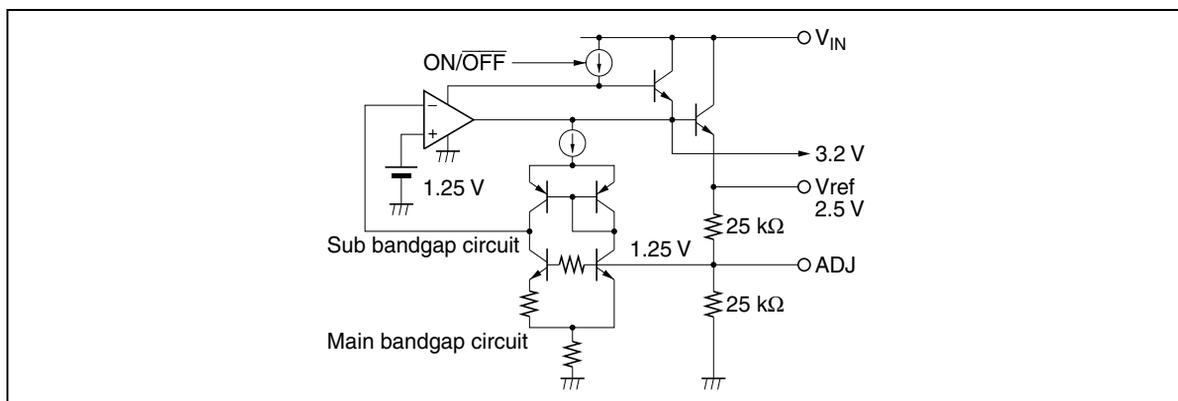


Figure 5.1 Vref Reference Circuit

5.2 Trimming the Reference Voltage (Vref and ADJ pins)

Figure 5.2 shows a simplified circuit equivalent to figure 5.1. The ADJ pin in this circuit is provided for trimming the reference voltage (Vref). The output at the ADJ pin is a voltage  $V_{ADJ}$  of 1.25 V (Typ) generated by the bandgap circuit. Vref is determined by  $V_{ADJ}$  and the ratio of internal resistors  $R_1$  and  $R_2$  as follows:

$$V_{ref} = V_{ADJ} \times \frac{R_1 + R_2}{R_2}$$

The design values of  $R_1$  and  $R_2$  are 25 kΩ with a tolerance of ±25%.

If trimming is not performed, the ADJ pin open can be left open.

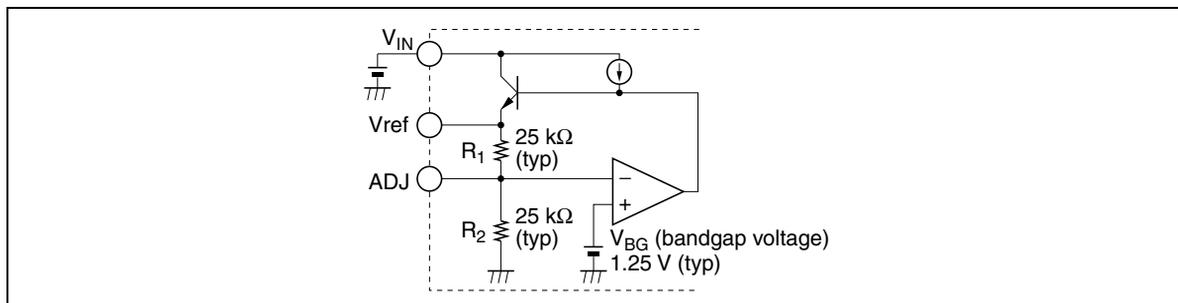


Figure 5.2 Simplified Diagram of Voltage Reference Circuit

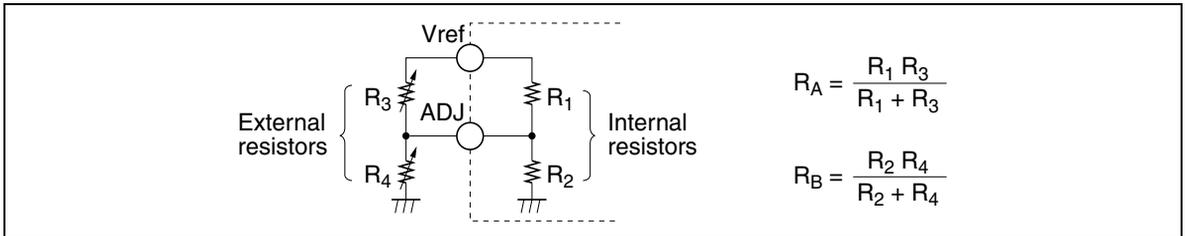
The relation between Vref and the ADJ pin enables Vref to be trimmed by inserting one external resistor (R<sub>3</sub>) between the Vref and ADJ pins and another (R<sub>4</sub>) between the ADJ pin and ground, to change the resistance ratio. Vref is then determined by the combined resistance ratio of the internal R<sub>1</sub> and R<sub>2</sub> and external R<sub>3</sub> and R<sub>4</sub>.

$$V_{ref} = V_{ADJ} \times \frac{R_A + R_B}{R_B}$$

Where, R<sub>A</sub>: parallel resistance of R<sub>1</sub> and R<sub>3</sub>

R<sub>B</sub>: parallel resistance of R<sub>2</sub> and R<sub>4</sub>

Although Vref can be trimmed by R<sub>3</sub> or R<sub>4</sub> alone, to decrease the temperature dependence of Vref it is better to use two resistors having identical temperature coefficients. Vref can be trimmed in the range of 2.5 V ± 0.2 V. Outside this range, the bandgap circuit will not operate and the IC may shut down.

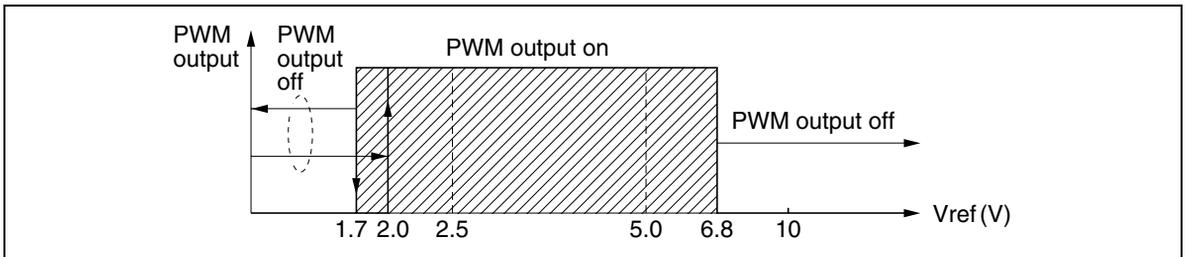


**Figure 5.3 Trimming of Reference Voltage**

### 5.3 Vref Undervoltage Lockout and Overvoltage Protection

The undervoltage lockout (UVL) function turns off PWM pulse output when the input voltage (V<sub>IN</sub>) is low. In these ICs, this is done by monitoring the Vref voltage, which normally stays constant at approximately 2.5 V. The UVL circuit operates with hysteresis: it shuts PWM output off when Vref falls below 1.7 V, and turns PWM output back on when Vref rises above 2.0 V. Undervoltage lockout also provides protection in the event that Vref is shorted to ground.

The overvoltage protection circuit shuts PWM output off when Vref goes above 6.8 V. This provides protection in case the Vref pin is shorted to V<sub>IN</sub> or another high-voltage source.



**Figure 5.4 Vref Undervoltage Lockout and Overvoltage Protection**

UVL Voltage	Vref (V typ)	V <sub>IN</sub> (V typ)	Description
V <sub>H</sub>	2.0 V	3.6 V	V <sub>IN</sub> increasing: UVL releases; PWM output starts
V <sub>L</sub>	1.7 V	3.3 V	V <sub>IN</sub> decreasing: undervoltage lockout; PWM output stops

## 6. Usage of ON/OFF Pin

This pin is used for the following purposes:

- To shut down the IC while its input power remains on (power management)
- To externally alter the UVL release voltage
- With the timer (TM) pin, to operate in intermittent mode during overcurrent (see next section)

### 6.1 Shutdown by ON/OFF Pin Control

The IC can be shut down safely by bringing the voltage at the ON/OFF pin below about 0.7 V (the internal VBE value). This feature can be used in power supply systems to save power. When shut down, the HA16114 draws a maximum current ( $I_{OFF}$ ) of 10  $\mu$ A, while the HA16120 draws a maximum 150  $\mu$ A. The ON/OFF pin sinks 290  $\mu$ A (Typ) at 5 V, so it can be driven by TTL and other logic ICs. If intermittent mode will also be employed, use a logic IC with an open-collector or open-drain output.

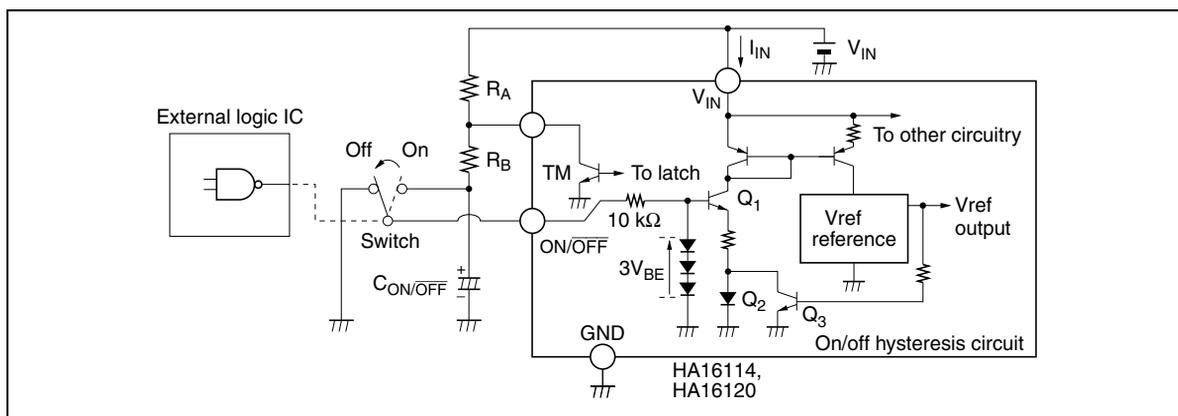


Figure 6.1 Shutdown by ON/OFF Pin Control

### 6.2 Adjustment of UVL Voltages (when not using intermittent mode)

These ICs permit external adjustment of the undervoltage lockout voltages. The adjustment is made by changing the undervoltage lockout thresholds  $V_{TH}$  and  $V_{TL}$  relative to  $V_{IN}$ , using the relationships shown in the accompanying diagrams.

When the IC is powered up, transistor  $Q_3$  is off, so  $V_{ON}$  is  $2V_{BE}$ , or about 1.4 V. Connection of resistors  $R_C$  and  $R_D$  in the diagram makes undervoltage lockout release at:

$$V_{IN} = 1.4 \text{ V} \times \frac{R_C + R_D}{R_D}$$

This  $V_{IN}$  is the supply voltage at which undervoltage lockout is released. At the release point  $V_{ref}$  is still below 2.5 V. To obtain  $V_{ref} = 2.5 \text{ V}$ ,  $V_{IN}$  must be at least about 4.3 V.

Since  $V_{ON/OFF}$  operates in relation to the base-emitter voltage of internal transistors,  $V_{ON}$  has a temperature coefficient of approximately  $-4 \text{ mV}/^\circ\text{C}$ . Keep this in mind when designing the power supply unit.

When undervoltage lockout and intermittent mode are both used, the intermittent-mode time constant is shortened, so the constants of external components may have to be altered.

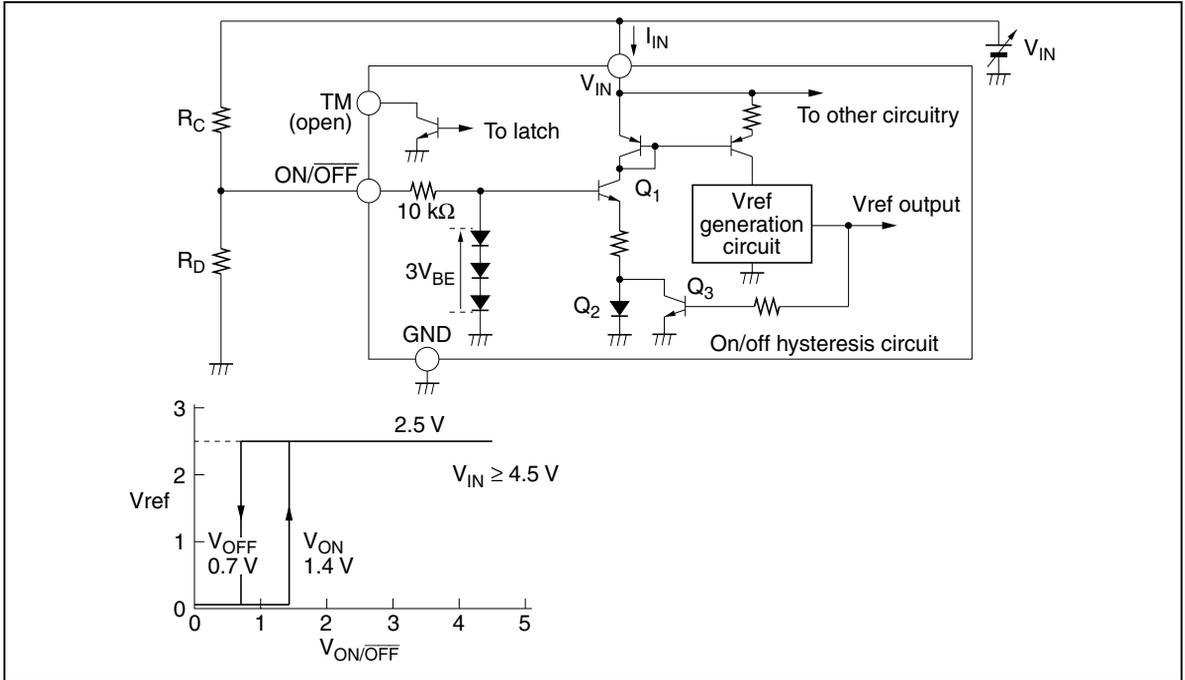


Figure 6.2 Adjustment of UVL Voltages

7. Timing of Intermittent Mode during Overcurrent

7.1 Principle of Operation

These ICs provide pulse-by-pulse overcurrent protection by sensing the current during each pulse and shutting off the pulse if overcurrent is detected. In addition, the TM and ON/OFF pins can be used to operate the IC in intermittent mode if the overcurrent state continues. A power supply with sharp settling characteristics can be designed in this way.

Intermittent mode operates by making use of the hysteresis of the ON/OFF pin threshold voltages  $V_{ON}$  and  $V_{OFF}$  ( $V_{ON} - V_{OFF} = V_{BE}$ ). The timing can be programmed as explained below.

When not using intermittent mode, leave the TM pin open, and pull the ON/OFF pin up to  $V_{ON}$  or higher. The  $V_{BE}$  is base emitter voltage of internal transistors.

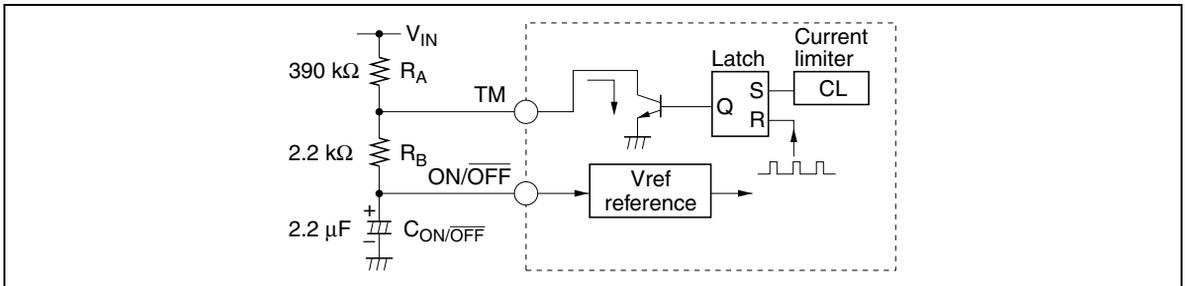


Figure 7.1 Connection Diagram (example)

7.2 Intermittent Mode Timing Diagram ( $V_{ON/OFF}$  only)

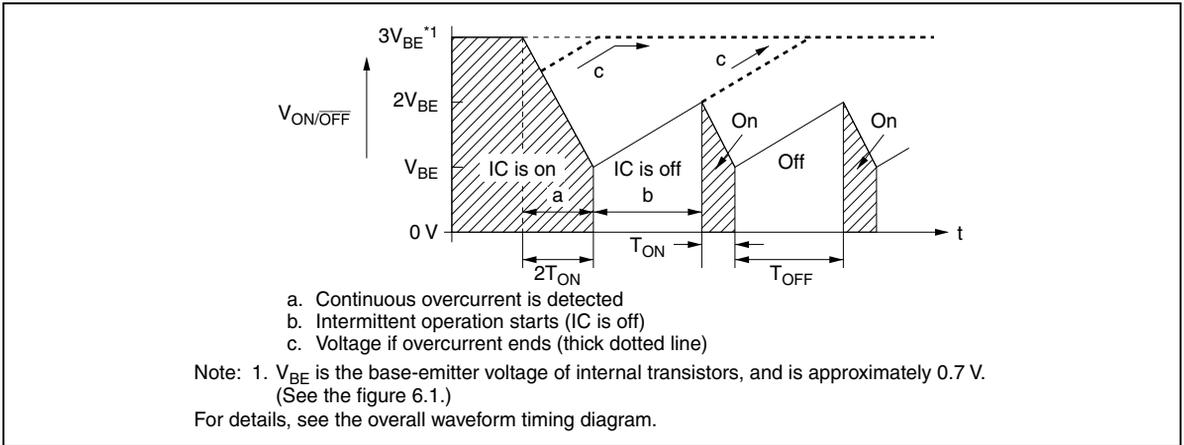


Figure 7.2 Intermittent Mode Timing Diagram ( $V_{ON/OFF}$  only)

7.3 Calculation of Intermittent Mode Timing

Intermittent mode timing is calculated as follows.

(1)  $T_{ON}$  (time until the IC shuts off when continuous overcurrent occurs)

$$T_{ON} = C_{ON/OFF} \times R_B \times \ln\left(\frac{2V_{BE}}{V_{BE}}\right) \times \left(\frac{1}{1 - \text{On duty}^*}\right)$$

$$= C_{ON/OFF} \times R_B \times \ln 2 \times \left(\frac{1}{1 - \text{On duty}^*}\right)$$

$$\approx 0.69 \times C_{ON/OFF} \times R_B \times \left(\frac{1}{1 - \text{On duty}^*}\right)$$

(2)  $T_{OFF}$  (time from when the IC shuts off until it next turns on)

$$T_{OFF} = C_{ON/OFF} \times (R_A + R_B) \times \ln\left(\frac{V_{IN} - V_{BE}}{V_{IN} - 2V_{BE}}\right)$$

Where  $V_{BE} \approx 0.7V$

The greater the overload, the sooner the pulse-by-pulse current limiter operates, the smaller  $t_{ON}$  becomes, and from the first equation (1) above, the smaller  $T_{ON}$  becomes. From the second equation (2),  $T_{OFF}$  depends on  $V_{IN}$ . Note that with the connections shown in the diagram, when  $V_{IN}$  is switched on the IC does not turn on until  $T_{OFF}$  has elapsed.

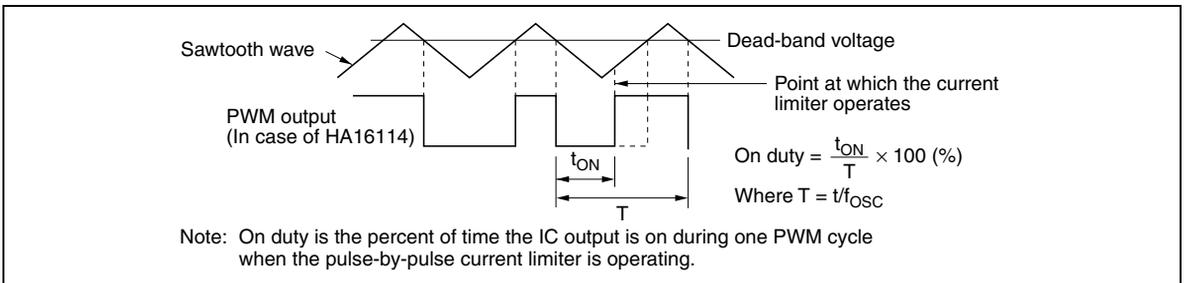


Figure 7.3

## 7.4 Examples of Intermittent Mode Timing (calculated values)

(1)  $T_{ON}$

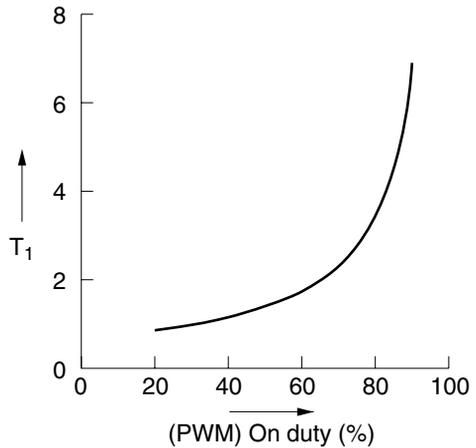
$$T_{ON} = T_1 \times C_{ON/OFF} \times R_B$$

Here, coefficient

$$T_1 = 0.69 \times \frac{1}{1 - \text{On duty}}$$

from section 7.3 (1) previously.

Example: If  $C_{ON/OFF} = 2.2 \mu\text{F}$ ,  
 $R_B = 2.2 \text{ k}\Omega$ , and the on duty  
of the current limiter is 75%,  
then  $T_{ON} = 13 \text{ ms}$ .



**Figure 7.4 Examples of Intermittent Mode Timing (1)**

(2)  $T_{OFF}$

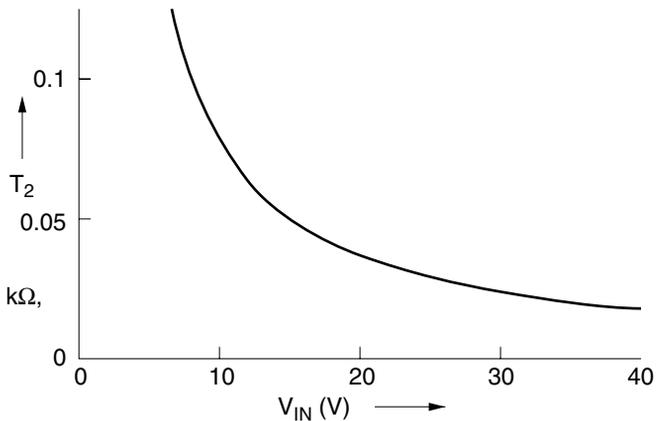
$$T_{OFF} = T_2 \times C_{ON/OFF} \times (R_A + R_B)$$

Here, coefficient

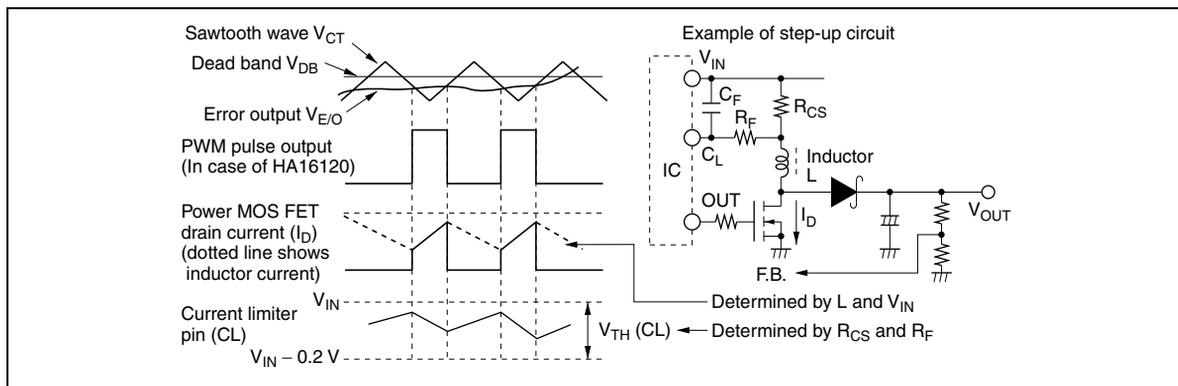
$$T_2 = \ln \frac{V_{IN} - V_{BE}}{V_{IN} - 2V_{BE}}$$

from section 7.3 (2) previously.

Example: If  $C_{ON/OFF} = 2.2 \mu\text{F}$ ,  $R_B = 2.2 \text{ k}\Omega$ ,  
 $R_A = 390 \text{ k}\Omega$ ,  $V_{IN} = 12 \text{ V}$ ,  
then  $T_{OFF} = 55 \text{ ms}$ .



**Figure 7.5 Examples of Intermittent Mode Timing (2)**



**Figure 7.6**

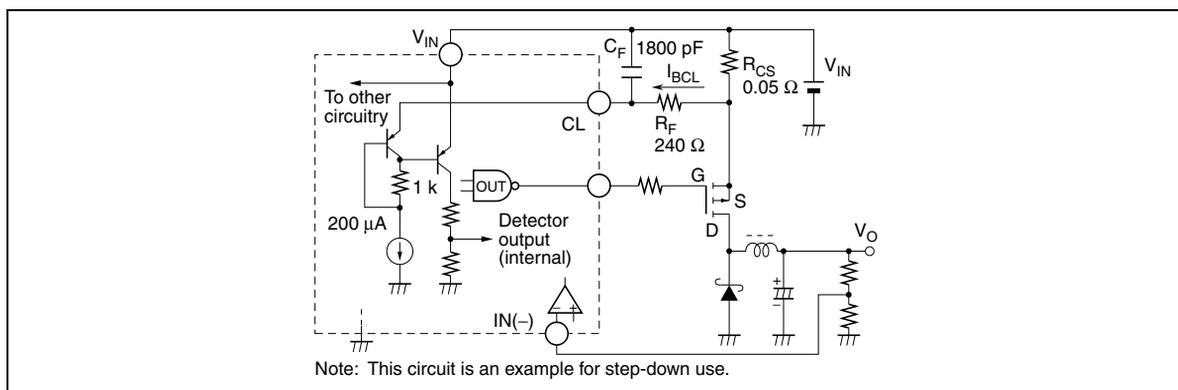
## 8. Setting the Overcurrent Detection Threshold

The voltage drop  $V_{TH}$  at which overcurrent is detected in these ICs is typically 0.2 V. The bias current is typically 200  $\mu\text{A}$ . The power MOS FET peak current value before the current limiter goes into operation is given as follows.

$$I_D = \frac{V_{TH} - (R_F + R_{CS}) \times I_{BCL}}{R_{CS}}$$

Where,  $V_{TH} = V_{IN} - V_{CL} = 0.2 \text{ V}$ ,  $V_{CL}$  is a voltage referred on GND.

Note that  $R_F$  and  $C_F$  form a low-pass filter with a cutoff frequency determined by their RC time constant. This filter prevents incorrect operation due to current spikes when the power MOS FET is switched on or off.



**Figure 8.1 Example for Step-Down Use**

With the values shown in the diagram, the peak current is:

$$I_D = \frac{0.2 \text{ V} - (240 \Omega + 0.05 \Omega) \times 200 \mu\text{A}}{0.05 \Omega} = 3.04 \text{ A}$$

The filter cutoff frequency is calculated as follows:

$$f_c = \frac{1}{2\pi C_F R_F} = \frac{1}{6.28 \times 1800 \text{ pF} \times 240 \Omega} = 370 \text{ kHz}$$

## Absolute Maximum Ratings

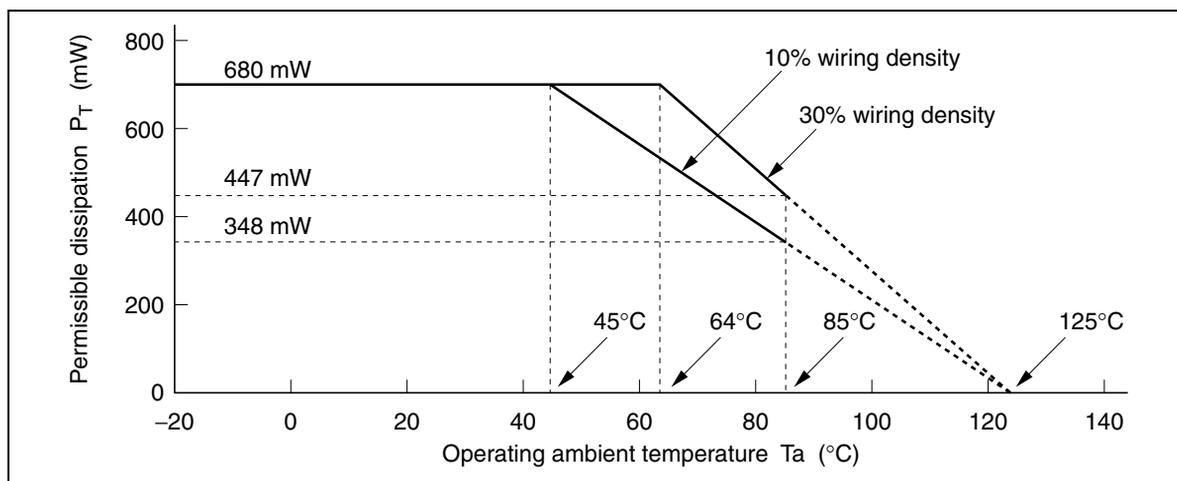
(Ta = 25°C)

Item	Symbol	Rating		Unit
		HA16114P/FP, HA16120FP	HA16114PJ/FPJ, HA16120FPJ	
Supply voltage	V <sub>IN</sub>	40	40	V
Output current (DC)	I <sub>O</sub>	±0.1	±0.1	A
Output current (peak)	I <sub>O peak</sub>	±1.0	±1.0	A
Current limiter input voltage	V <sub>CL</sub>	V <sub>IN</sub>	V <sub>IN</sub>	V
Error amplifier input voltage	V <sub>IEA</sub>	V <sub>IN</sub>	V <sub>IN</sub>	V
E/O input voltage	V <sub>IE/O</sub>	V <sub>ref</sub>	V <sub>ref</sub>	V
RT source current	I <sub>RT</sub>	500	500	μA
TM sink current	I <sub>TM</sub>	3	3	mA
SYNC voltage	V <sub>SYNC</sub>	V <sub>ref</sub>	V <sub>ref</sub>	V
SYNC current	I <sub>SYNC</sub>	±250	±250	μA
Power dissipation	P <sub>T</sub>	680*1, *2	680*1, *2	mW
Operating temperature	Topr	-20 to +85	-40 to +85	°C
Junction temperature	TjMax	125	125	°C
Storage temperature	Tstg	-55 to +125	-55 to +125	°C

Notes: 1. This value is for an SOP package (FP) and is based on actual measurements on a 40 × 40 × 1.6 mm glass epoxy circuit board. With a 10% wiring density, this value is permissible up to Ta = 45°C and should be derated by 8.3 mW/°C at higher temperatures. With a 30% wiring density, this value is permissible up to Ta = 64°C and should be derated by 11.1 mW/°C at higher temperatures.

2. For the DILP package.

This value applies up to Ta = 45°C; at temperatures above this, 8.3 mW/°C derating should be applied.

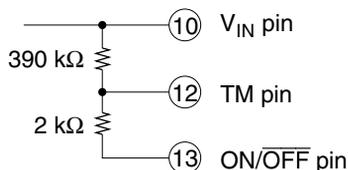


## Electrical Characteristics

( $T_a = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $f_{OSC} = 100\text{ kHz}$ )

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes	
Voltage reference section	Output voltage	Vref	2.45	2.50	2.55	V	$I_o = 1\text{ mA}$	
	Line regulation	Line	—	2	60	mV	$4.5\text{ V} \leq V_{IN} \leq 40\text{ V}$	1
	Load regulation	Load	—	30	60	mV	$0 \leq I_o \leq 10\text{ mA}$	
	Short-circuit output current	$I_{OS}$	10	24	—	mA	$V_{ref} = 0\text{ V}$	
	Vref overvoltage protection threshold	Vrovp	6.2	6.8	7.4	V		
	Temperature stability of output voltage	$\Delta V_{ref}/\Delta T_a$	—	100	—	ppm/ $^\circ\text{C}$		
	Vref adjustment voltage	$V_{ADJ}$	1.225	1.25	1.275	V		
Sawtooth oscillator section	Maximum frequency	fmax	600	—	—	kHz		
	Minimum frequency	fmin	—	—	1	Hz		
	Frequency stability with input voltage	$\Delta f/f_{01}$	—	$\pm 1$	$\pm 3$	%	$4.5\text{ V} \leq V_{IN} \leq 40\text{ V}$ $(f_{01} = (f_{max} + f_{min})/2)$	
	Frequency stability with temperature	$\Delta f/f_{02}$	—	$\pm 5$	—	%	$-20^\circ\text{C} \leq T_a \leq 85^\circ\text{C}$ $(f_{02} = (f_{max} + f_{min})/2)$	
	Oscillator frequency	$f_{OSC}$	90	100	110	kHz	$R_T = 10\text{ k}\Omega$ $C_T = 1300\text{ pF}$	
Dead-band adjustment section	Low level threshold voltage	$V_{TL}$	0.9	1.0	1.1	V	Output duty cycle: 0% on	
	High level threshold voltage	$V_{TH}$	1.5	1.6	1.7	V	Output duty cycle: 100% on	
	Threshold difference	$\Delta V_{TH}$	0.5	0.6	0.7	V	$\Delta V_{TH} = V_{TH} - V_{TL}$	
	Output source current	$I_{source}$	170	250	330	$\mu\text{A}$	DB pin: 0 V	
PWM comparator section	Low level threshold voltage	$V_{TL}$	0.9	1.0	1.1	V	Output duty cycle: 0% on	
	High level threshold voltage	$V_{TH}$	1.5	1.6	1.7	V	Output duty cycle: 100% on	
	Threshold difference	$\Delta V_{TH}$	0.5	0.6	0.7	V	$\Delta V_{TH} = V_{TH} - V_{TL}$	

Note: 1. Resistors connected to ON/OFF pin:



# HA16114P/PJ/FP/FPJ, HA16120FP/FPJ

## Electrical Characteristics (cont.)

( $T_a = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $f_{OSC} = 100\text{ kHz}$ )

Item		Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Error amplifier section	Input offset voltage	$V_{IO}$	—	2	10	mV		
	Input bias current	$I_B$	—	0.5	2.0	$\mu\text{A}$		
	Output sink current	$I_{O\text{sink}}$	28	40	52	$\mu\text{A}$	$V_o = 2.5\text{ V}$	
	Output source current	$I_{O\text{source}}$	28	40	52	$\mu\text{A}$	$V_o = 1.0\text{ V}$	
	Common-mode input voltage range	$V_{CM}$	1.1	—	3.7	V		
	Voltage gain	$A_V$	40	50	—	dB	$f = 10\text{ kHz}$	
	Unity gain bandwidth	BW	—	4	—	MHz		
	High level output voltage	$V_{OH}$	3.5	4.0	—	V	$I_o = 10\ \mu\text{A}$	
	Low level output voltage	$V_{OL}$	—	0.2	0.5	V	$I_o = 10\ \mu\text{A}$	
Overcurrent detection section	Threshold voltage	$V_{TH}$	$V_{IN}-0.22$	$V_{IN}-0.2$	$V_{IN}-0.18$	V		
	CL(-) bias current	$I_{BCL(-)}$	140	200	260	$\mu\text{A}$	$CL(-) = V_{IN}$	
	Turn-off time	$t_{OFF}$	—	200	300	ns		1
—			500	600	ns		2	
UVL section	Vref high level threshold voltage	$V_{TH}$	1.7	2.0	2.3	V		
	Vref low level threshold voltage	$V_{TL}$	1.4	1.7	2.0	V		
	Threshold difference	$\Delta V_{TH}$	0.1	0.3	0.5	V	$\Delta V_{TH} = V_{TH} - V_{TL}$	
	VIN high level threshold voltage	$V_{INH}$	3.3	3.6	3.9	V		
	VIN low level threshold voltage	$V_{INL}$	3.0	3.3	3.6	V		

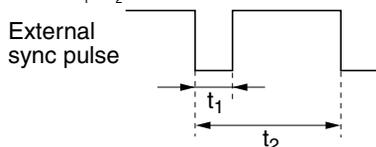
Notes: 1. HA16114 only.  
2. HA16120 only.

## Electrical Characteristics (cont.)

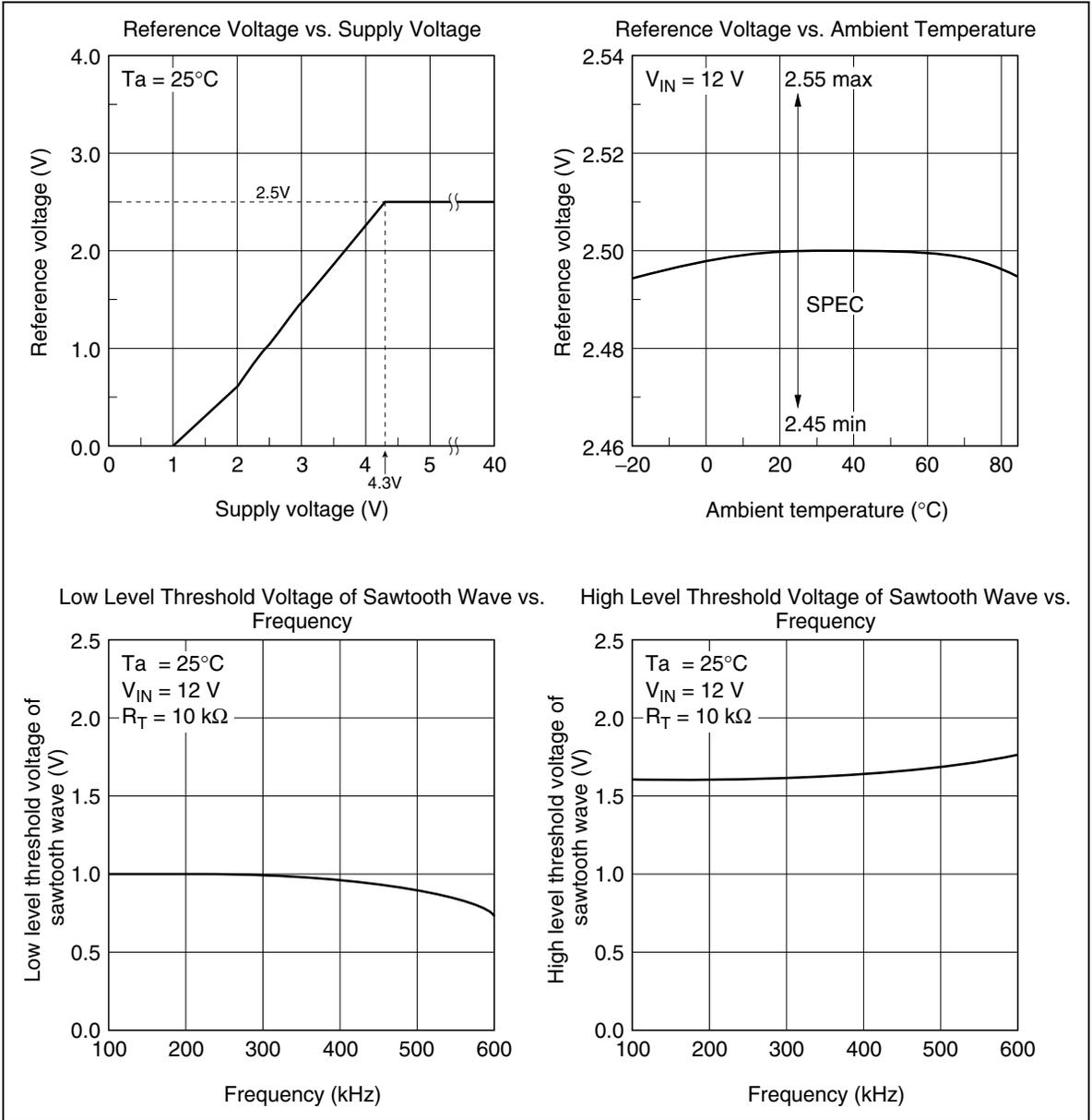
( $T_a = 25^\circ\text{C}$ ,  $V_{IN} = 12\text{ V}$ ,  $f_{OSC} = 100\text{ kHz}$ )

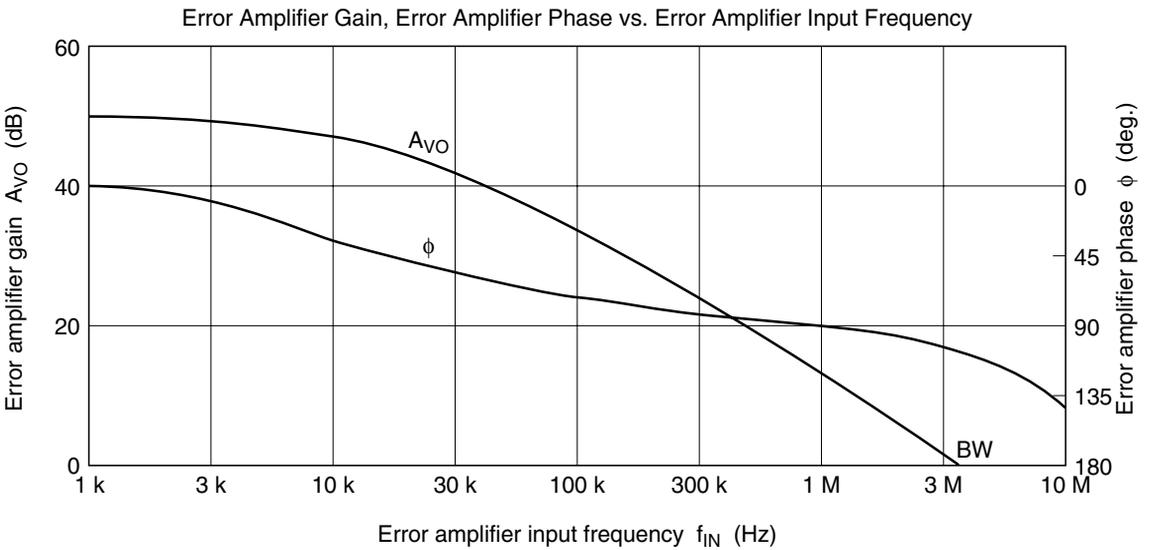
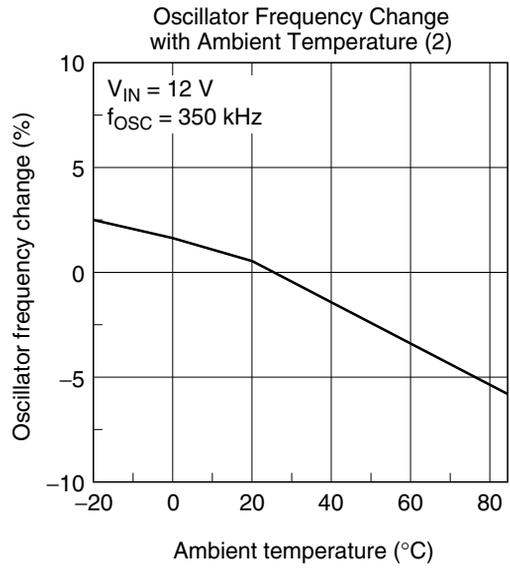
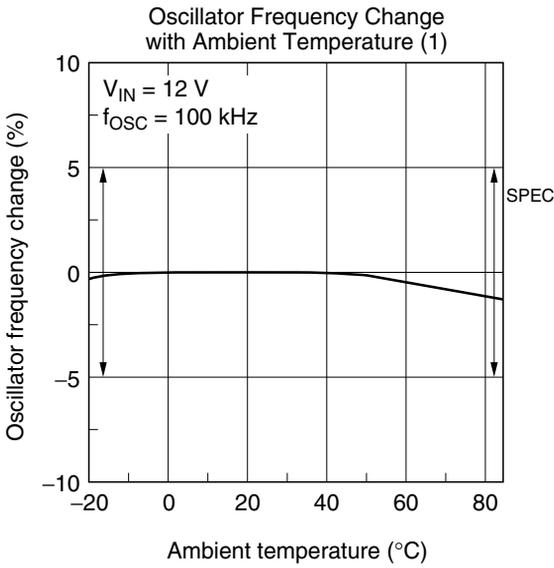
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes	
Output stage	Output low voltage	$V_{OL}$	—	0.9	1.5	V	$I_{O\text{sink}} = 10\text{ mA}$	
	Output high voltage	$V_{OH1}$	$V_{IN}-2.2$	$V_{IN}-1.6$	—	V	$I_{O\text{source}} = 10\text{ mA}$	
	High voltage when off	$V_{OH2}$	$V_{IN}-2.2$	$V_{IN}-1.6$	—	V	$I_{O\text{source}} = 1\text{ mA}$ ON/OFF pin: 0 V	1
	Low voltage when off	$V_{OL2}$	—	0.9	1.5	V	$I_{O\text{sink}} = 1\text{ mA}$ ON/OFF pin: 0 V	2
	Rise time	$t_r$	—	50	200	ns	$C_L = 1000\text{ pF}$	
	Fall time	$t_f$	—	50	200	ns	$C_L = 1000\text{ pF}$	
External sync section	$\overline{\text{SYNC}}$ source current	$I_{\overline{\text{SYNC}}}$	120	180	240	$\mu\text{A}$	$\overline{\text{SYNC}}$ pin: 0 V	
	Sync input frequency range	$f_{\overline{\text{SYNC}}}$	$f_{OSC}$	—	$f_{OSC} \times 2$	kHz		
	External sync initiation voltage	$V_{\overline{\text{SYNC}}}$	$V_{ref}-1.0$	—	$V_{ref}-0.5$	V		
	Minimum pulse width of sync input	PWmin	300	—	—	ns		
	Input sync pulse duty cycle	PW	5	—	50	%		3
On/off section	ON/OFF sink current 1	$I_{ON/OFF1}$	60	90	120	$\mu\text{A}$	ON/OFF pin: 3 V	
	ON/OFF sink current 2	$I_{ON/OFF2}$	220	290	380	$\mu\text{A}$	ON/OFF pin: 5 V	
	IC on threshold	$V_{ON}$	1.1	1.4	1.7	V		
	IC off threshold	$V_{OFF}$	0.4	0.7	1.0	V		
	ON/OFF threshold difference	$\Delta V_{ON/OFF}$	0.5	0.7	0.9	V		
Total device	Operating current	$I_{IN}$	6.0	8.5	11.0	mA	$C_L = 1000\text{ pF}$	
	Quiescent current	$I_{OFF}$	0	—	10	$\mu\text{A}$	ON/OFF pin: 0 V	1
			—	120	150	$\mu\text{A}$	ON/OFF pin: 0 V	2

- Notes: 1. HA16114 only.  
 2. HA16120 only.  
 3.  $PW = t_1 / t_2 \times 100$

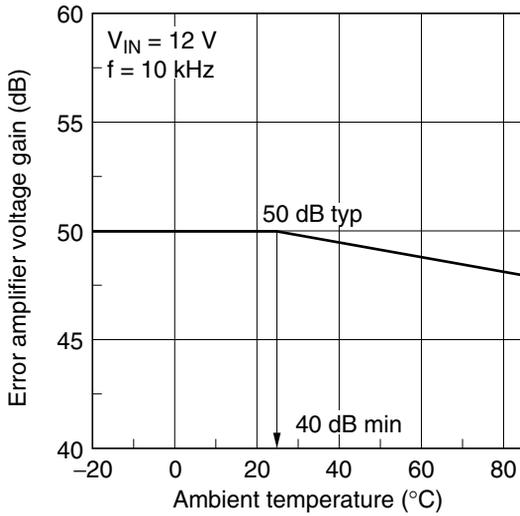


## Characteristic Curves

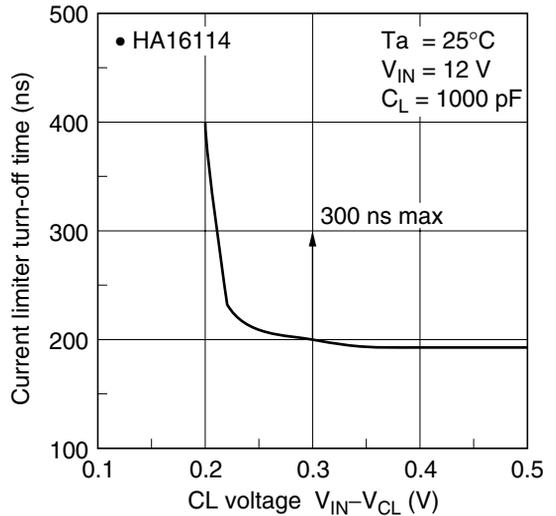




Error Amplifier Voltage Gain vs. Ambient Temperature

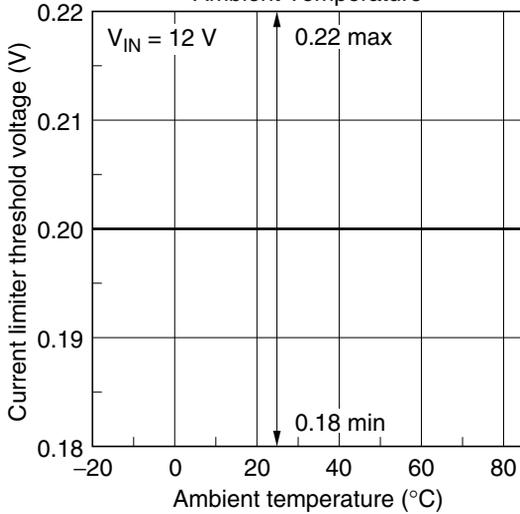


Current Limiter Turn-Off Time vs. Current Limiter Threshold Voltage <sup>Note</sup>

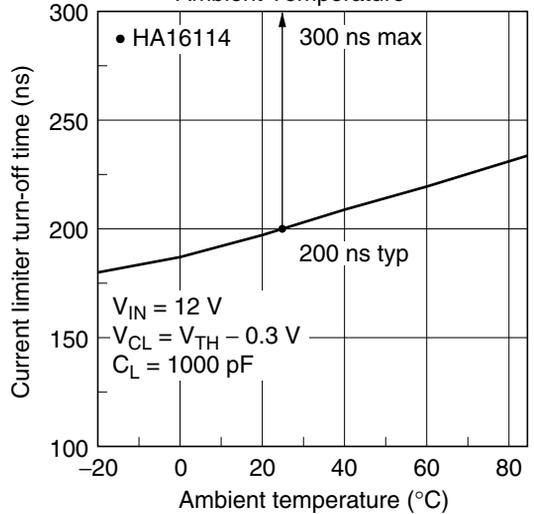


Note: Approximately 300 ns greater than this in the case of the HA16120.

Current Limiter Threshold Voltage vs. Ambient Temperature

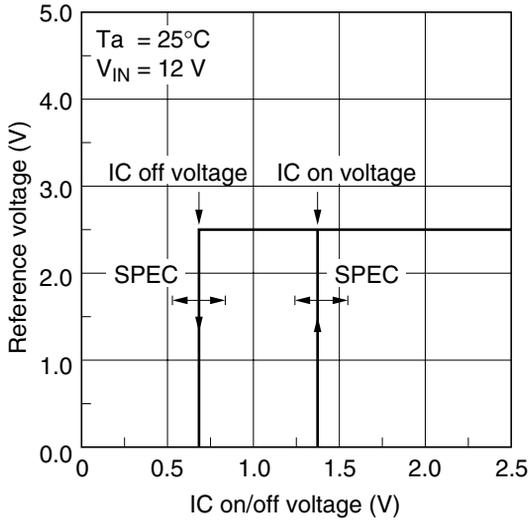


Current Limiter Turn-Off Time vs. Ambient Temperature <sup>Note</sup>

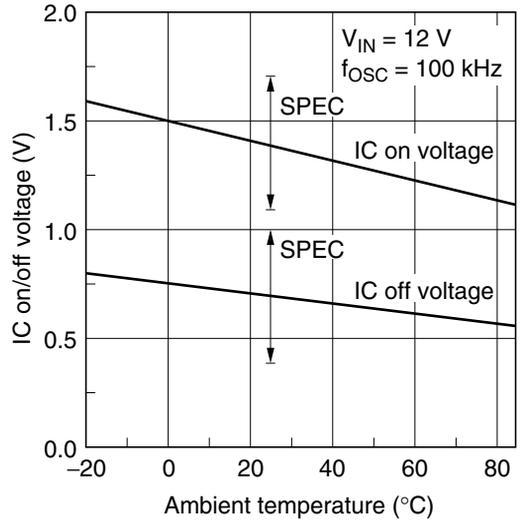


Note: Approximately 300 ns greater than this in the case of the HA16120.

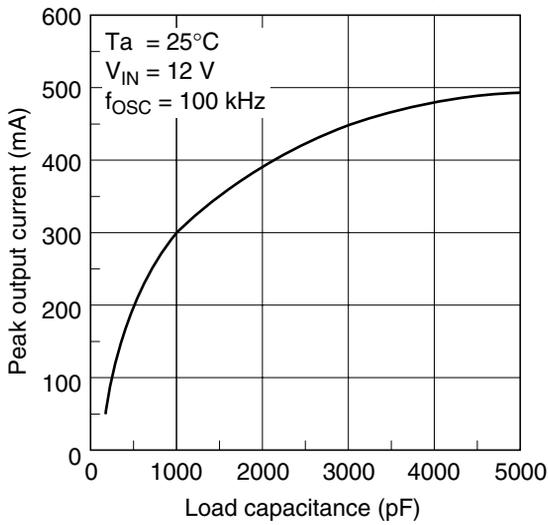
Reference Voltage vs. IC On/Off Voltages



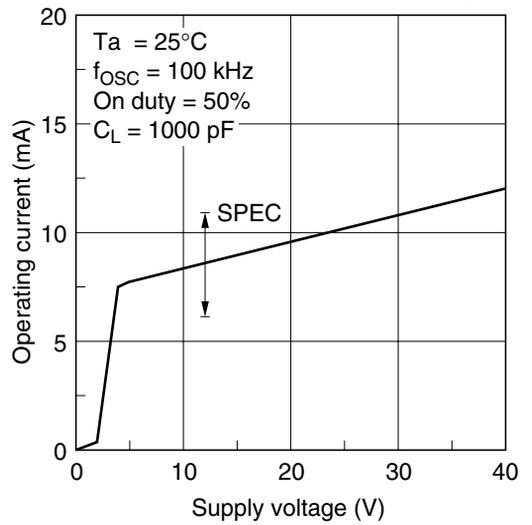
IC On/Off Voltages vs. Ambient Temperature



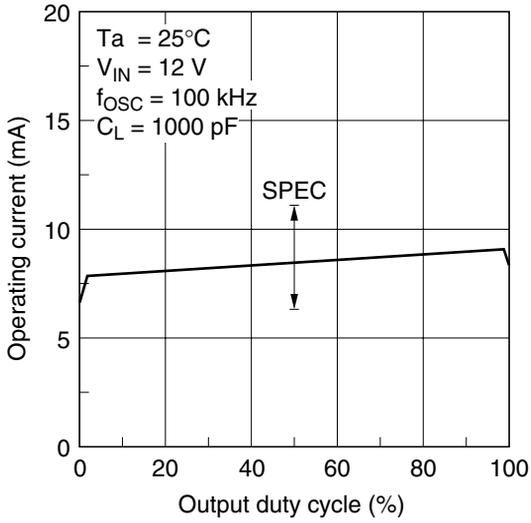
Peak Output Current vs. Load Capacitance



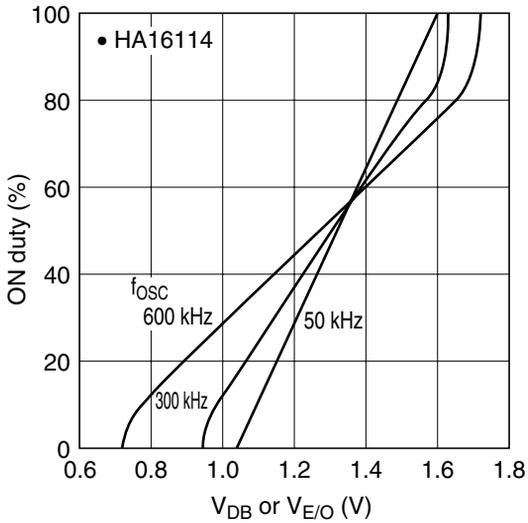
Operating Current vs. Supply Voltage



Operating Current vs. Output Duty Cycle

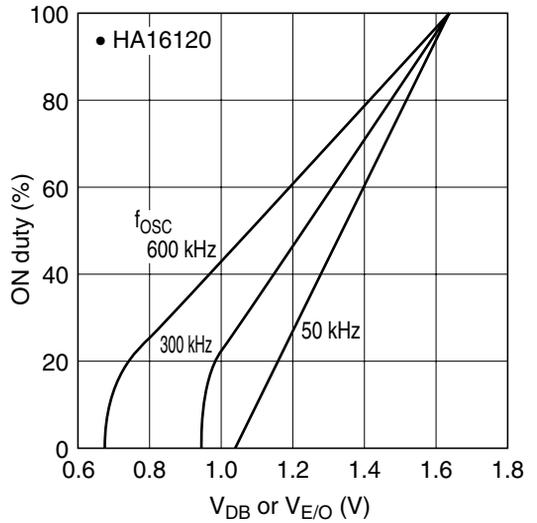


PWM Comparator Input vs. Output Duty Cycle (1)

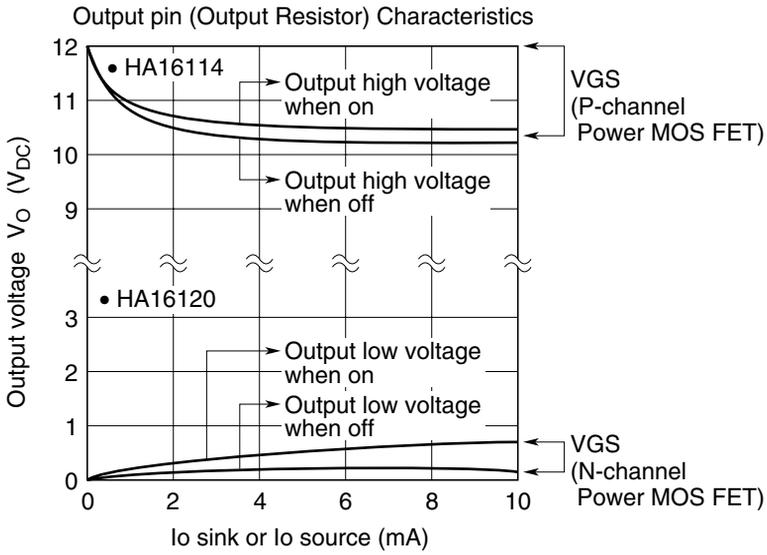


Note: The on-duty of the HA16114 is the proportion of one cycle during which output is low.

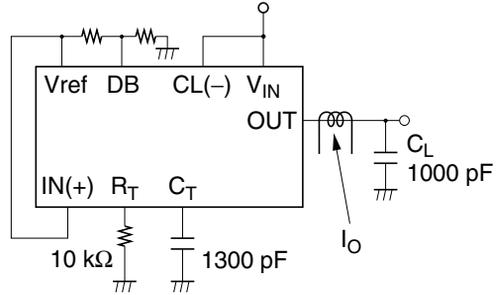
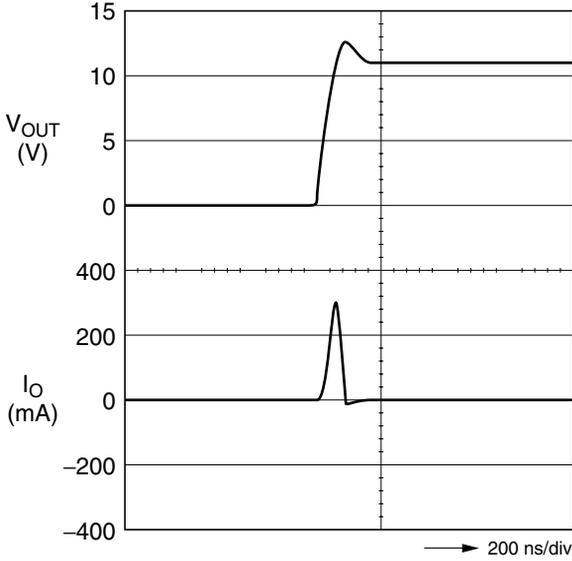
PWM Comparator Input vs. Output Duty Cycle (2)



Note: The on-duty of the HA16120 is the proportion of one cycle during which output is high.

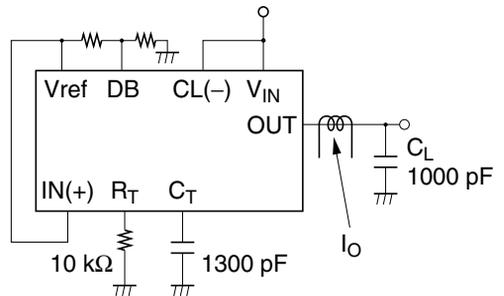
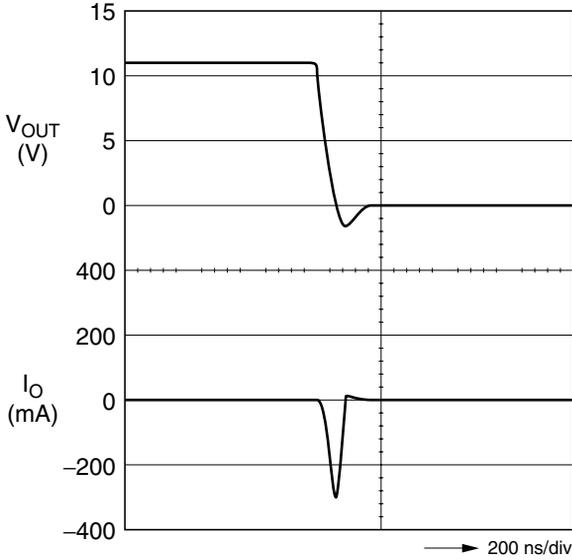


Output Waveforms: Rise of Output Voltage  $V_{OUT}$



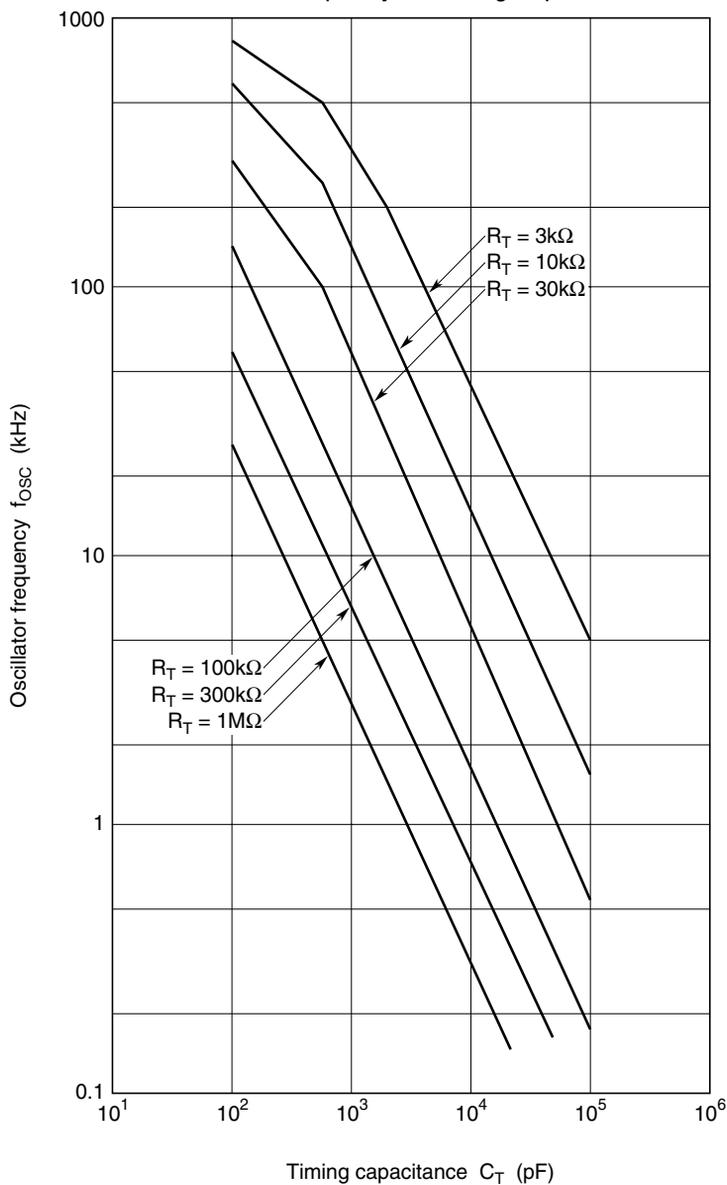
Test Circuit

Output Waveforms: Fall of Output Voltage  $V_{OUT}$



Test Circuit

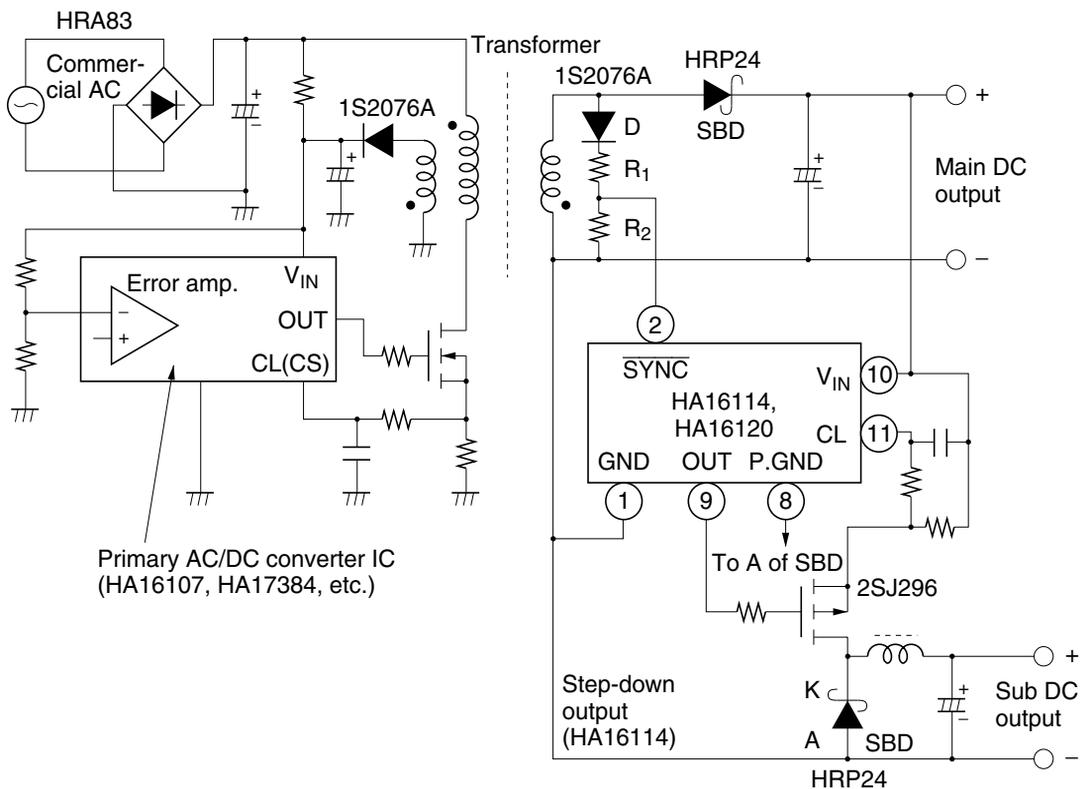
Oscillator Frequency vs. Timing Capacitance





## Application Examples (2)

- External Synchronization with Primary-Control AC/DC Converter
  - Combination with a flyback AC/DC converter (simplified schematic)

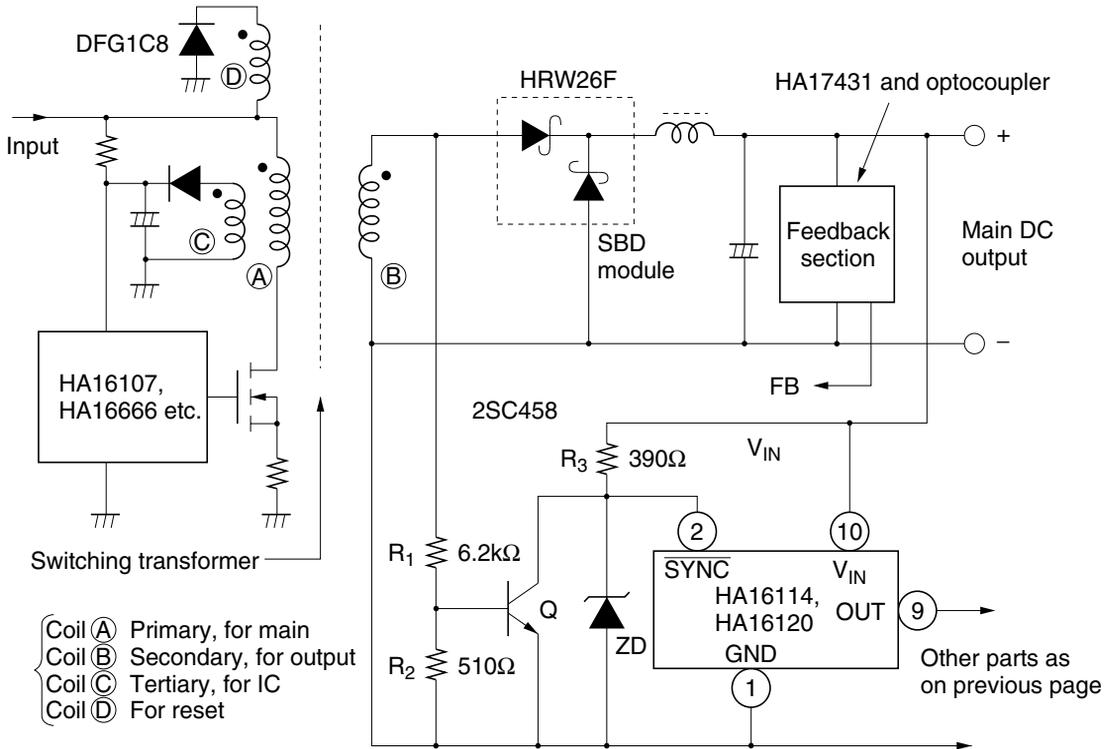


This is one example of a circuit that uses the features of the HA16114/120 by operating in synchronization with a flyback AC/DC converter. Note the following design points concerning the circuit from the secondary side of the transformer to the  $\overline{\text{SYNC}}$  pin of the HA16114/120.

- Diode D prevents reverse current. Always insert a diode here. Use a general-purpose switching diode.
- Resistors  $R_1$  and  $R_2$  form a voltage divider to ensure that the input voltage swing at the  $\overline{\text{SYNC}}$  pin does not exceed  $V_{\text{ref}}$  (2.5 V). To maintain operating speed,  $R_1 + R_2$  should not exceed 10 k $\Omega$ .

## Application Examples (3)

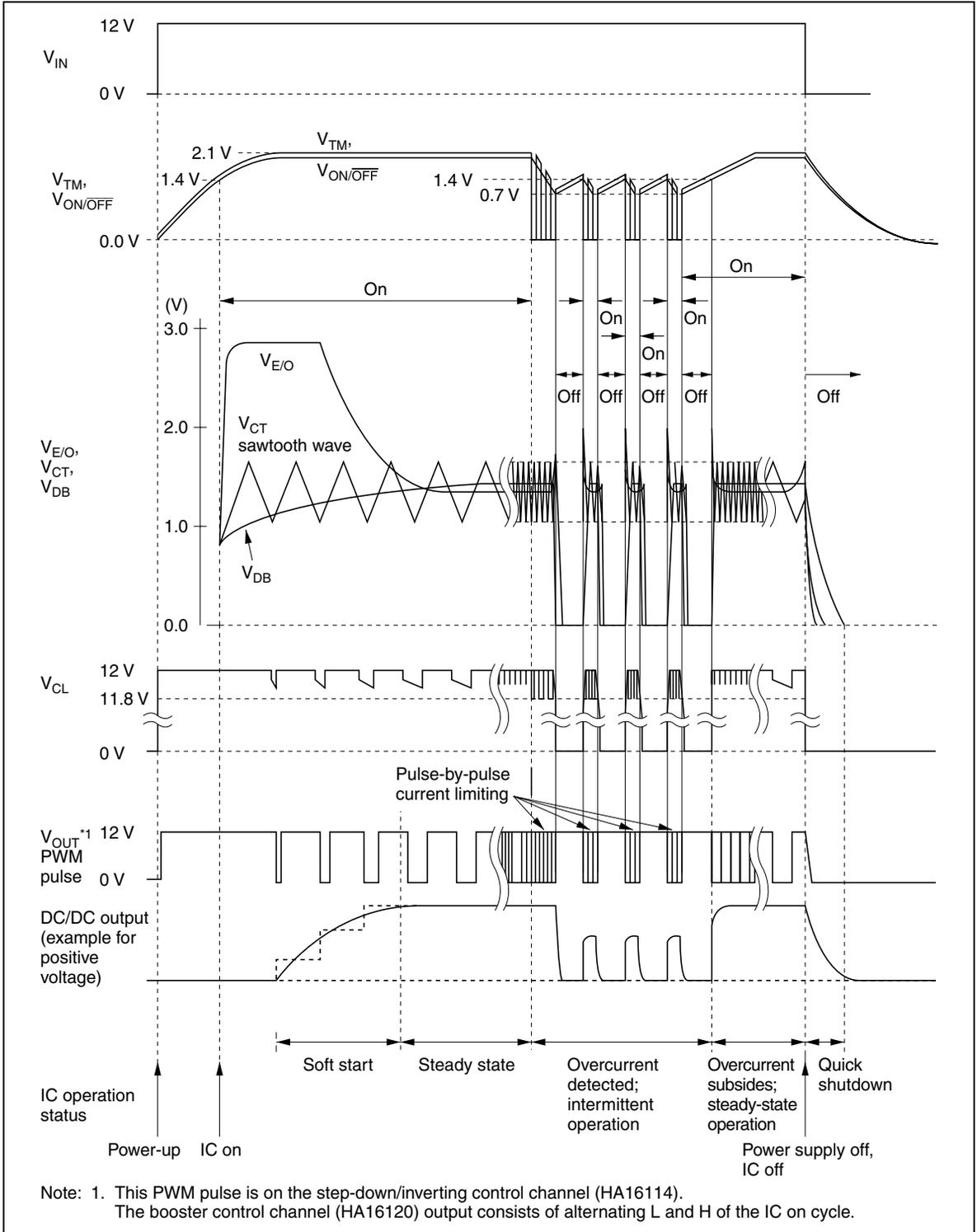
- External Synchronization with Primary-Control AC/DC Converter (cont.)
- (2) Combination with a forward AC/DC converter (simplified schematic)



This circuit illustrates the combination of the HA16114/120 with a forward AC/DC converter. The HA16114/120 synchronizes with the falling edge of the external sync signal, so with a forward transformer, the sync pulses must be inverted. In the diagram, this is done by an external circuit consisting of the following components:

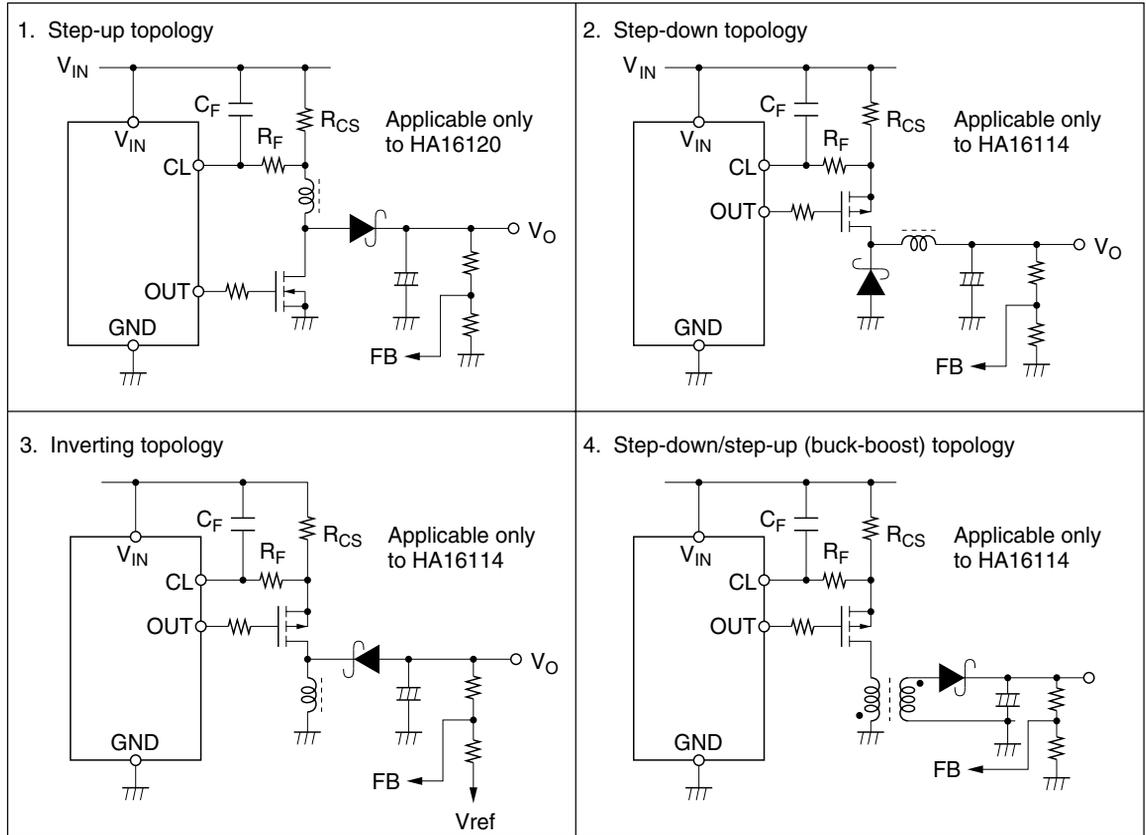
- Q: Transistor for inverting the pulses. Use a small-signal transistor.
- R<sub>1</sub> and R<sub>2</sub>: These resistors form a voltage divider for driving the base of transistor Q. R<sub>2</sub> also provides a path for base discharge, so that the transistor can turn off quickly.
- R<sub>3</sub>: Load resistor for transistor Q.
- ZD: Zener diode for protecting the  $\overline{\text{SYNC}}$  pin.

Overall Waveform Timing Diagram (for Application Example (1))



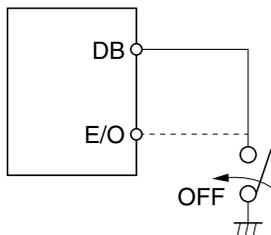
## Application Examples (4) (Some Pointers on Use)

### 1. Inductor, Power MOS FET, and Diode Connections

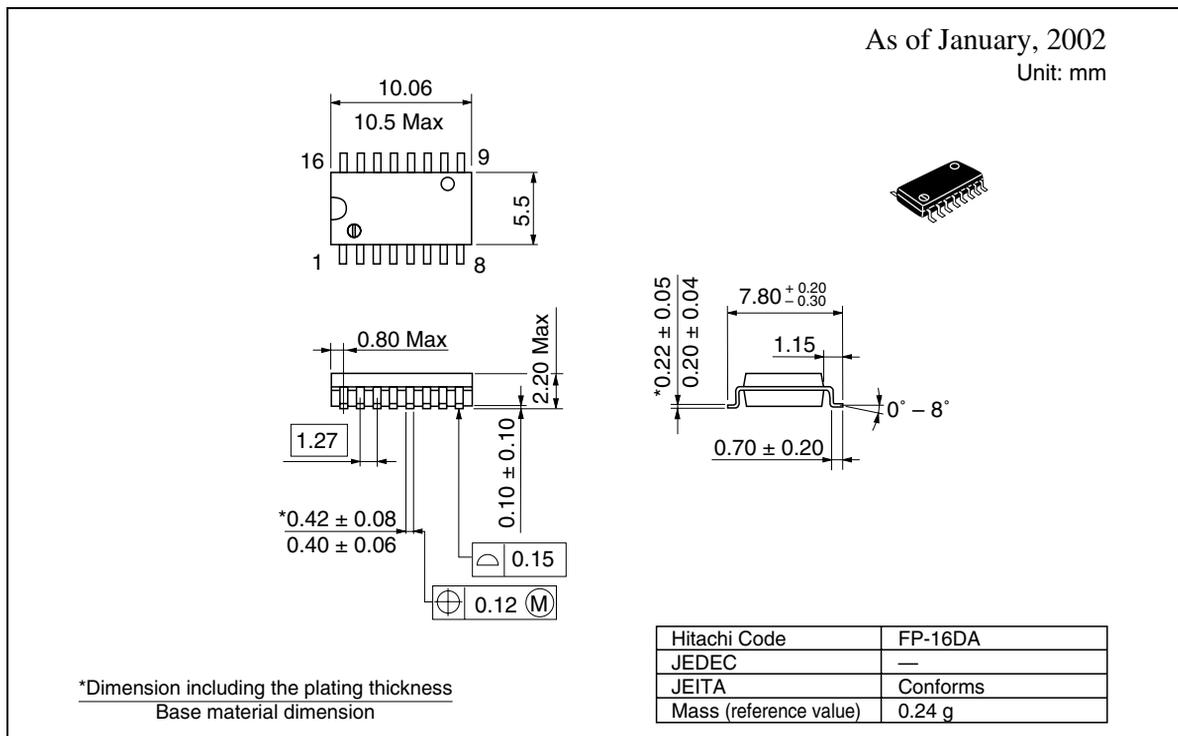
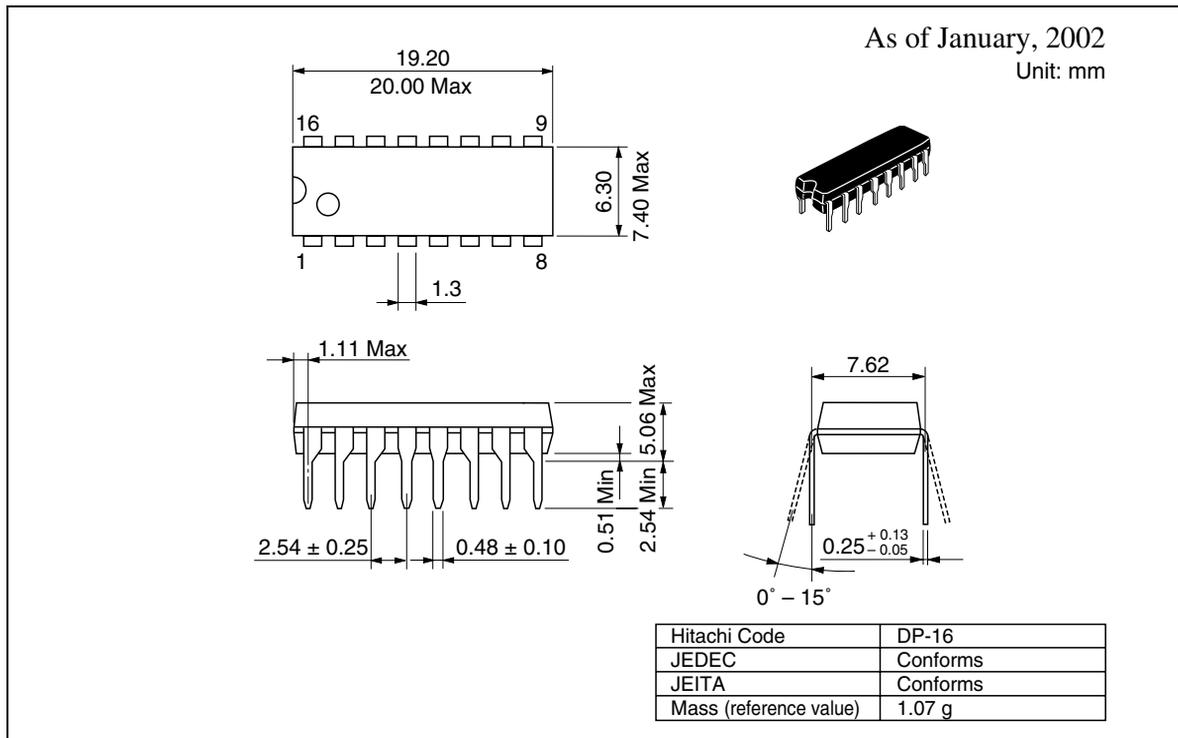


### 2. Turning Output On and Off while the IC is On

To turn only one channel off, ground the DB pin or the E/O pin. In the case of E/O, however, there will be no soft start when the output is turned back on.



## Package Dimensions



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