

DUAL RATE 1773 FIBER OPTIC TRANSCEIVER

HC1773

FEATURES

- Fabricated with RICMOS™ IV Bulk CMOS 0.8 μm Process ($L_{\text{eff}} = 0.65 \mu\text{m}$)
- CMOS Compatible I/O
- Single 5V $\pm 10\%$ Power Supply
- 1Mbps or 20Mbps 1773 format
- Total Dose Hardness of $\geq 3 \times 10^5 \text{ rad}(\text{SiO}_2)$
- No Latchup

GENERAL DESCRIPTION

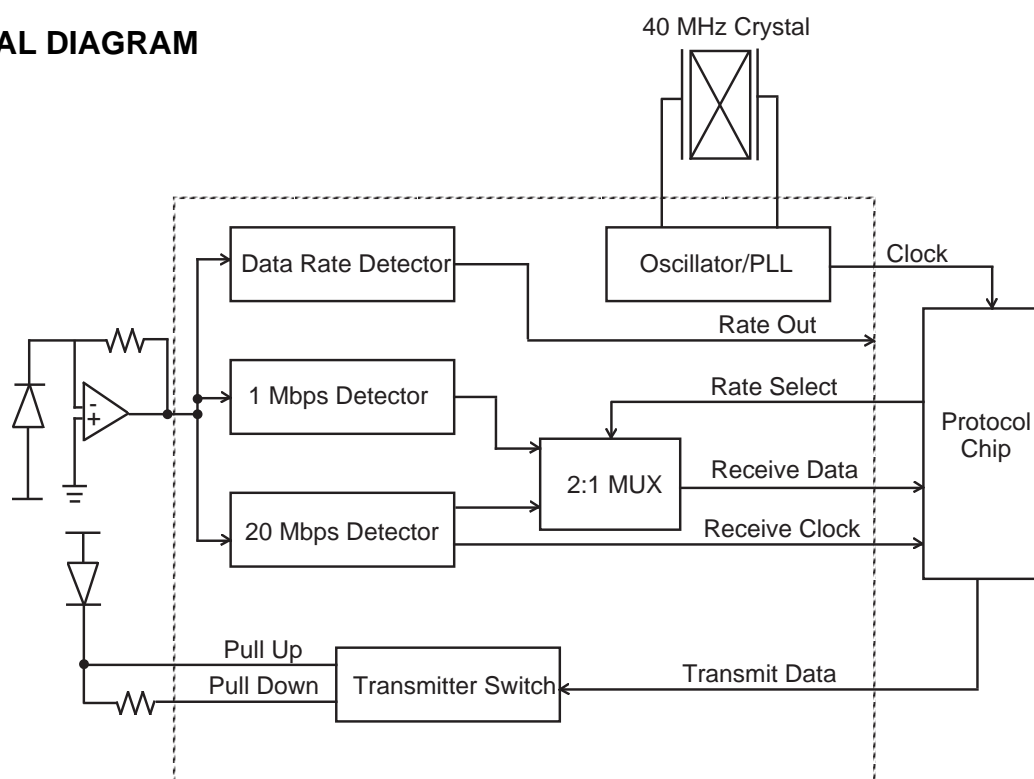
The HC1773 chip is intended to be used in a hybrid package with a photo diode, a transimpedance amplifier, a crystal and an LED or laser diode. Interfacing is intended to be via a protocol chip. Information is transmitted over the fiber optic cable in either 1Mbps or 20Mbps 1773 format. The transceiver chip recovers clock and data from the transimpedance amplifier's output for 20Mbps data, but only recovers the data in the 1Mbps mode. The transceiver chip does not decode the Manchester data, but instead treats the 1Mbps Manchester data as 2Mbps NRZ data, and the 20Mbps Manchester data as 40Mbps NRZ data. An LED or laser diode is also driven with data received from the protocol chip.

The fiber optic transceiver chip consists of five main circuits as shown in the functional diagram.

- Receive post-amplifiers
- 1Mbps decision circuit
- 20Mbps decision circuit
- Data rate detect circuit
- Crystal oscillator and frequency multiplier
- Transmit switch

A detailed functional description of each circuit is available.

FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Conditions
VIL	Low-Level Input voltage	VSS	0.3 x VDD	V	
VIH	High-Level Input Voltage	0.7 x VDD	VDD	V	
VOL	Low-level Output voltage	VSS	0.1 x VDD	V	IOL <500µA
VOH	High-Level Output Voltage	0.9 x VDD	VDD	V	IOH <500µA
VIHR	TTL Input High Voltage	2.0	VDD	V	Reset Pin
VILR	TTL Input Low Voltage	VSS	0.8	V	Reset Pin
IIL	Input Leakage	-1.0	+1.0	µA	
Tr	Output Rise Time		4.0	ns	Cload <50pF
Tf	Output Fall Time		4.0	ns	Cload <50pF
	20 Mbps Post-Amp 3dB BW	50		MHz	Cload <20pF
	1 Mbps Post-Amp 3dB BW	50	5	MHz	
	20 MBps Post-Amp Gain	39	41	dB	Rload <1k
	1 Mbps Post-Amp Gain	39	41	dB	Rload <100k
	20 Mbps Post-Am Input R	900	1100		
	Pulse Width Distortion	-20	20	%	
	P1Inp Input Cap	50		nF	
	1 Mbps Fixed Threshold	0.3	0.4	V	
	PeakDetect Attack		50	ns	PD Cap <150pF
	Transmitter Current	150		mA	Vout 0.5V
	Transmitter Rise Time		2	ns	Cjo<50pF (2)
	RClk Period	20		ns	Cjo<50pF (2)
	RClk Pulse Width Loe	5		ns	
	RClk Pulse Width High	5		ns	
	Power Consumption		200	mW	Transmitter Off
	Power Up Time		0.1	msec	

(1) Worst case operating conditions: VDD=4.5 V to 5.5 V, Die Temp = -55°C, post total dose at 25°C.

(2) Cjo is the zero bias junction capacitance of the LED or laser diode.

ORDERING INFORMATION (1)

H	C	1773	S	R
SOURCE	PROCESS	PART NUMBER	SCREEN LEVEL (2)	TOTAL DOSE HARDNESS
H=HONEYWELL	C=Bulk CMOS		S=Class S Visual B=Class B Visual E=Engr Device (3)	R=1x10 ⁵ rad(SiO ₂) F=3x10 ⁵ rad(SiO ₂) N=No Level Guaranteed

(1) Orders may be faxed to 612-954-2051. Please contact our Customer Logistics Department at 612-954-2888 for further information.

(2) Parts are delivered in die form.

(3) Engineering Device description: Parameters are tested from -55 to 125°C, 24 hr burn-in, no radiation guaranteed. Contact Factory with other needs.

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<http://www.ssec.honeywell.com>

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