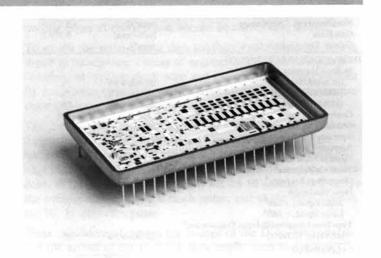


Ultra High-Speed 12-Bit A/D Converter

HAS-1204

FEATURES
12-Bit Resolution
500kHz Word Rates
Internal Track-and-Hold
Single 40-Pin DIP

APPLICATIONS
Medical Instrumentation
Radar Systems
Test Systems
Waveform Analysis
Fast Fourier Transforms



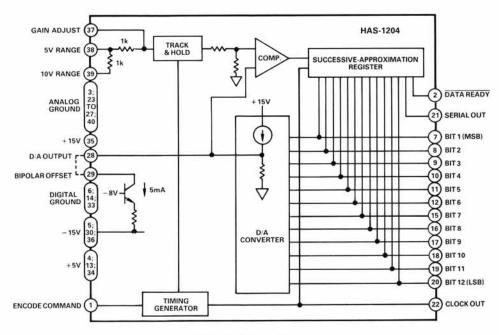
GENERAL DESCRIPTION

The HAS-1204 A/D Converter is a *complete* 12-bit hybrid A/D converter in a single 40-pin metal DIP. In this context, "complete" means the unit includes a track-and-hold (T/H) amplifier, encoder, and all the necessary timing circuits. It is a remarkable, self-contained device ready to perform the conversion function without the need for external circuits.

The maximum conversion time of the HAS-1204 is 2.0 microseconds, including the acquisition time of the internal T/H. The large-signal bandwidth of the T/H is 4MHz and the small-signal

bandwidth is 7MHz. This combination of characteristics assures that the HAS-1204 will operate at word rates from dc through 500kHz, digitizing analog signals containing frequency components to 250kHz with minimum attenuation or distortion.

Integrating the T/H, encoder, and timing circuits into a single package allows optimum matching of T/H-encoder parameters to obtain the best possible performance. It also lowers the overall power dissipation to 2.2 watts, making the HAS-1204 an ideal choice for designers who face space and/or power restrictions for their designs.



HAS-1204 Block Diagram

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

P.O. Box 280; Tel:617/329-4700

Telex: 924491

Norwood, Mas

Massachusetts 02062 U.S.A. Twx: 710/394-6577

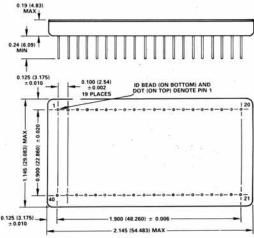
Cables: ANALOG NORWOODMASS

$\begin{center} \textbf{SPECIFICATIONS} & \textbf{(typical @ +25°C with nominal power supplies unless otherwise noted)} \\ \end{center}$

Model	Units	HAS-1204BM	HAS-1204SM
RESOLUTION (FS = Full Scale)	Bits (%FS)	12 (0.024)	*
LSB WEIGHT			
5V Input Range	mV	1.22	*
10V Input Range	mV	2.44	*
ACCURACY			
Linearity @ dc	$%FS \pm 1/2LSB$	0.0125	*
Monotonicity		Guaranteed	
Nonlinearity vs. Temperature	ppm/°C	3	
Gain Error Gain vs. Temperature	%FS (max) ppm/°C	0.1 (0.7) 35	*
DYNAMIC CHARACTERISTICS	ppin 0		
In-Band Harmonics ¹			
(dc to 60kHz)	dB below FS	75	*
(60kHz to 120kHz)	dB below FS	75	*
(120kHz to 200kHz)	dB below FS	70	*
Conversion Rate	kHz	500	*
Conversion Time	μs, max	2.0	*
Aperture Uncertainty (Jitter)	ps	60	1
Aperture Time (Delay)	ns (min/max)	10 (4/18)	-
Signal to Noise Ratio (SNR) ²	dB	69 400	
Transient Response ³ Overvoltage Recovery ⁴	ns ns	900	*
Input Bandwidth	115	700	
Small Signal, – 3dB ⁵	MHz	7	*
Large Signal, -3dB ⁶	MHz	4	*
Two-Tone Linearity (@ Input Frequencies)7			
(37.5kHz; 52.5kHz)	dB below FS	85	*
ANALOG INPUT			
Voltage Ranges	V,FS	0 to -5; 0 to -10	*
		$\pm 5; \pm 2.5$	
Overvoltage	V, max	2×FS	*
Impedance			
5V Ranges	Ω(max)	$1,000 (\pm 10)$	•
10V Ranges	Ω(max)	$2,000(\pm 20)$	· 5
Offset ⁸	V ()	10/60)	
Initial-10V Input vs. Temperature (Unipolar)	mV (max) FS ppm/°C	10 (60) 15	*
vs. Temperature (Empolar)	FS ppm/°C	50	* 3
ENCODE COMMAND INPUT ⁹	roppin o		
Logic Levels, TTL-Compatible	v	"0" = $0 \text{ to } + 0.4$	*
2001		"1" = $+2.4$ to $+5$	* 52
Impedance	LS TTL Loads	2	
Rise and Fall Times	ns, max	10	*
Width			
Min	ns	90	*
Max	ns	160	*
Frequency	kHz	dc to 500	
DIGITAL OUTPUT10			
Format	Data Bits	12 Parallel; NRZ	*
1 Otmat	D. D.	1 07	2
	Data Ready	1; RZ	*
Logic Levels, TTL-Compatible	Data Ready V	"0" = $0 \text{ to } + 0.4$	*
Logic Levels, TTL-Compatible	v	"0" = 0 to +0.4 "1" = +2.4 to +5	*
Logic Levels, TTL-Compatible Drive		"0" = $0 \text{ to } + 0.4$:
Logic Levels, TTL-Compatible Drive Coding	v	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard	* * *
Logic Levels, TTL-Compatible Drive	v	"0" = 0 to +0.4 "1" = +2.4 to +5 1 Standard Complementary	*
Logic Levels, TTL-Compatible Drive Coding	v	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary	*
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode	v	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN)	* * * * * * * * * * * * * * * * * * * *
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode	v	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary	* * * * * * * * * * * * * * * * * * * *
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode Bipolar Mode	v	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary	* * * * * * * * * * * * * * * * * * * *
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode Bipolar Mode	v	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary	*
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode Bipolar Mode	V TTL Loads	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary (COB)	* * * * * * * * * * * * * * * * * * * *
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode Bipolar Mode POWER REQUIREMENTS +15V ± 0.5V -15V ± 0.5V +5V ± 0.5V	V TTL Loads mA (max)	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary (COB)	* * * * * * * * * * * * * * * * * * * *
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode Bipolar Mode POWER REQUIREMENTS +15V ± 0.5V -15V ± 0.5V	V TTL Loads mA (max) mA (max)	"0" = 0 to + 0.4 "1" = +2.4 to +5 1 Standard Complementary Binary (CBN) Complementary Offset Binary (COB) 54(76) 40(55)	* * * * * * * * * * * * * * * * * * * *
Drive Coding Unipolar Mode Bipolar Mode POWER REQUIREMENTS +15V ± 0.5V -15V ± 0.5V Power Dissipation ¹¹	V TTL Loads mA (max) mA (max) mA (max)	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary (COB) 54(76) 40(55) 160(177)	* * * * * * * * * * * * * * * * * * * *
Drive Coding Unipolar Mode Bipolar Mode POWER REQUIREMENTS +15V ± 0.5V -15V ± 0.5V Power Dissipation ¹¹	V TTL Loads mA (max) mA (max) mA (max)	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary (COB) 54(76) 40(55) 160(177)	* * * * * * * * -55 to +100
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode Bipolar Mode POWER REQUIREMENTS +15V ± 0.5V -15V ± 0.5V +5V ± 0.5V Power Dissipation ¹¹ TEMPERATURE RANGE ¹²	MA (max) mA (max) mA (max) W (max)	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary (COB) 54 (76) 40 (55) 160 (177) 2.2 (2.85)	* * * * * * * -55 to +100
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode Bipolar Mode POWER REQUIREMENTS +15V ± 0.5V -15V ± 0.5V +5V ± 0.5V Power Dissipation ¹¹ TEMPERATURE RANGE ¹² Operating Storage	TTL Loads mA (max) mA (max) mA (max) V (max)	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary (COB) 54 (76) 40 (55) 160 (177) 2.2 (2.85) - 25 to + 85	* * * * * * * * * * * * *
Drive Coding Unipolar Mode Bipolar Mode POWER REQUIREMENTS +15V ± 0.5V -15V ± 0.5V +5V ± 0.5V Power Dissipation ¹¹ TEMPERATURE RANGE ¹² Operating Storage THERMAL RESISTANCE ¹³	TTL Loads mA (max) mA (max) mA (max) V (max)	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary (COB) 54 (76) 40 (55) 160 (177) 2.2 (2.85) - 25 to + 85	* * * * * * * * * * * * * * * * * * *
Logic Levels, TTL-Compatible Drive Coding Unipolar Mode Bipolar Mode POWER REQUIREMENTS +15V ± 0.5V -15V ± 0.5V +5V ± 0.5V Power Dissipation ¹¹ TEMPERATURE RANGE ¹² Operating	TTL Loads mA (max) mA (max) mA (max) V (max)	"0" = 0 to + 0.4 "1" = + 2.4 to + 5 1 Standard Complementary Binary (CBN) Complementary Offset Binary (COB) 54 (76) 40 (55) 160 (177) 2.2 (2.85) - 25 to + 85	* * * * * * * * * * * * * * * * * * *

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



HAS-1204 PIN DESIGNATIONS

(As viewed from bottom)

PIN	FUNCTION	PIN	FUNCTION	
40	ANALOG GROUND	1	ENCODE COMMAND	
39	10V RANGE	2	DATA READY	
38	5V RANGE	2 3	ANALOG GROUND	
37	GAIN ADJUST	4	+5V	
36	-15V	5	-15V	
35	+ 15V	6	DIGITAL GROUND	
34	+5V	7	BIT 1 (MSB)	
33	DIGITAL GROUND	8	BIT 2	
32	FACTORY USE ONLY	9	BIT 3	
31	FACTORY USE ONLY	10	BIT 4	
30	-15V	11	BIT 5	
29	BIPOLAR OFFSET	12	BIT 6	
28	D/A OUTPUT	13	+5V	
27	ANALOG GROUND	14	DIGITAL GROUND	
26	ANALOG GROUND	15	BIT 7	
25	ANALOG GROUND	16	BIT 8	
24	ANALOG GROUND	17	BIT9	
23	ANALOG GROUND	18	BIT 10	
22	CLOCKOUT	19	BIT 11	
21	SERIALOUT	20	BIT 12 (LSB)	

NOTES

*Specification same as HAS-1204BM

¹In-band harmonics expressed in terms of spurious in-band signals generated at 500kHz encode rate at analog input frequencies

shown in ().

²RMS signal to rms noise ratio with 50kHz analog input and encode rate of

500kHz; input signal at -1.0dB.

³For full-scale step input, 12-bit accuracy attained in specified time.

Recovers to specified performance in specified time after 2×FS input voltage.

input voltage.

⁵With analog input 40dB below FS.

⁶With FS analog input. (Large-signal bandwidth flat within 0.5dB, dc to 1MHz).

⁷Each input frequency applied at a level 7dB below full scale.

⁸Externally adjustable to zero.

⁹Transition from digital "0" to digital "1" initiates encoding.

¹⁰Use trailing edge of Data Ready pulse to strobe digital outputs into external circuits (See Figure 2).

¹¹Power dissipation shown is at zero input.

¹²T = Case temperature.

¹³Maximum junction temperature = 150°C. Operating unit requires

¹³Maximum junction temperature = 150°C. Operating unit requires 500 cubic feet per minute (CFPM) moving air.

Specifications subject to change without notice.

THEORY OF OPERATION/TIMING

Refer to the block diagram of the HAS-1204.

Analog input signals to be digitized are applied to either Pin 38 (5V RANGE) or Pin 39 (10V RANGE), depending upon their amplitude. These signals are inputs to the internal track-and-hold (T/H) which is normally operating in the "track" mode as a buffer amplifier, following all changes in analog as they occur.

An external strap, shown between Pin 28 and Pin 29, is used if operating the converter in the bipolar mode; it is important to keep this strap as short as possible. For unipolar operation, connect Pin 29 to ground.

The user determines the point at which the digitizing process is to be initiated by controlling the application of the TTL-compatible Encode Command pulse. Its positive-going leading edge switches the T/H to the "hold" mode of operation, "freezing" the analog input signal and beginning the digitizing process. As shown in the block diagram, the Encode Command applied to Pin 1 generates the required timing signals within the HAS-1204 A/D, making it unnecessary to add external circuits.

The held value of analog input is part of the input to a high-speed comparator within the converter. The other input is the analog output of the internal high-speed, high-accuracy D/A converter. The resulting output of the comparator is applied to the successive approximation register (SAR), also controlled by timing signals initiated by the encode command.

Digital outputs are available in both serial and parallel formats, as shown in Figure 1, HAS-1204 Timing.

Times shown in the timing diagram are typical times, unless noted otherwise. In the illustration, the Track/Hold signal is internal, not available to the user; it is included to help understand the operation of the converter.

Timing intervals are measured from the leading edge of the Encode Command supplied by the user; this makes it easier to establish appropriate system timing.

Note the trailing edge of each clock pulse occurs after its corresponding serial output information has changed. If the serial output of the HAS-1204 converter is the desired signal, the trailing edges of clock pulses should be used as the stobes.

To assure the serial output data are fully established, the user is urged to incorporate a delay of approximately 30 nanoseconds between the trailing clock edge and the latch. This compensates for latch setup time, and slight variations in timing between the clock pulses and their associated data.

The portion of Figure 1 pertaining to Data Ready timing shows it returns to the digital "0" state 10 nanoseconds before the track-and-hold switches from "hold" to "track". The trailing edge of clock pulse #12 and the "track" transition are time-coincident, so this change in Data Ready occurs 10 nanoseconds before the trailing edge of the last clock pulse; and at the same time as the Bit 12 data change.

Time coincidence between the change of the \overline{Data} Ready pulse and the arrival of Bit 12 (LSB) data might seem to preclude using the \overline{Data} Ready pulse as a strobe. Despite that initial impression, the trailing (falling) edge of the \overline{Data} Ready is recommended for strobing the parallel outputs into external circuits. This can be accomplished by using an inverter with a time delay (t_D) of the appropriate amount for the latch which is being used, as illustrated in Figure 2.

The timing relationships discussed above are generated internally because the clock pulses' rising edges control the switching. The 30-nanosecond width of each clock signal helps assure that its serial output data are firmly established by the time the clock's trailing edge arrives.

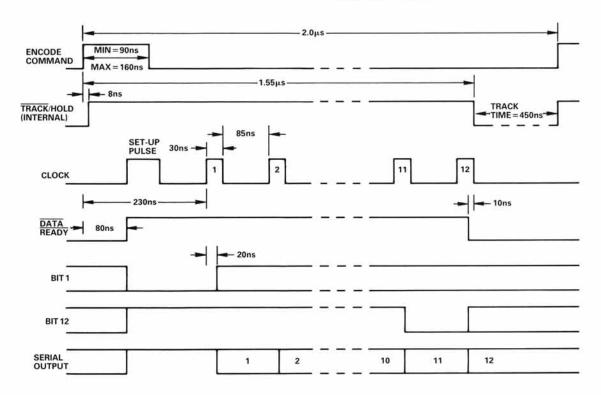


Figure 1. HAS-1204 Timing

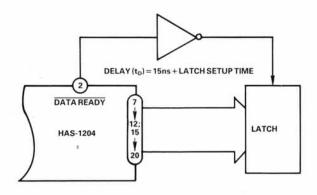


Figure 2. Output Strobe

APPLICATIONS INFORMATION

Figures 3 and 4 provide needed details on the adjustment of controls for setting the amount of offset and gain.

As noted in both illustrations, the OFFSET control must be set first for proper performance of the converter. Since the HAS-1204 is capable of operating in either a unipolar or bipolar mode, OFFSET ADJUST and GAIN ADJUST include information for both.

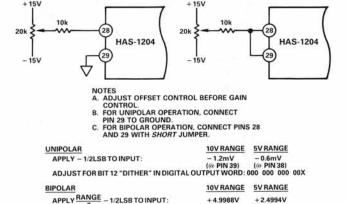


Figure 3. Offset Adjust

ADJUST FOR BIT 12 "DITHER" IN DIGITAL OUTPUT WORD: 000 000 00X

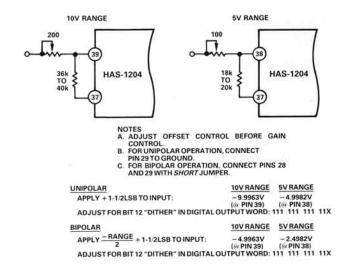


Figure 4. Gain Adust

However, careful adjustment of available controls is not the only way to help assure optimum performance. Like all high-speed, high-resolution components, the HAS-1204 is also sensitive to layout constraints. The use of a large, low-impedance ground plane is imperative.

In addition, bypass capacitors on the power supply leads are recommended. For most applications, electrolytic capacitors of 10-22 microfarads in parallel with ceramic capacitors of $0.01\mu F$ to $0.1\mu F$ will enhance the converter's effectiveness. These should be connected as closely as possible to the power supply pins entering the hybrid.

To prevent cross-coupling of analog and digital signals which may "mask" lower-order bits, analog and digital signal paths should be physically separated as much as possible. The user is urged to pay careful attention to both electrical and mechanical design to obtain best results.

ORDERING INFORMATION

Two versions of HAS-1204 A/D Converters are available as standard products; both are housed in 40-pin hermetically-sealed metal packages. With the exception of operating temperatures, the specifications are the same for both units. For a temperature range of -25° C to $+85^{\circ}$ C, specify the model HAS-1204BM; for a range of -55° C to $+100^{\circ}$ C, order model number HAS-1204SM. Units screened to military requirements are also available; contact the factory for details.