64-Channel Serial To Parallel Converter With Temperature Sense and High Voltage Push-Pull Outputs

Ordering Information

Device	Package Option	
	Micro-BGA	Die
HV512	HV512GA	HV512X

Features

- ❑ High voltage HVCMOS® output
- ❑ Output voltages from 0V to 50V-200V
- ❑ Low power level shifting
- ❑ Shift register speed 12.5MHz double clocked for 25MHz data rate
- ❑ Logic control includes Direction, Blank, Polarity, Latch and High-Z
- ❑ CMOS compatible inputs
- ❑ Internal pull-up or pull-down on logic inputs
- ❑ Continuously monitored temperature sense
- ❑ Quad 16-bit output latch control

General Description

The HV512 is a low voltage serial to high voltage parallel converter with push-pull outputs. The device allows switching of the outputs between V_{PP} and HVGND.

Data is loaded into the 64-bit shift register using the data input signal, D_{IOA} or D_{IOB}, and clock, CLK. Control of the data direction is by the use of the DIR pin. Data is shifted out through the data output signals, D_{IOB} or D_{IOA}. The data is controlled through the device using the latch enable, $\overline{LE}$, and blank, BLE_X, control signals. The output drivers are further controlled by a polarity, $\overline{POL}$, and high-Z, $\overline{HI\text{-}Z}$, control lines.

Die temperature sensing is provided to inform the user when the die temperature reaches the limit of the operating temperature.

Absolute Maximum Ratings

Logic supply voltage, V_{DD}		7.5V
Driver supply voltage, V_{PP}		220V
Output voltage		220V
Input voltage[1]		-2.0V to V_{DD}+2.0V
Thermal Resistance	Junction to Case, R_{JC}	1 °C/W
Operating Temperature Range		-0°C to +150°C

All voltages are referenced to GND.

[1] Minimum of -2.0V for 20 nsec. Maximum of V_{DD} +2.0V for 20 nsec. allowable.

Electrical Characteristics

DC Characteristics (Over recommended Operating Conditions unless otherwise noted)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
V_{OH}	High-level output voltage	HV outputs	V_{PP}-2.0			V	I_{OH}=-1mA
V_{DOH}		Serial output	V_{DD}-0.75			V	V_{DD}=4.5V, I_{OH}=-100 μA
V_{OL}	Low-level output voltage	HV outputs			2.0	V	I_{OL}=1mA
V_{DOL}		Serial output			0.75	V	V_{DD}=4.5V, I_{OL}=100 μA
V_{IH}	High level input voltage		0.8 V_{DD}		V_{DD} + 0.5	V	Standard CMOS levels, with respect to ground
V_{IL}	Low level input voltage		-0.5		0.2 V_{DD}	V	
I_{AVDD}	AV_{DD} current				0.2	mA	
I_{DD}	V_{DD} current				25	mA	inputs high, f_{CLK} = 12.5MHz [1]
I_{DDQ}	V_{DD} quiescent current				1	mA	all inputs = floating; D_{IOA}, D_{IOB} , CLK = LOW
I_{PP}	V_{PP} current	C_L=10pF			30	mA	f_{OUT} = 300Kcycles, V_{PP} = 220V
		C_L=30pF			25		f_{OUT} = 100Kcycles, V_{PP} = 220V
I_{PPQ}	V_{PP} quiescent current				0.5	ma	Outputs H or L.
$I_{O(OFF)}$	High-Z state output current				TBD	μA	
I_H	High-level input current [2]				10	μA	For inputs with 20k pull-up resistor
					275		For inputs with 20k pull-down resistor
I_L	Low-level Input current [2]				10	μA	For inputs with 20k pull-down resistor
					275		For inputs with 20k pull-up resistor
T_{TRIP}	Over temperature trip level		110	115	120	°C	
T_{HYS}	Temperature hysteresis				25	°C	Required cooling to reset /OT output

Internal Capacitance

Symbol	Parameter	Max	Unit	Condition
C_{IN}	Input Capacitance	10	pF	f = 1 MHZ
C_{HVout}	HV Output Capacitance	5	pF	f = f_O max
C_{OUTL}	Output Logic Capacitance	10	pF	f = 1 MHZ

Electrical Characteristics, continued:

AC Characteristics (Over recommended Operating Conditions unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock frequency			12.5	MHZ	to 140°C T_J
f_{DATA}	Data rate			25	MHZ	to 140°C T_J
t_{WL}, t_{WH}	Clock width low / high	30			nsec	
t_{SU}	Data setup to before clock rise/fall	15			nsec	
t_H	Data hold after clock rise/fall	15			nsec	
t_{LL}, t_{LH}	Delay clock to logic output rise/fall		200	250	nsec	Not compatible for cascading at 12.5MHz
t_{DLE}	Clock rise/fall to latch enable fall	25			nsec	Min. time to allow S/R to settle before $\overline{LE}$
t_{WLE}	Latch enable width	40			nsec	Min. $\overline{LE}$ pulse width to latch data
t_{SLE}	Latch enable fall to clock rise/fall	80			nsec	Delay before restarting clock
t_{LBH}	Setup time from $\overline{LE}$ to BLE_X	60			nsec	
t_R	Input rise time	0		10	nsec	All input signals
t_F	Input fall time	0		10	nsec	All input signals
t_{ON}, t_{OFF}	BLE_X or $\overline{POL}$ to HV output rise/fall			500	nsec	10pF external load, to start (10%) of output rise or start (90%) of output fall
Δt_{ON}, Δt_{OFF}	Variation on single IC			100		
t_{OT}	Over temp sense			250	nsec	From over temp sense to output state [3]
f_D	HV output switching rate	0		300	kHz	10pF external load
		0		100		30pF external load
t_{DR90}	HV output 90% rise time			550	nsec	10pF external load [4]
				900		30pF external load [4]
t_{DR95}	HV output 95% rise time			600	nsec	10pF external load [4]
				1000		30pF external load [4]
t_{DF10}	HV output 10% fall time			550	nsec	10pF external load [4]
				900		30pF external load [4]
t_{DF5}	HV output 5%Fall Time			600	nsec	10pF external load [4]
				1000		30pF external load [4]
t_{HI-Z}	HV output to high-Z State			500	nsec	Input to high-Z state on outputs

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{PP}	High voltage supply	50		200	V	
V_{DD}	Logic supply voltage	4.75	5.0	5.25	V	
AV_{DD}	Over-temp circuit supply	4.75	5.0	5.25	V	
f_{SC}	Shift clock frequency			12.5	MHZ	
T_J	Junction temperature	10		140	°C	

Electrical Characteristics, continued:

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Conditions
V_{DD}	Logic Supply Voltage	-0.5	7.5	V	with respect to ground [5]
AV_{DD}	Analog Supply Voltage	-0.5	7.5	V	with respect to ground [5]
V_{PP}	High Supply Voltage	-0.5	220	V	with respect to ground [5]
V_{IN}	Logic Inputs	-2.0	V_{DD}+2.0 [6]	V	with respect to ground [5]
T_{STG}	Storage Temperature	-65	150	°C	No bias
T_J	Junction Temperature	0	150	°C	Max DC voltages applied, all inputs GND [7]
T_{SHORT}	Output Short Duration	2		μsec	Any high output to any output at any levels, or any output to ground, V_{PP}; with V_{PP} at max voltage; no IC damage (need characterization)

Notes:

1 Outputs switching V_{PP} = 200V to GND, 300,000 times per second, 10pf external load on each output. Or, outputs switching V_{PP} = 200V to GND 100,000 times per second, 30pF external load on each output.

2 Inputs include nominal 20k ±25% value bias resistor to V_{DD} or GND to prevent damage from a floating input.

3 Need to respond, typically setting Hi-Z to LOW, to over-temperature (/OT) signal within 1ms to prevent die damage.

4 Rise and fall times are currently based on simulation of S-4 process. This is a new process and distribution of variance is not completely modeled. Thus, these numbers are goals and not a guarantee of production performance. (DELETE THIS NOTE ON FINAL SPEC)

5 All grounds must be at the same potential.

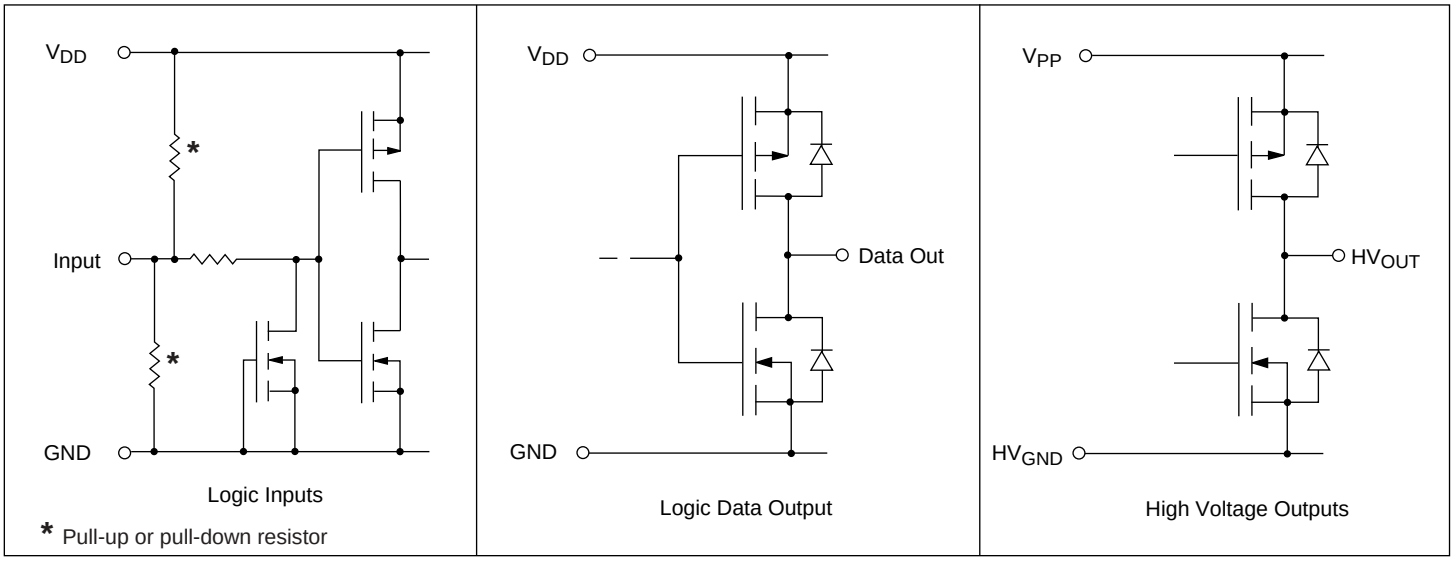
6 Minimum of -2.0V for 20 nsec. Maximum of V_{DD} +2.0V for 20 nsec. allowable.

7 Power dissipation assumes a package with a thermal resistance = 7.5 °C / Watt in 50 °C ambient. Duty cycle is limited by total power dissipation of the carrier.

Power sequence should be the following:

1. Connect ground.
2. Apply V_{DD}, AV_{DD}, and V_{PP} bias (≥V_{DD}-1V).
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply full V_{PP}. Power down sequence should be the reverse of the above.

Input and Output Equivalent Circuit



Pad/Ball Definitions

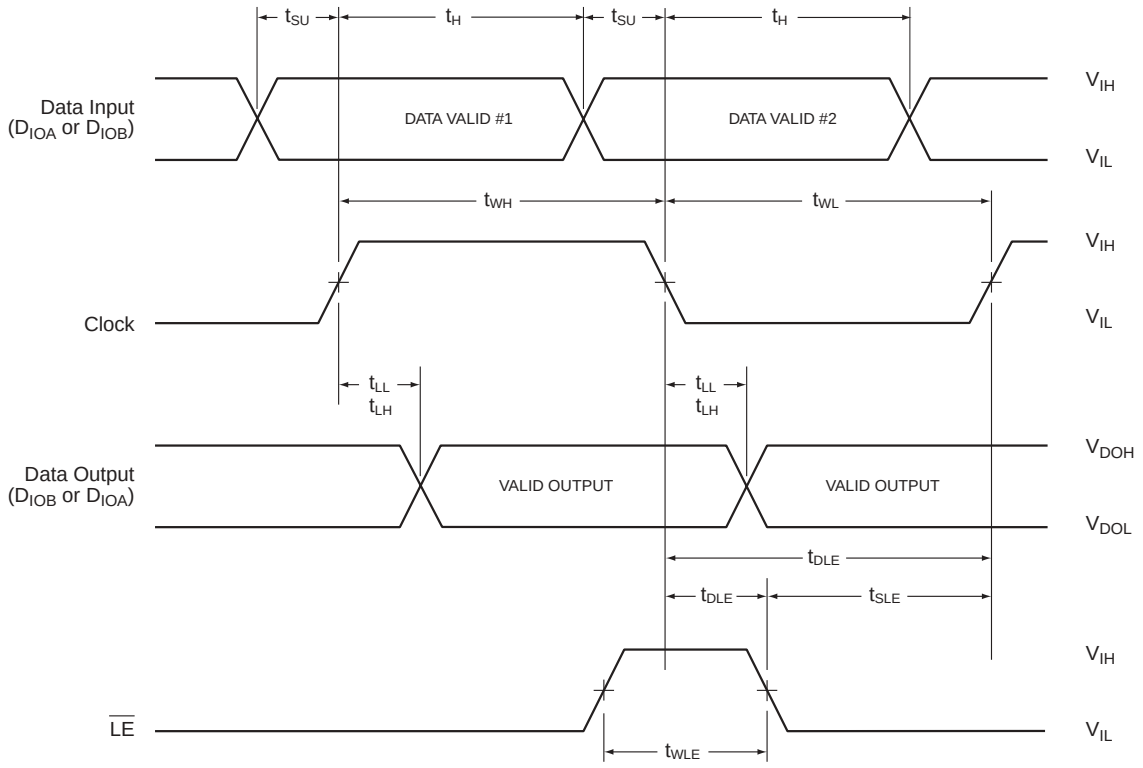
Pad	Ball #	Name	I/O	Function
13	A6	AGND	-	Analog ground for over-temp circuit
12	A7	AV_{DD}	-	Over-temp circuit supply voltage
5	B1	BLE_A	I	Transfers data from 64-bit latches to output latches when low
6	A2	BLE_B	I	Transfers data from 64-bit latches to output latches when low
7	B4	BLE_C	I	Transfers data from 64-bit latches to output latches when low
8	A3	BLE_D	I	Transfers data from 64-bit latches to output latches when low
15	B6	CLK	I	Clock shift register data on rise/fall edge
18	B7	D_{IOA}	I/O	Shift register input data when DIR=L
19	B10	D_{IOB}	O/I	Shift register input data when DIR=H
14	A9	DIR	I	Controls the data shift directions
11	B5	GND	-	Logic ground
2	F5	HVGND	-	V_{PP} ground
22	F6	HVGND	-	V_{PP} ground
66	K5	HVGND	-	V_{PP} ground
66	L5	HVGND	-	V_{PP} ground
9	A4	$\overline{LE}$	I	Transfers data from shift register to 64-bit latches when high
3	B3	HI-Z	I	Set all HV outputs to high-Z state when low
20	B9	$\overline{OT}$	O	Signal for die over temperature detection
4	B2	POL	I	Output polarity control
21	B8	TEST	-	not used, leave open
10	A5	V_{DD}	-	Logic supply voltage
1	E5	V_{PP}	-	High voltage source supply
23	E6	V_{PP}	-	High voltage source supply
47	K6	V_{PP}	-	High voltage source supply
47	L6	V_{PP}	-	High voltage source supply
16, 17	A8, A10	N/C	-	No connect

High Voltage Outputs

Pad	Ball #	Name	Pad	Ball #	Name	Pad	Ball #	Name	Pad	Ball #	Name
89	D2	HV1	73	L1	HV17	56	Q6	HV33	39	K10	HV49
88	C2	HV2	72	M1	HV18	55	P6	HV34	38	J9	HV50
87	E2	HV3	71	K2	HV19	54	Q7	HV35	37	N10	HV51
86	D1	HV4	70	P1	HV20	53	Q9	HV36	36	J10	HV52
85	E1	HV5	69	N2	HV21	52	P7	HV37	35	H9	HV53
84	F2	HV6	68	L2	HV22	51	Q8	HV38	34	H10	HV54
83	C1	HV7	67	M2	HV23	50	Q10	HV39	33	G10	HV55
82	F1	HV8	65	P2	HV24	49	P8	HV40	32	F10	HV56
81	G2	HV9	64	P3	HV25	48	P9	HV41	31	G9	HV57
80	G1	HV10	63	Q1	HV26	46	M9	HV42	30	C10	HV58
79	H1	HV11	62	Q3	HV27	45	L9	HV43	29	E10	HV59
78	H2	HV12	61	P4	HV28	44	N9	HV44	28	F9	HV60
77	J1	HV13	60	Q2	HV29	43	P10	HV45	27	D10	HV61
76	N1	HV14	59	Q4	HV30	42	K9	HV46	26	C9	HV62
75	J2	HV15	58	P5	HV31	41	M10	HV47	25	E9	HV63
74	K1	HV16	57	Q5	HV32	40	L10	HV48	24	D9	HV64

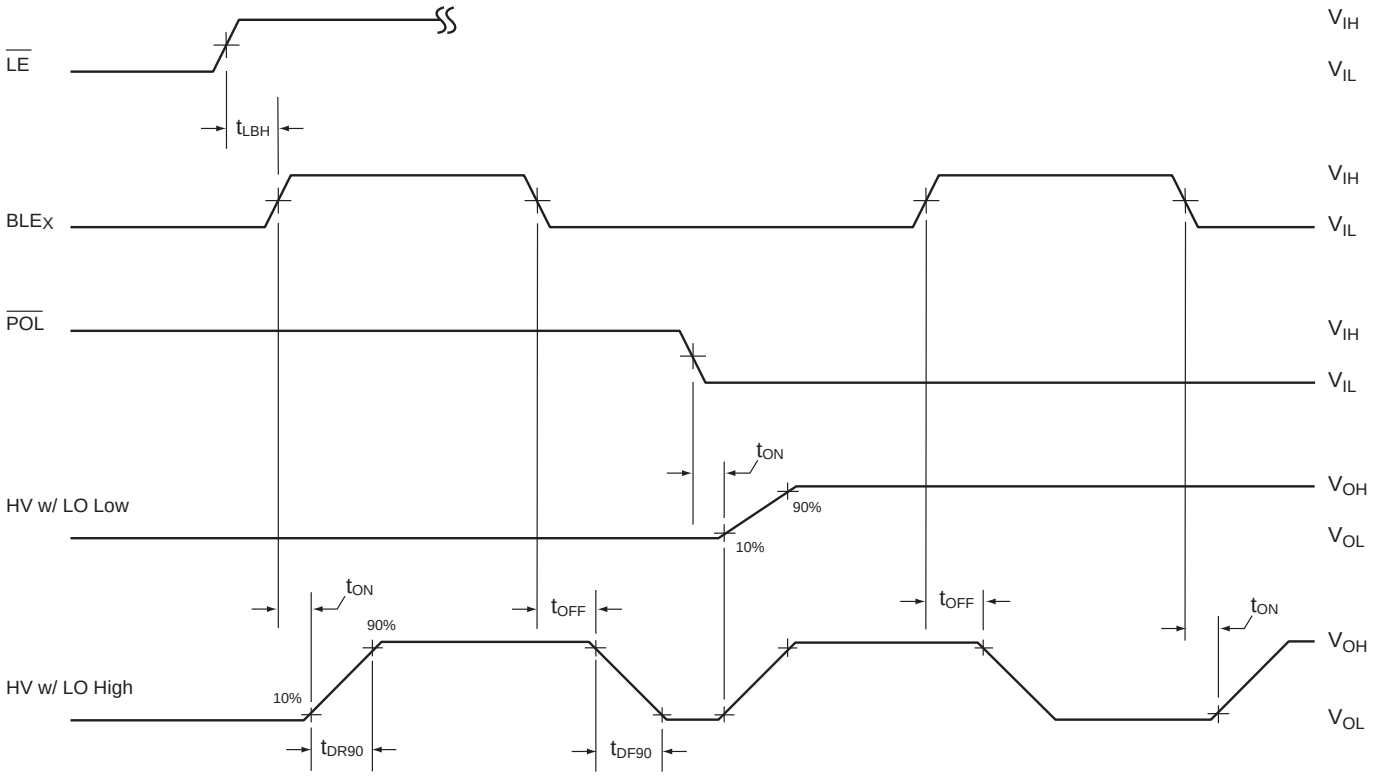
Switching Waveforms

Input Timing Diagram

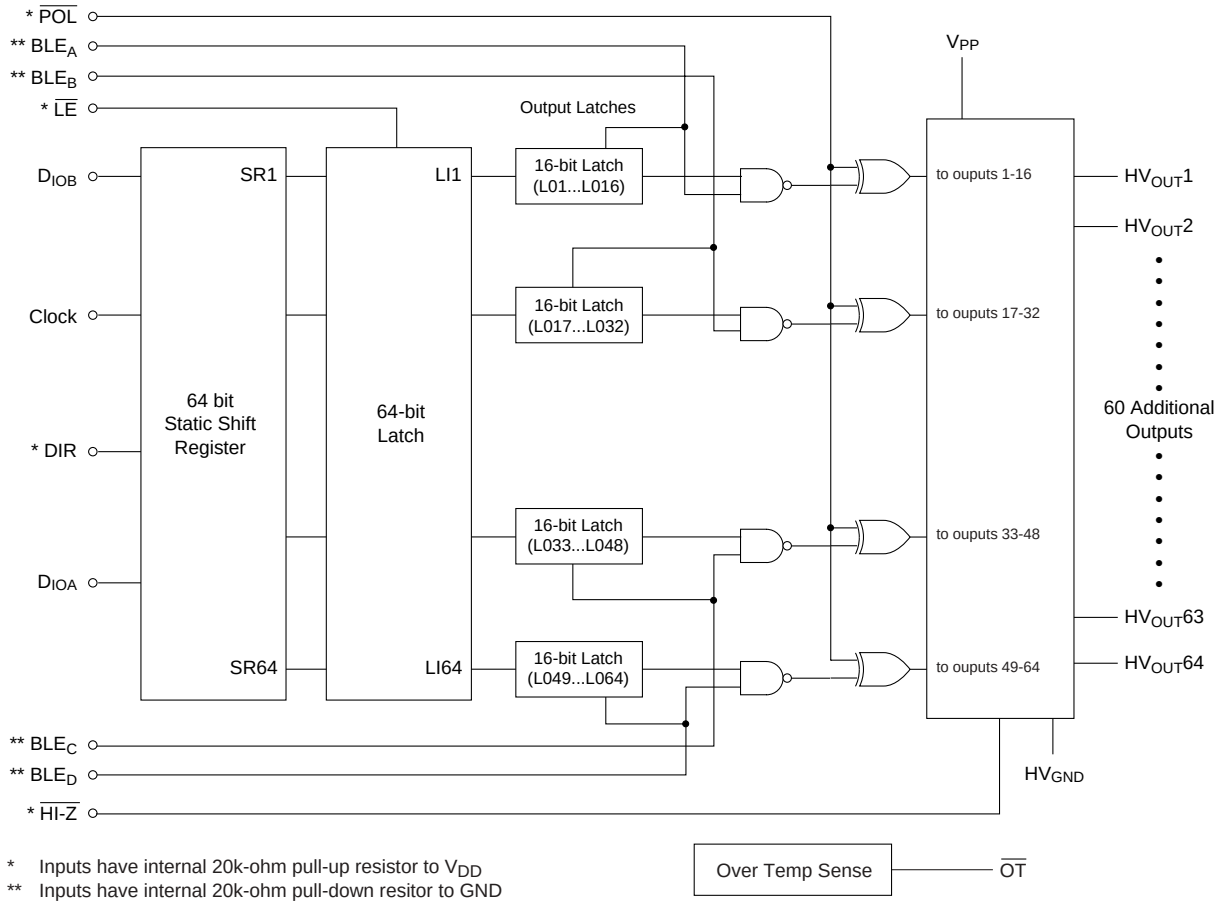


NOTE: First input data is loaded on rising clock edge.

Output Timing Diagram



Functional Block Diagram



* Inputs have internal 20k-ohm pull-up resistor to V_{DD}
** Inputs have internal 20k-ohm pull-down resitor to GND

Functional Table

Function	Data In	CLK	DIR	$\overline{LE}$	BLE_X	$\overline{POL}$	$\overline{Hi\text{-}Z}$	Data Out	Action
I/O Relation to Shift Register	D_{IOA}	↑	L					SR1 → D_{IOB}	Shift even registers; D_{IOA} → SR64 → SR62 ...
		↓						SR2 → D_{IOB}	Shift odd registers; D_{IOA} → SR63 → SR61 ...
	D_{IOB}	↑	H					SR64 → D_{IOA}	Shift odd registers; D_{IOB} → SR1→ SR3 ...
		↓						SR63 → D_{IOA}	Shift even registers; D_{IOB} → SR2 → SR4 ...
64-bit Latch transparent	X	X	X	H				N/A	SR_N LI_N
64-bit Latch held	X	X	X	L				N/A	LI_N held to previous value
HV outputs OFF	X	X	X	X	L	L	H	N/A	LI_N → LO_N; HV outputs High
	X	X	X	X		H	H	N/A	LI_N → LO_N; HV outputs Low
HV outputs ON	X	X	X	X	H	L	H	N/A	LO_N held to previous value; HV_{OUTN}=$\overline{LO_N}$
	X	X	X	X		H	H	N/A	LO_N held to previous value; HV_{OUTN}=LO_N
High-Z	X	X	X	X	X	X	L	N/A	Outputs have high impedance
Outputs functioning	X	X	X	X	X	X	H	N/A	Outputs operational

Typical Operation

(refer to the Functional Block Diagram and Function Table)

Data is first loaded into the 64-bit shift register using the clock, CLK, and data input lines, D_{IOA} or D_{IOB}. If the direction pin, DIR, is high, then data is shifted into D_{IOB} and out D_{IOA}; SR1 to SR64. If DIR is low, then data is shifted into D_{IOA} and out D_{IOB}; SR64 to SR1. The data rate is twice the CLK frequency. The first data bit is loaded on the rising clock edge and the next data is loaded on the falling edge; 32 complete clock cycles are required to load the 64-bit shift register. Data is transferred from 64-bit shift register to the 64-bit latch when the latch enable, $\overline{LE}$, is high. When $\overline{LE}$ is set low, data is retained in the 64-bit latch.

The blanking signals, BLE_A, BLE_B, BLE_C, and BLE_D, do two functions: blanking and data transfer from the 64-bit latch to the four 16-bit output latches. BLE_A controls HV outputs 1 through 16, BLE_B controls HV outputs 17 through 32, etc. When BLE_X is low, the high voltage, HV, outputs are blanked and data transfers from the 64-bit latch to the output latch. When BLE_X is high, the HV outputs are enabled and data in the output latch is retained. A blanked HV output combined with a high polarity signal, $\overline{POL}$, sets the HV output low. If $\overline{POL}$ is low, the blanked HV output is set high.

If BLE_X is high, the data in the 16-bit output latch are sent to the HV outputs. If $\overline{POL}$ is high the HV output is not inverted; a high data yields a high HV output. If $\overline{POL}$ is low, the HV output is inverted.

The control signal High-Z, $\overline{HI\text{-}Z}$, sets the HV outputs to a high impedance state. If $\overline{HI\text{-}Z}$ is high, the outputs can be set to either high or low. If $\overline{HI\text{-}Z}$ is low, the outputs are set to a high impedance state, both output transistors are turned off.

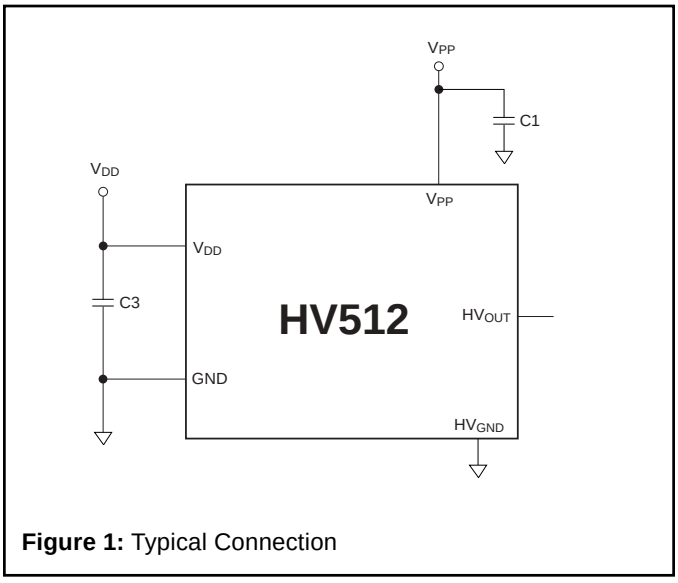


Figure 1: Typical Connection

Die Temperature Sensing

A signal is provided for die over-temp sensing, $\overline{OT}$. A CMOS digital LOW signal will be provided when the center of the die temperature exceeds T_{TRIP}. This will be a non-synchronized, non-latched, continuously monitored output that will contain hysteresis to prevent oscillation at the threshold temperature. This circuit is driven by the analog supply, AV_{DD} and AGND.

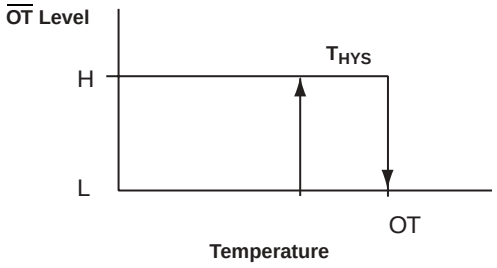
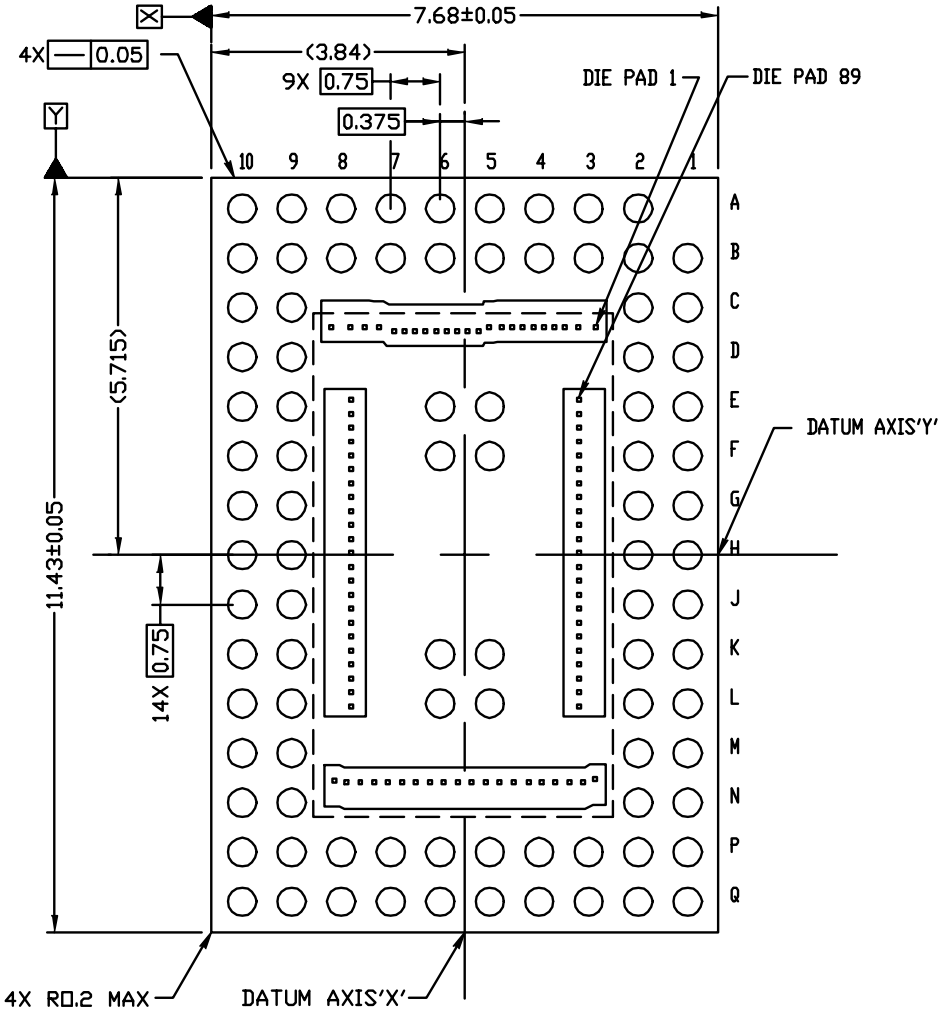


Figure 2: Over-temp/Hysteresis Performance

μBGA® PACKAGE, 91 BALL, 15x10 ARRAY ASSEMBLY DRAWING

(Unless Otherwise Specified, Dimensions are in Millimeters)



Bump View

NOTES:

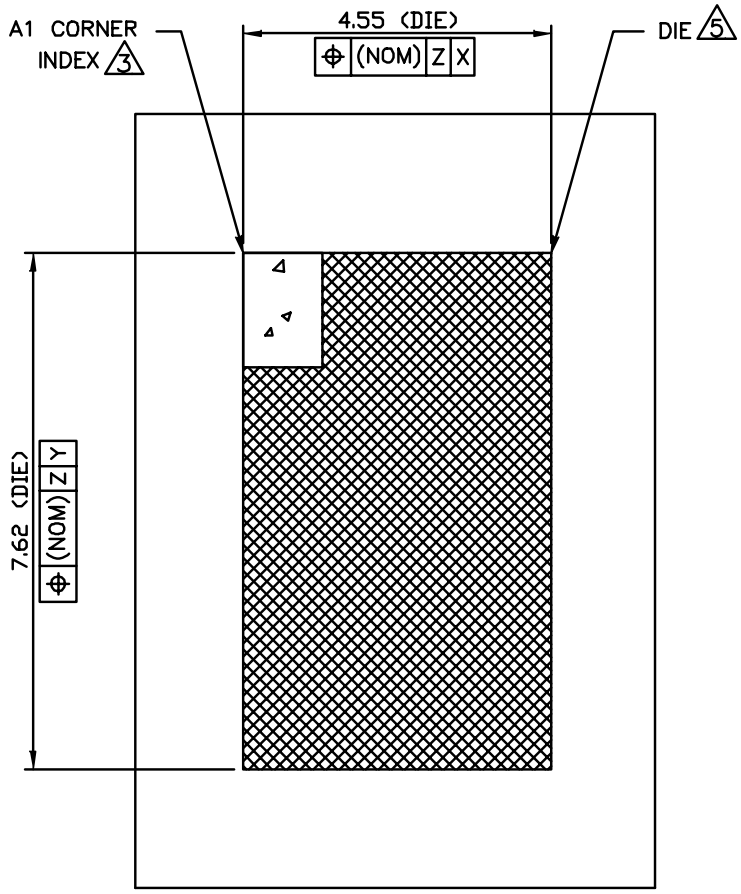
1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Do not subject part to ultrasonic cleaning or intense UV.
3. Mark back of die with laser.
4. Contact ball position designation per JESD 95-1, SOO-010.
5. Die P/N HV512.
6. Elastomer

   106000200108 (Dow Corning 6811 Encapsulant).

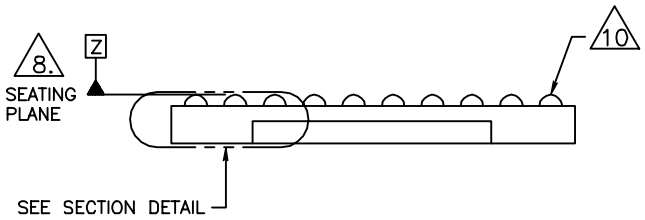
   1030001000108 (Dow Corning 6910 Space Adhesive).
7. Make from Eutectic Solder Ball (ø0.3mm). Dimensions apply after solder ball reflow.
8. Datum Z established by high points of solder bumps.
9. Elastomer shall not extend beyond Datum A.
10. Max. vertical load allowed per ball of 40 grams.

μBGA® PACKAGE, 91 BALL, 15x10 ARRAY ASSEMBLY DRAWING, Continued

(Unless Otherwise Specified, Dimensions are in Millimeters)



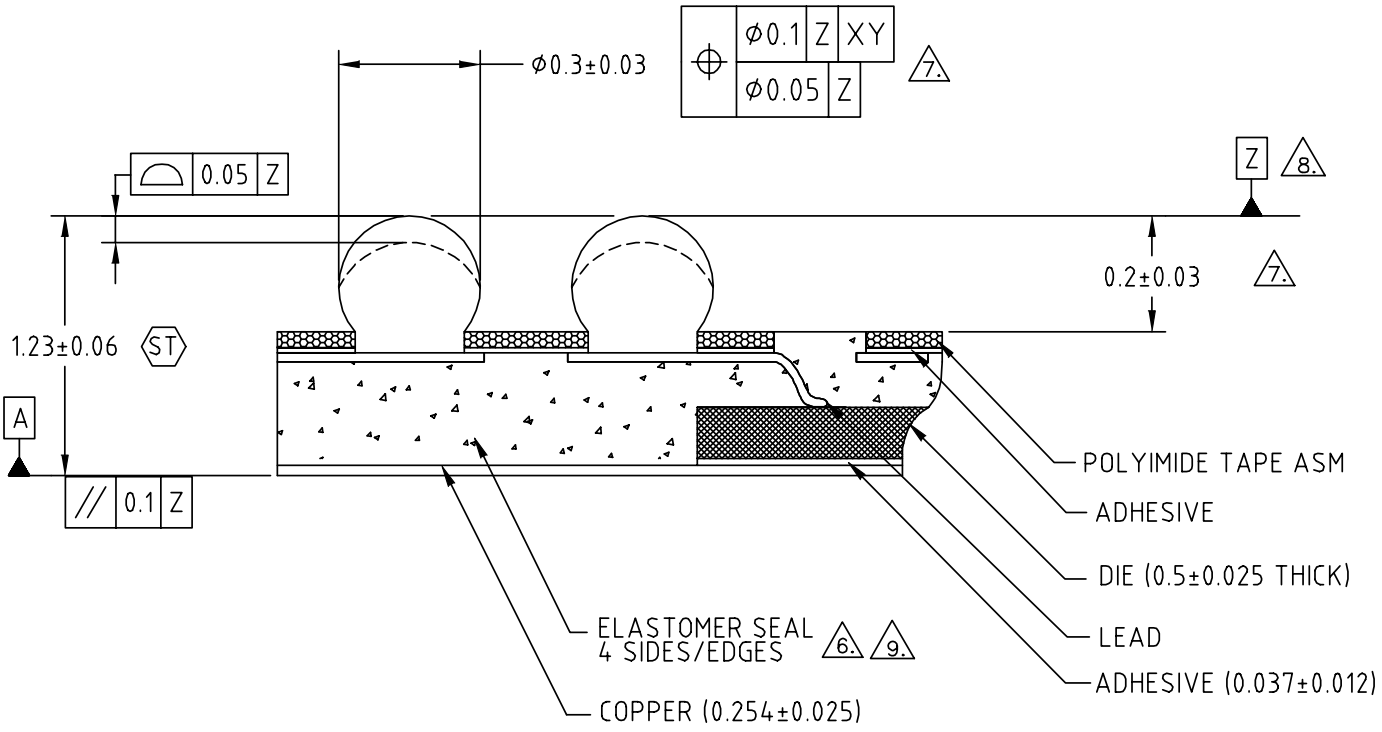
Back View



Side View
(Not to Scale)

μBGA® PACKAGE, 91 BALL, 15x10 ARRAY ASSEMBLY DRAWING, Continued

(Unless Otherwise Specified, Dimensions are in Millimeters)



GENERAL ASSEMBLY SECTION
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