HIP2030

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July 1998

30V MCT/IGBT Gate Driver

Features

- ± Polarity Gate Drive
- High Output Voltage Swing. 30V
- Peak Output Current 6.0A
- Fast Rise Time . . . . . .200ns at 60,000pF
- Ability to Interface and Drive P-MCTs
- Programmable Minimum ON/OFF Time
- Gate Output Inhibit Latch
- 5V Reference . . . . . .Sinks Up to 30mA
- High Side Charge Pump
- 120kHz Operation . . . . . at 15,000pF

Applications

- Motor Controllers
- Uninterruptible Power Supplies
- Resonant Inverters
- Static Circuit Breakers
- Inverters
- Converters
- Arc Welders

Description

The HIP2030 is a medium voltage integrated circuit (MVIC) capable of driving large capacitive loads at high voltage slew rates (dv/dts). This device is optimized for driving 60nF of MOS gate capacitance at 30V peak to peak in less than 200ns. The half bridge gate driver is ideal for driving MOS Controlled Thyristor (MCT) and IGBT modules.

The architecture of the HIP2030 includes four comparator input channels, a 5V regulator, a 12V clamp, and a high side charge pump. The device provides the user with the ability to control minimum low time (MLT) and minimum high time (MHT) at the gate channel output (GO) by varying two external capacitances. In addition, the device contains two uncommitted comparator channels (channels A and B) that can be used as monitors (temperature sensing), indicators (LEDs or opto-couplers), input signal conditioning (both contain Schmitt triggers), or oscillators.

The power requirements of the HIP2030 are low. The driver can be easily configured to operate in one of three power configurations. This allows the use of a small PCB mountable transformer or battery to provide isolated power to the driver chip.

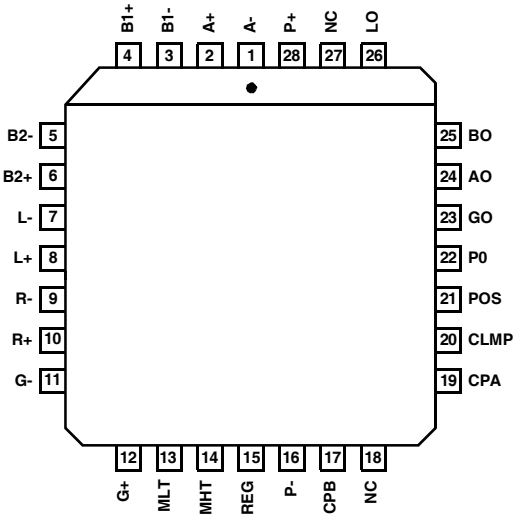
The HIP2030 supplies high output current drive to large capacitive loads and requires few external components to implement a wide variety of MOS gate driver circuits.

Ordering Information

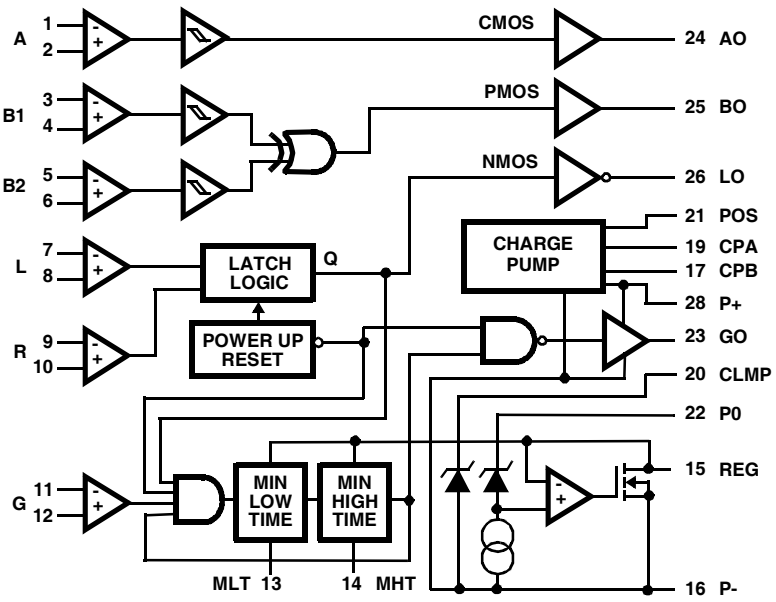
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP2030IM	-40°C to +110°C	28 Lead PLCC

Pinout

HIP2030 (PLCC)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 321-724-7143 | Intersil (and design) is a registered trademark of Intersil Americas Inc.

File Number **3691.3**

Absolute Maximum Ratings

Gate Channel Supply Voltage, P+ to P- . . . . . -0.5V to 32V
Logic Supply Voltage, P0 to P- . . . . . 7V to 18V
All Other Pin Voltages
(A+, A-, B1+, B1-, B2+, B2-, L+, L-, R+, R-) . . . . . (P-)-0.5 to (P+)+0.5

Thermal Information

Thermal Resistance θ_{JA}
PLCC Package . . . . . $60^oC/W$
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Junction Temperature . . . . . $+150^oC$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

$T_J = -40^oC$ to $+150^oC$ Unless Otherwise Noted, All Voltages Referenced to P-

Gate Channel Supply Voltage, P+ to P- . . . . . -0.5V to 30V
Logic Supply Voltage, P0 to P- . . . . . 10V to 15V
All Other Pin Voltages
(A+, A-, B1+, B1-, B2+, B2-, L+, L-, R+, R-) . . . . . (P-)+2V to (P0)+2V
Max Output Source Current, Channels A, B 10mA
Max Output Sink Current, Channels A, L 10mA
Min Load Current, Reg to P- 2mA
(Required for Proper Chip Operation)
Max Load Current, Reg to P- 30mA

Static Electrical Specifications

P0 to P- = 15V, P+ to P- = 30V, P- = 0V, Reg to P- = 2mA. Full Temp $T_J = -40^oC$ to $+150^oC$

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
I_{P0}	P0 Quiescent Supply Current		Full	-	3.5	5	mA
I_{P+}	P+ Quiescent Supply Current		+25°C	-	1	10	µA
			Full	-	-	250	µA
I_{QPOS}	POS Quiescent Supply Current	Osc Freq = 100kHz	Full	-	3	5	mA
BV_{P+}	P+ to P- Breakdown Voltage	I_{BV} = 100µA	Full	30	35	-	V
V_{REG}	Regulator Voltage, P0 to Reg	I_{REG} = 2mA	+25°C	4.4	5.2	6.0	V
			Full	4.0	-	6.5	V
R_{REG}	Regulator Impedance, P0 to Reg	I_{REG} = 10mA, 30mA	Full	3	8	17	Ω
V_{CLMP}	Clamp Voltage, CLMP to P-	I_{CLMP} = 15mA	Full	11	12.5	14	V
R_{CLMP}	Clamp Impedance, CLMP to P-	I_{CLMP} = 15mA, 30mA	Full	7	20	32	Ω
F_{CP}	Charge Pump Frequency		Full	-	200	-	kHz
D_{CP}	Charge Pump Duty Cycle		Full	-	50	-	%
VO_{CP}	Charge Pump $V_{OUT,}$ P+ to P-	IP+ = 500µA	Full	28	28.5	29	V
VO_{CP}	Charge Pump $V_{OUT,}$ P+ to P-	IP+ = 4mA	Full	26.5	27.5	28.5	V
I_{IN}	Comparator Input Leakage	VIN_{CMP} = VP0/2	Full	-	.01	1	µA
V_{OS}	Comparator Offset Voltage	V_{CM} = VP0/2	Full	-	10	50	mV
VCM	Comparator Common Mode Voltage Range		Full	(VP-)+2	-	VP0+2	V
RGO_{SRC}	GO Output RDS, Sourcing	I_{SRC} = 2A	+25°C	-	.6	1	Ω
			Full	-	-	1.5	Ω
RGO_{SNK}	GO Output RDS, Sinking	I_{SNK} = 2A	+25°C	-	2	3	Ω
			Full	-	-	4	Ω
RDS_{SRC}	AO, BO Output RDS, Sourcing	I_{SRC} = 10mA	+25°C	-	85	150	Ω
			Full	-	-	175	Ω
RDS_{SNK}	AO, LO Output RDS, Sinking	I_{SNK} = 10mA	+25°C	-	75	125	Ω
			Full	-	-	150	Ω

Dynamic Electrical Specifications

P0 to P- = 15V, P+ to P- = 30V, P- = 0V, Ref to P- = 2mA. Full Temp $T_J = -40^oC$ to $+150^oC$

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
TH_{MIN}	Min GO Output Hi Duration	C_{LOAD} = 20pF	Full	600	1100	1600	ns
TL_{MIN}	Min GO Output Lo Duration	C_{LOAD} = 20pF	Full	200	750	1500	ns
TP_{LHAB}	Prop Delay, Lo - Hi, Chs. A, B	C_{LOAD} = 300pF	Full	-	90	150	ns
TP_{LHL}	Prop Delay, Lo - Hi, Ch. L	C_{LOAD} = 300pF, V_{OD} = 2V	Full	-	115	170	ns

Dynamic Electrical Specifications P0 to P- = 15V, P+ to P- = 30V, P- = 0V, Ref to P- = 2mA. Full Temp T_J = -40°C to +150°C **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
TP_{HLA}	Prop Delay, Hi - Lo, Ch. A	C_{LOAD} = 300pF, V_{OD} = 2V	Full	-	200	320	ns
TR_{AB}	Rise Time, Channels A, B	C_{LOAD} = 300pF, V_{OD} = 2V	Full	-	20	50	ns
TF_{AL}	Fall Time Channels A, L	C_{LOAD} = 300pF, V_{OD} = 2V	Full	-	50	75	ns
TP_{LHG}	Prop Delay, Lo - Hi, Ch. G	C_{LOAD} = 60nF, V_{OD} = 2V	+25°C	-	135	200	ns
			Full	-	-	275	ns
TP_{HLG}	Prop Delay, Hi - Lo, Ch. G	C_{LOAD} = 60nF, V_{OD} = 2V	+25°C	-	280	400	ns
			Full	-	-	475	ns
TR_G	Rise Time, Channel G	C_{LOAD} = 60nF, V_{OD} = 2V	+25°C	-	150	300	ns
			Full	-	-	450	ns
TF_G	Fall Time Channel G	C_{LOAD} = 60nF, V_{OD} = 2V	+25°C	-	235	340	ns
			Full	-	-	500	ns

Timing Waveforms

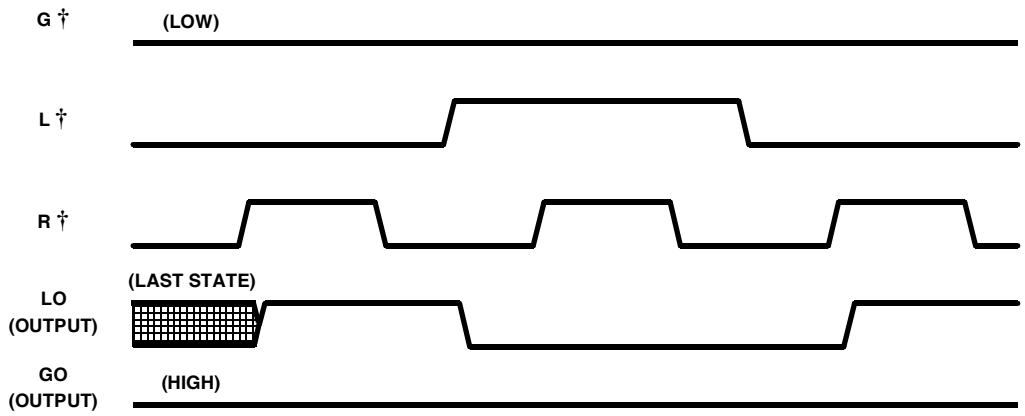
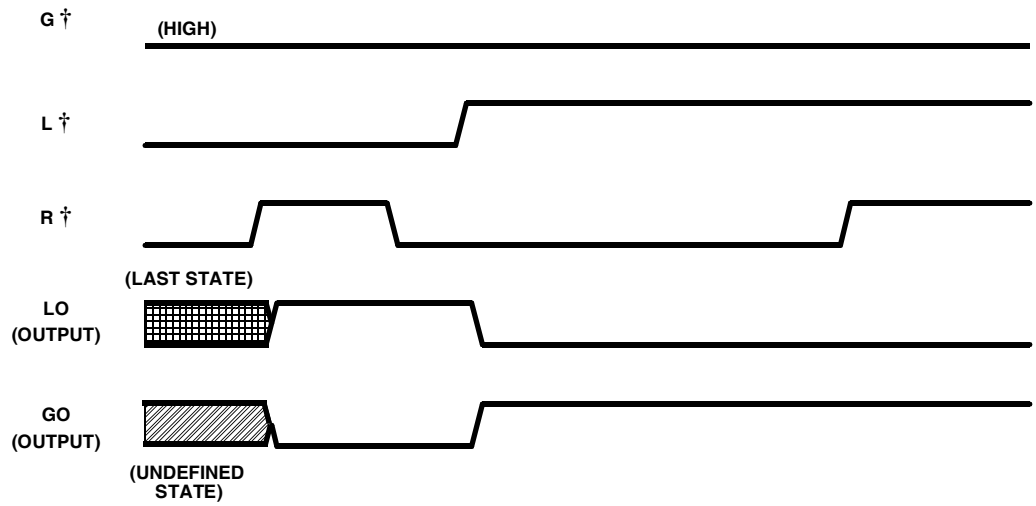


FIGURE 1.



† Refers to the state of the input comparator output

FIGURE 2.

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	A-	Negative Comparator input for A channel. This input has a Protected Comparator Input that is clamped to P+ and P- through a 330 ohm resistor. The common mode input voltage, for the Protected Comparator Input, ranges from (VP-) +2V and (VP0) +2V. The CMOS output AO (Pin 24) is low when input A- is “True” and input A+ is “False”.
2	A+	Positive Comparator Input for A channel. The CMOS output AO (Pin 24) is high when input A+ is “True” and input A- is “False”.
3	B1-	Negative Comparator input for B1 channel. The output of the internal B1-channel comparator is low when input B1- is “True” and input B1+ is “False”.
4	B1+	Positive Comparator Input for B1 channel. The output of the internal B1-channel comparator is high when input B1+ is “True” and input B1- is “False”.
5	B2-	Negative Comparator Input for B2 channel. The output of the internal B2-channel comparator is low when input B2- is “True” and input B2+ is “False”.
6	B2+	Positive Comparator Input for B2 channel. The output of the internal B2-channel comparator is high when input B2+ is “True” and input B2- is “False”.
7	L-	Negative Comparator Input for L (Latch) channel. Latch mode operation is disabled when L- is “True” and L+ is “False”. NMOS output LO (Pin 26) is active high in a no latch state. The GO output (Pin 23) is controlled by G-channel inputs.
8	L+	Positive Comparator Input for L (Latch) channel. Latch mode operation is enabled when L+ is “True” and L- is “False”. NMOS output LO (Pin 26) is active low in latch state. The GO output (Pin 23) goes to a “P-MCT OFF” state (VGO = VP+) and is controlled by the internal L-channel latch; which bypasses the G-channel inputs. Latch mode always overrides the R-channel.
9	R-	Negative Comparator Input for R (Reset) channel. Reset mode, for the internal L-channel latch, is disabled when R- is “True” and R+ is “False”.
10	R+	Positive Comparator Input for R (Reset) channel. Reset mode, for the internal L-channel latch, is enabled when R+ is “True” and R- is “False”. Reset mode (enabled) unlatches the internal L-channel latch; which allows the G-channel inputs to control the GO output (Pin 23). Latch mode must be disabled to operate in reset mode.
11	G-	Negative Comparator Input for G (Main) channel. The G-channel output (Pin 23) goes to a “P-MCT OFF” state (VGO = VP+) when G- is “True” and G+ is “False”.
12	G+	Positive Comparator Input for G (Main) channel. The G-channel output (Pin 23) goes to a “P-MCT ON” state (VGO = VP-) when G+ is “True” and G- is “False”.
13	MLT	Input for programmable Minimum Low Time timing capacitor (C_T). MLT is set by connecting a capacitor between P0 (Pin 22) and MLT (Pin 13). MLT is approximated by the equation: (C_T)(5V)/(100uA).
14	MHT	Input for programmable Minimum High Time timing capacitor (C_T). MHT is set by connecting a capacitor between P0 (Pin 22) and MHT (Pin 14). MHT is approximated by the equation: (C_T)(5V)/(100μA). MHT becomes Minimum Low Time function for turning on N-MCT’s.
15	REG	5V regulator output. An opto-coupler or fiber-optic receiver may be power by connecting the positive voltage pin of the IC to P0 (Pin 22) and the IC common to REG (Pin 15). The internal regulator (REG) must sink 2mA of current minimum for the MLT and MHT functions to work properly.
16	P-	Chip negative supply. This pin is generally used as the DC bias power supply common. The regulator transistor, charge pump and logic are referenced to P- (Pin 16).
17	CPB	Output of the Charge Pump Oscillator Inverter stage. A 0.47μF capacitor is normally connected from this output to CPA (Pin 19).
18	NC	Unused pin.
19	CPA	Input of the charge pump steering diode. A 0.47μF capacitor is normally connected from this input to CPB (Pin 18).

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	DESCRIPTION
20	CLMP	An internal 12V clamp that can be used for additional regulation across P0 (Pin 22) and P- (Pin 16).
21	POS	Positive supply rail for the charge pump.
22	P0	Chip positive supply. This pin is generally used as the DC bias power supply positive input.
23	GO	Main channel output (Gate Output). The gate output controls the switching of power devices and is normally connected to the P-MCT gate. GO can sink or source greater than 6A peak at VP+ equal to 30V.
24	AO	A-Channel Output. AO has a CMOS output that switches from P0 (Pin 22) to P- (Pin 16). AO can source or sink 10mA of DC current.
25	BO	B-Channel Output. B-channel has a PMOS output that connects BO to P0 (Pin 22) when turned on. BO can source 10mA of DC current from P0.
26	LO	L-Channel Output. L-channel has a NMOS output that connects LO to P- (Pin 16) in latch mode. LO can sink 10mA of DC current.
27	NC	Unused pin.
28	P+	High side output. Connects to the output of a charge pump steering diode. A 10.0µF capacitor is normally connected from this output to P0 (Pin 22) to supply the high side of the gate voltage.

HIP2030 Application Information

The **Intersil Photo-Coupled Isolated Gate Drive** (HPCIGD) circuit, illustrated in Figure 3, contains four subcircuits: a Single Supply DC bias, a Regulated voltage divider reference, a Local Energy Source Capacitance, and a Photo-Couple Receiver.

The **Single Supply DC Bias Circuit**, shown in Figure 3, consists of a single external dropping resistor (R1) connected between pins P+ (U1-28) and P0 (U1-22). When an input voltage of 30V is applied across pins P+ and P- (U1-16), R1 forms a resistive divider network with the input impedance located between pins P0 and P- (RVP0). This allows the circuit designer to adjust the value of R1 to obtain a desired bias voltage between pins P0 and P- (VP0.). The value of RVP0 can be calculated by evaluating the equivalent Quiescent Input Impedance (RQ) and the 5V reference impedance (RR) as parallel resistances. The values for R1, RQ, RR, and RVP0 can be determined by using Equations 1(A, B, C, D) as shown in Appendix A, Exercise 1.1.

The **Regulated Voltage Divider Reference** is comprised of two resistors (R3 and R4) connected in series and are located across pins P0 and REG. This voltage divider provides a stable voltage reference to all of the HIP2030 comparator inputs. Resistors R3 and R4 are selected equal in value to create a midpoint bias reference between the peak to peak input signal of U2. Also, the midpoint bias method ensures that input signals generated from U2 and midpoint bias reference voltages are within a safe common mode voltage range of the comparators.

The **Local Energy Source Capacitances**, C1 and C2, are needed to supply the charge required to drive large capacitance loads at high dv/dts. The HPCIGD circuit uses low cost "oversized" tantalum capacitors (C = 10µF) that are used for C1 and C2. If rise times and overshoot are critical, ceramic capacitors with low ESL and ESR should be used to improve gate drive signals. In a power circuit, where the gate driver is exposed to high dv/dts, the network of C1 and C2 directs noise current away from the HIP2030. This allows the HFOIGD circuit to operate well in half bridge power circuits that use a transformer coupled power source.

The **Photo-Coupled Receiver** subcircuit consists of U2, R5, C4, and R6. U2 is a photocoupler which combines an infrared emitter diode (IRED) and a high speed photo detector to translate light pulses to low voltage input signals. These signals are routed to the G channel and are used to control the output GO. Component R5 is used to limit the DC current through the IRED when the input signal voltage switches to its most positive level. A wide range of input voltages may be accommodated by varying R5 to limit the IRED current to 25mA. C4 is a speed up capacitor and is selected to match the forward bias capacitance of the IR diode. The last component, R6, is an optional part and is intended to be a termination resistor with the value set by the user.

The Intersil HIP2030 Evaluation Board (HIP2030EVAL) is a printed circuit board (PCB) developed to help evaluate the performance of the HIP2030 MCT/IGBT Driver IC in power switching circuits. The component layout of the HIP2030DB circuit enables the user to conveniently populate the PCB for either Photo-Coupled or fiber-optic receivers. In addition, the PCB layout has provisions for "on board prototyping" and special function components. This facilitates the gate drive circuit design and allows the user to exercise the internal architecture and special functions of the HIP2030. The schematic of the HIP2030DB, illustrated in Figure 4, uses the basic HPCIGD circuitry and has provisions for "on board prototyping" and special function components.

TABLE 1. LOGIC

INPUTS			OUTPUTS	
G	L	R	LO	GO
0	0	0	LS	H
0	0	1	H	H
0	1	0	L	H
0	1	1	L	H
1	0	0	LS	U
1	0	1	H	L
1	1	0	L	H
1	1	1	L	H

1 = Input True
0 = Input False

U = Undefined
LS = Last State

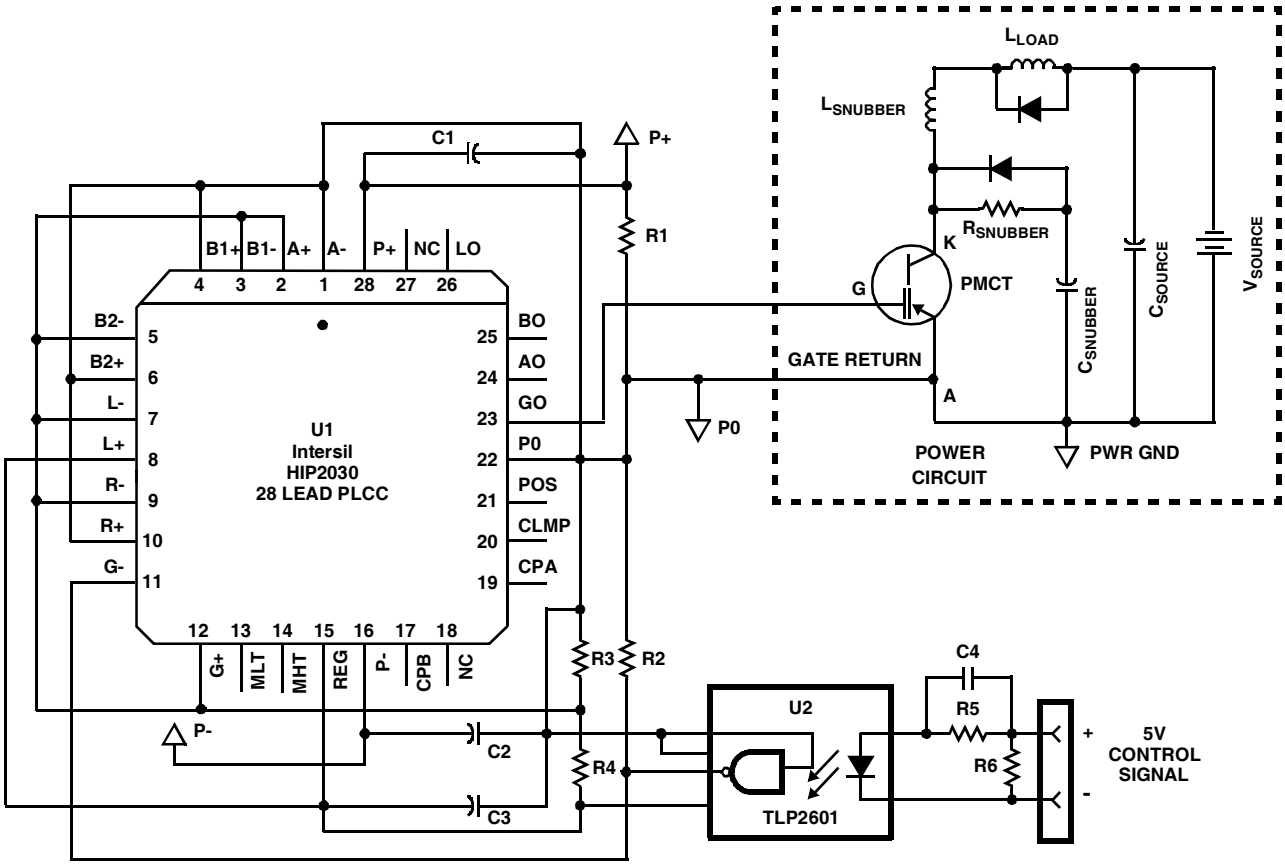


FIGURE 3. INTERSIL PHOTO-COUPLED ISOLATED GATE DRIVE

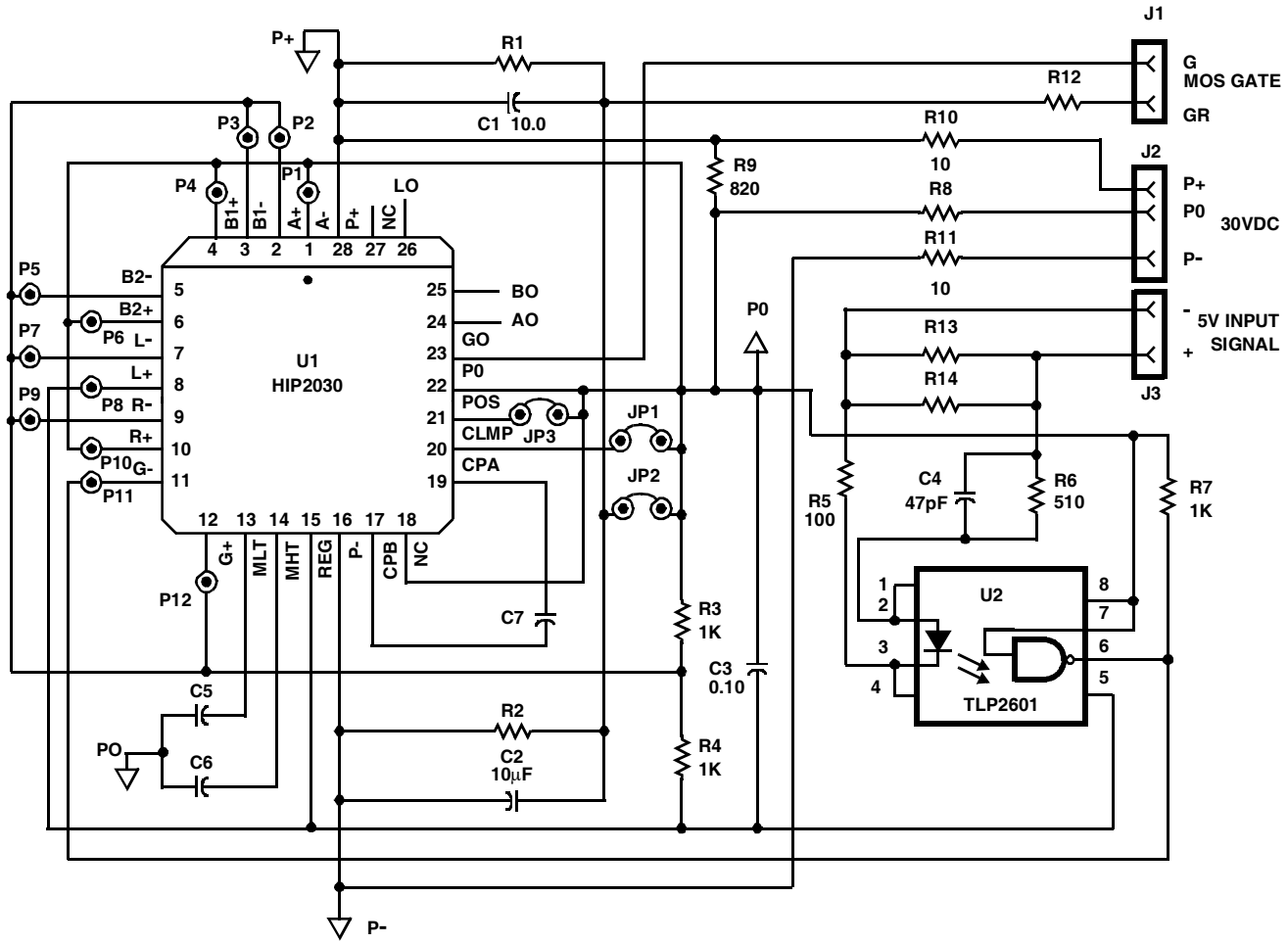


FIGURE 4. INTERSIL HIP2030 EVALUATION BOARD (NOTE 9)

NOTES:

1. Capacitors C5 and C6 are special function components which control MLT and MHT.
2. Asymmetrical gate drive may be obtained by opening J2 and adjusting R1 and R2 for the desired voltage ratio.
3. Insert C7 for charge pump operation.
4. Open J3 to disable the charge pump oscillator.
5. Open J1 to disable the internal 12V regulator.
6. R5 is added for noise rejection at high Cdv/dts.
7. The internal 5V reference (REF) must be operational for MHT and MLT functions to work properly.
8. P1 - P12 are access pads for all comparator inputs.
9. Request Intersil File #3918 for a full description of the HIP2030EVAL board.

Typical Performance Curves

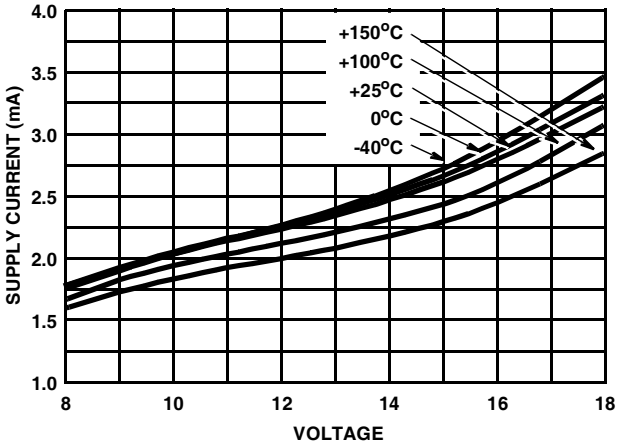


FIGURE 5. SUPPLY CURRENT (IP0) vs SUPPLY VOLTAGE (P0)

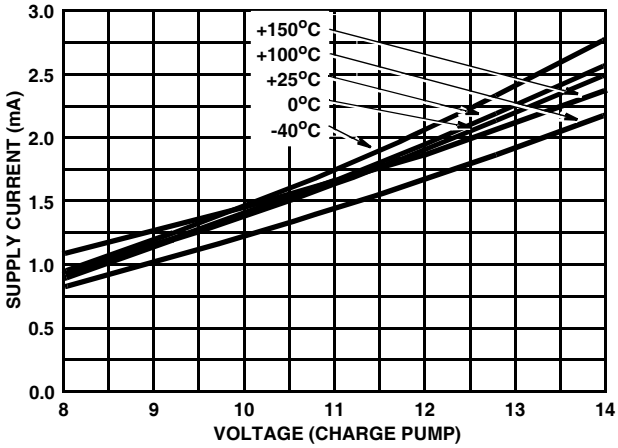


FIGURE 6. SUPPLY CURRENT (IPOS) vs SUPPLY VOLTAGE (POS)

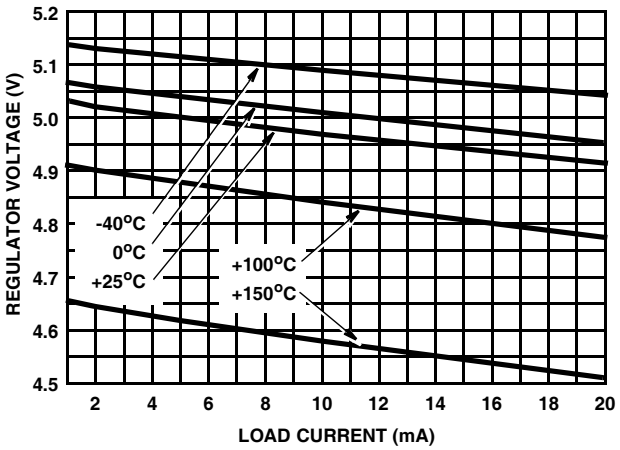


FIGURE 7. REGULATOR VOLTAGE vs LOAD CURRENT

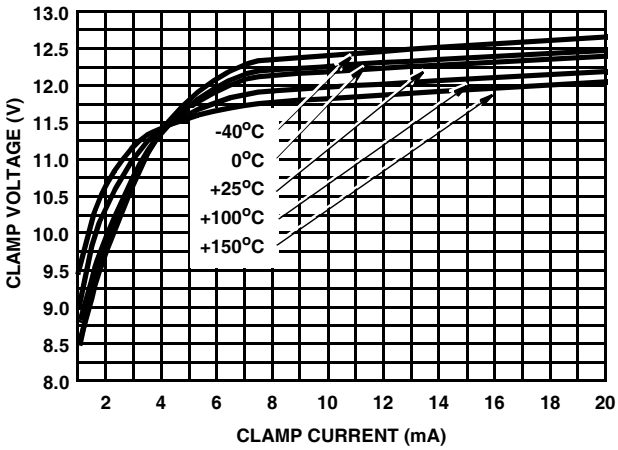


FIGURE 8. CLAMP VOLTAGE vs CLAMP CURRENT

Typical Performance Curves (Continued)

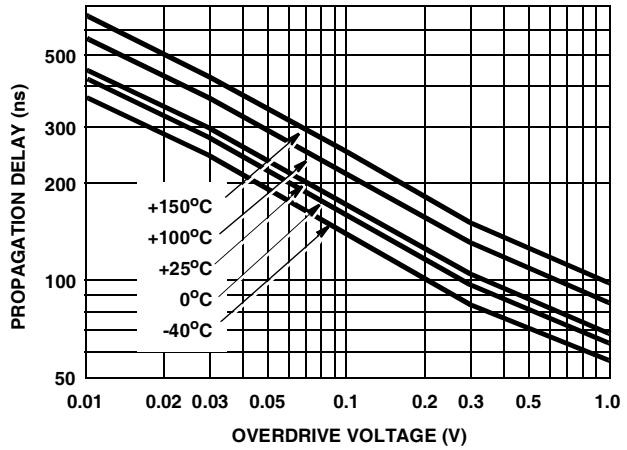


FIGURE 9. PROPAGATION DELAY vs VOLTAGE OVERDRIVE FOR A, B1, AND B2 CHANNELS

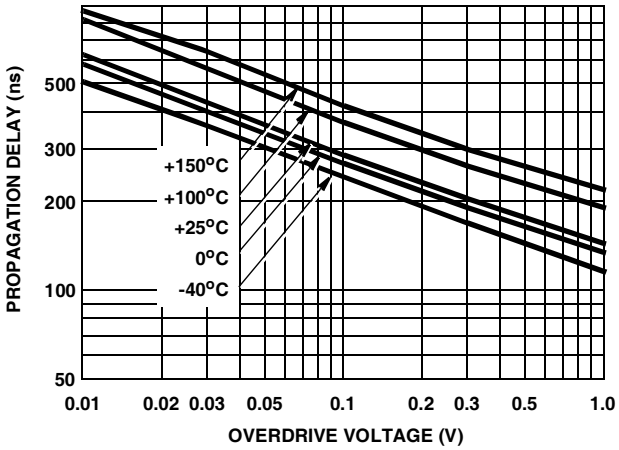


FIGURE 10. PROPAGATION DELAY vs VOLTAGE OVERDRIVE FOR G CHANNEL

Appendix A Exercises

Exercise 1.1

Q: How do I calculate the value of the series dropping resistor R1, shown in Figure 3?

A: The values for R1, R_Q, R_R and R_{VPO} can be determined by using Equations 1 (A, B, C, and D).

$$R_Q = \frac{V_{PO}}{I_{QPO}} \quad \text{(EQ. 1A)}$$

$$R_R = \frac{V_{PO}}{I_{OPTO} + I_{VDR} + I_{RP}} \quad \text{(EQ. 1B)}$$

$$R_{VPO} = \frac{1}{\frac{1}{R_Q} + \frac{1}{R_R}} \quad \text{(EQ. 1C)}$$

Where: V_{PO} = Voltage between pins P0 and P- (U1 - U22 and U1 - U16).

I_{QPO} = Quiescent current flowing into pin P0.

I_{QPTO} = Quiescent current of the HBR-2521 fiber-optic receiver.

I_{VDR} = Current flowing through R3 and R4 (voltage divider reference).

I_{RP} = Current flowing through pull up resistor R2 (in “ON” or “OFF” state)

The maximum value of R1 can easily be determined in four design steps:

1. Assume the following values:

V_{IN} = 30V DC

I_{QPO} = 2.75mA at V_{P0} = 15V

I_{OPTO} = 5mA

I_{VDR} = 2.5mA

$I_{RP(ON)}$ = 5mA, R2 = 1K, VR2 = 5V

2. Select a usable value of V_{P0} between 7V and 15V DC.

   Use V_{P0} = 15V

3. Solve for R_{VP0} using Equations 1 (A, B, and C):

$$R_Q = \frac{15V}{2.75mA} = 5.45K$$

$$R_R = \frac{15V}{(5mA + 2.5mA + 5mA)} = 1.20K$$

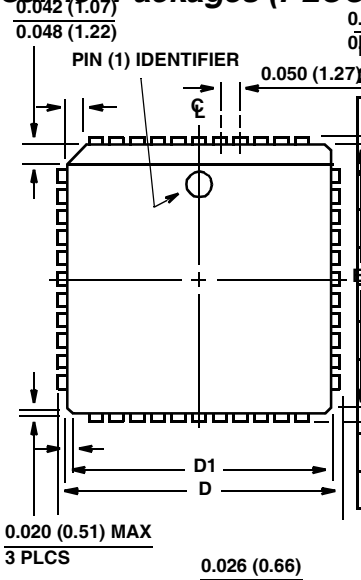
$$R_{VP0} = \frac{1}{\frac{1}{5.45K} + \frac{1}{1.20K}} = 984$$

4. Solve for R1 using Equation 1(D):

$$R1 = \frac{R_{VP0}(V_{IN} - V_{P0})}{V_{P0}} \quad \text{(EQ. 1D)}$$

$$R1 = \frac{984(30V - 15V)}{15V} = 984$$

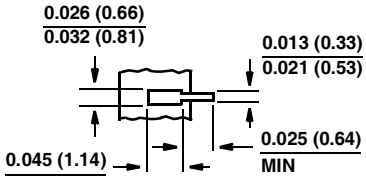
Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	165	0.180	4.20	4.57	-
A1	090	0.120	2.29	3.04	-
D	485	0.495	12.32	12.57	-
D1	450	0.456	11.43	11.58	3
D2	191	0.219	4.86	5.56	4, 5
E	485	0.495	12.32	12.57	-
E1	450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 1 3/95



VIEW "A" TYP.

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.