HD74ALVC16831

1-bit to 4-bit Address Register Driver with 3-state Outputs

HITACHI

Description

This 1-bit to 4-bit address register / driver is designed for 2.3 V to 3.6 V V_{cc} operation. The device is ideal for use in applications where a single address bus is driving four separate memory locations. The HD74ALVC16831 can be used as a buffer or a register, depending on the logic level of the select ($\overline{SEL}$) input. When $\overline{SEL}$ is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output enable ($\overline{OE}$) controls. Each $\overline{OE}$ controls two groups of nine outputs. When $\overline{SEL}$ is logic low, the device is in the register mode. The register is an edge triggered D-type flip flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. $\overline{OE}$ controls operate the same as in buffer mode. When $\overline{OE}$ is logic low, the outputs are in a normal logic state (high or low logic level). When $\overline{OE}$ is logic high, the outputs are in the high impedance state. To ensure the high impedance state during power up or power down, $\overline{OE}$ should be tied to V_{cc} through a pullup registor; the minimum value of the registor is determined by the current sinking capability of the driver. $\overline{SEL}$ and $\overline{OE}$ do not affect the internal operation of the flip flops. Old data can be retained or new data can be entered while the outputs are in the high impedance state.

Features

- V_{cc} = 2.3 V to 3.6 V

- Typical V_{OL} ground bounce < 0.8 V (@V_{cc} = 3.3 V, Ta = 25°C)

- Typical V_{OH} undershoot > 2.0 V (@V_{cc} = 3.3 V, Ta = 25°C)

- High output current ±24 mA (@V_{cc} = 3.0 V)

HD74ALVC16831

Function Table

Inputs				Output Y
$\overline{OE}$	$\overline{SEL}$	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

H : High level
L : Low level
X : Immaterial
Z : High impedance
↑ : Low to high transition

HITACHI

Pin Arrangement

Left	Pin		Pin	Right
4Y1	1		80	1Y2
3Y1	2		79	2Y2
GND	3		78	GND
2Y1	4		77	3Y2
1Y1	5		76	4Y2
V$_{CC}$	6		75	V$_{CC}$
NC	7		74	1Y3
A1	8		73	2Y3
GND	9		72	GND
NC	10		71	3Y3
A2	11		70	4Y3
GND	12		69	GND
NC	13		68	1Y4
A3	14		67	2Y4
V$_{CC}$	15		66	V$_{CC}$
NC	16		65	3Y4
A4	17		64	4Y4
GND	18		63	GND
CLK	19		62	1Y5
$\overline{OE1}$	20		61	2Y5
$\overline{OE2}$	21		60	3Y5
$\overline{SEL}$	22		59	4Y5
GND	23		58	GND
A5	24		57	1Y6
A6	25		56	2Y6
V$_{CC}$	26		55	V$_{CC}$
A7	27		54	3Y6
NC	28		53	4Y6
GND	29		52	GND
A8	30		51	1Y7
NC	31		50	2Y7
GND	32		49	GND
A9	33		48	3Y7
NC	34		47	4Y7
V$_{CC}$	35		46	V$_{CC}$
4Y9	36		45	1Y8
3Y9	37		44	2Y8
GND	38		43	GND
2Y9	39		42	3Y8
1Y9	40		41	4Y8

(Top view)

HITACHI

3

HD74ALVC16831

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	–0.5 to 4.6	V	
Input voltage [1]	V_I	–0.5 to 4.6	V	
Output voltage [1, 2]	V_O	–0.5 to V_{CC} +0.5	V	
Input clamp current	I_{IK}	–50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{CC}
V_{CC}, GND current / pin	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) [3]	P_T	1	W	TVSOP
Storage temperature	T_{stg}	–65 to 150	°C	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	–12	mA	$V_{CC} = 2.3$ V
		—	–12		$V_{CC} = 2.7$ V
		—	–24		$V_{CC} = 3.0$ V
Low level output current	I_{OL}	—	12	mA	$V_{CC} = 2.3$ V
		—	12		$V_{CC} = 2.7$ V
		—	24		$V_{CC} = 3.0$ V
Input transition rise or fall rate	Æt / Æv	0	10	ns / V	
Operating temperature	T_a	–40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

HITACHI

Logic Diagram

To eight other channels
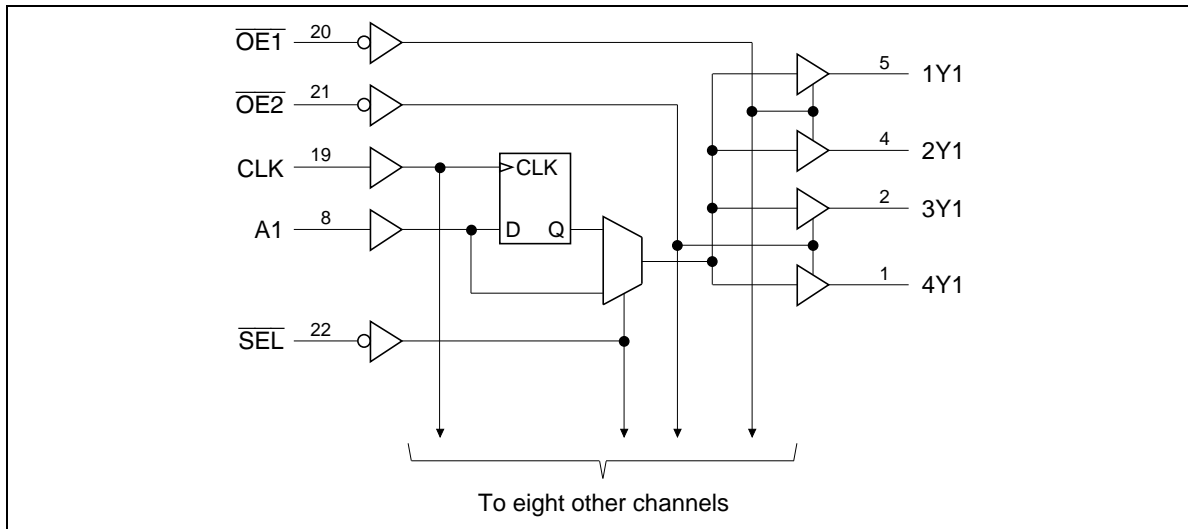
HD74ALVC16831

Electrical Characteristics (Ta = –40 to 85°C)

| Item	Symbol	V_{cc}(V)	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V_{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V_{OH}	2.3 to 3.6	V_{CC}–0.2	—	V	I_{OH} = −100 μA
		2.3	2.0	—		I_{OH} = –6 mA, V_{IH} = 1.7 V
		2.3	1.7	—		I_{OH} = –12 mA, V_{IH} = 1.7 V
		2.7	2.2	—		I_{OH} = –12 mA, V_{IH} = 2.0 V
		3.0	2.4	—		I_{OH} = –12 mA, V_{IH} = 2.0 V
		3.0	2.0	—		I_{OH} = –24 mA, V_{IH} = 2.0 V
	V_{OL}	2.3 to 3.6	—	0.2		I_{OL} = 100 μA
		2.3	—	0.4		I_{OL} = 6 mA, V_{IL} = 0.7 V
		2.3	—	0.7		I_{OL} = 12 mA, V_{IL} = 0.7 V
		2.7	—	0.4		I_{OL} = 12 mA, V_{IL} = 0.8 V
		3.0	—	0.55		I_{OL} = 24 mA, V_{IL} = 0.8 V
Input current	I_{IN}	3.6	—	±5	μA	V_{IN} = V_{CC} or GND
Off state output current	I_{OZ}	3.6	—	±10	μA	V_{OUT} = V_{CC} or GND
Quiescent supply current	I_{CC}	3.6	—	40	μA	V_{IN} = V_{CC} or GND
	ΔI_{CC}	3.0 to 3.6	—	750	μA	V_{IN} = one input at (V_{CC}–0.6) V, other inputs at V_{CC} or GND

Note: 1. This is the bus hold maximum dynamic current required to switch the input from one state to another.

HITACHI

Switching Characteristics (Ta = –40 to 85°C)

Item	Symbol	V_{cc} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f_{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t_{PLH}	2.5±0.2	1.7	—	4.6	ns	A	Y
	t_{PHL}	2.7	—	—	4.1			
		3.3±0.3	1.6	—	3.6			
		2.5±0.2	1.6	—	5.1		CLK	Y
		2.7	—	—	4.4			
		3.3±0.3	1.5	—	3.9			
		2.5±0.2	1.8	—	5.8		$\overline{SEL}$	Y
		2.7	—	—	5.2			
		3.3±0.3	1.7	—	4.4			
Output enable time	t_{ZH}	2.5±0.2	1.2	—	5.6	ns	$\overline{OE}$	Y
	t_{ZL}	2.7	—	—	5.0			
		3.3±0.3	1.2	—	4.3			
Output disable time	t_{HZ}	2.5±0.2	2.1	—	5.7	ns	$\overline{OE}$	Y
	t_{LZ}	2.7	—	—	4.7			
		3.3±0.3	1.6	—	4.5			
Setup time	t_{su}	2.5±0.2	2.0	—	—	ns		
		2.7	2.0	—	—			
		3.3±0.3	1.6	—	—			
Hold time	t_{h}	2.5±0.2	0.7	—	—	ns		
		2.7	0.5	—	—			
		3.3±0.3	1.1	—	—			
Pulse width	t_{w}	2.5±0.2	3.3	—	—	ns		
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
Input capacitance	C_{IN}	3.3	—	4.5	—	pF	Control inputs	
		3.3	—	5.0	—		Data inputs	
Output capacitance	C_{O}	3.3	—	7.5	—	pF		

HITACHI

7
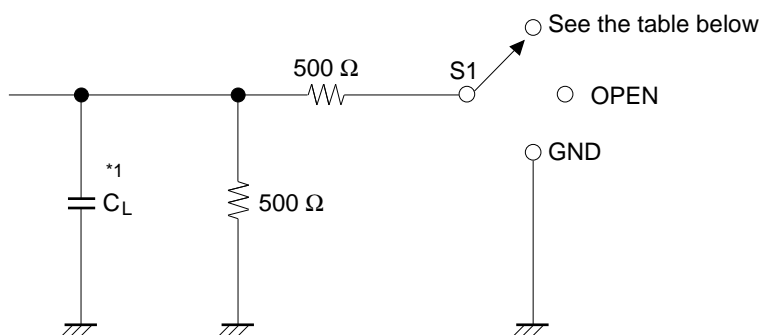
Test Circuit

Load Circuit for Outputs

Symbol	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
t_{PLH} / t_{PHL} t_{su} / t_h / t_w	OPEN	OPEN
t_{ZH} / t_{HZ}	GND	GND
t_{ZL} / t_{LZ}	$2 \times V_{CC}$	6.0 V
C_L	30 pF	50 pF

Note: 1. C_L includes probe and jig capacitance.

HITACHI
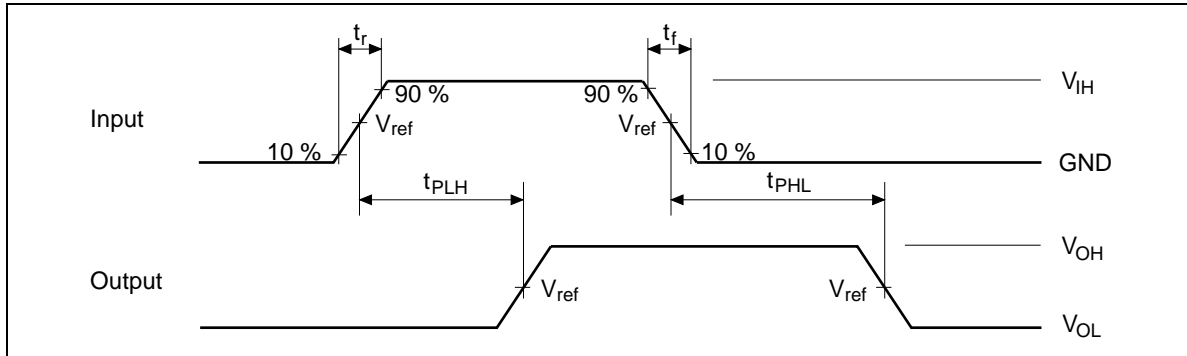
Waveforms – 1

Waveforms – 2
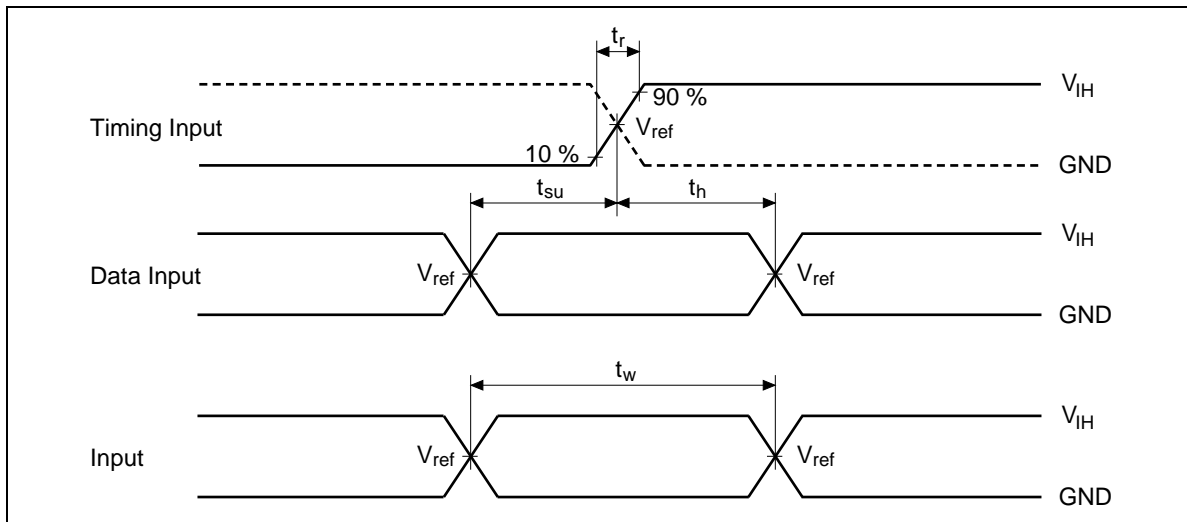
Waveforms – 3
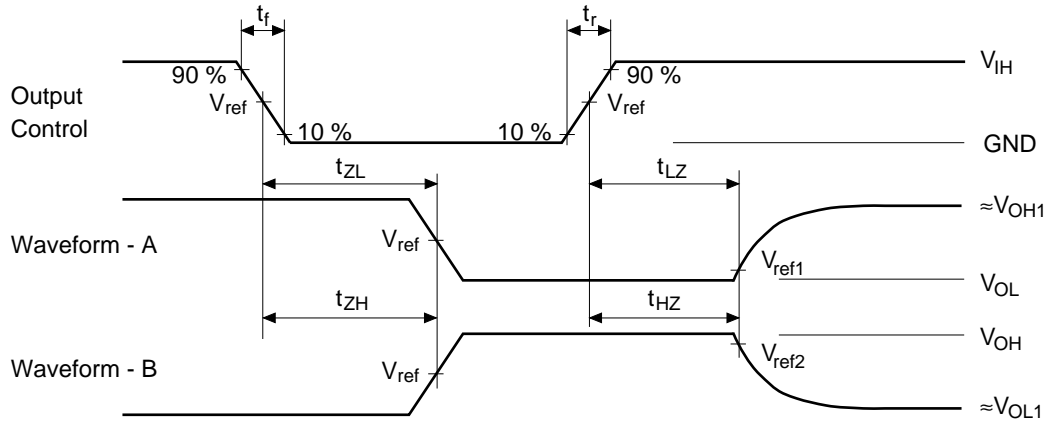
TEST	Vcc=2.5±0.2V	Vcc=2.7V, 3.3±0.3V
V_{IH}	V_{CC}	2.7 V
V_{ref}	1/2 V_{CC}	1.5 V
V_{ref1}	V_{OL} +0.15 V	V_{OL} +0.3 V
V_{ref2}	V_{OH}−0.15 V	V_{OH}−0.3 V
V_{OH1}	V_{CC}	3.0 V
V_{OL1}	GND	GND

Notes: 1.   All input pulses are supplied by generators having the following characteristics :
PRR ≤ 10 MHz, Zo = 50 Ω, t_r ≤ 2.0 ns, t_f ≤ 2.0 ns. (V_{cc} = 2.5±0.2 V)
PRR ≤ 10 MHz, Zo = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns. (V_{cc} = 2.7 V, 3.3±0.3 V)

2.   Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.

3.   Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.

4.   The output are measured one at a time with one transition per measurement.

HITACHI

Package Dimensions

Unit : mm

Hitachi code	—
EIAJ code	—
JEDEC code	—
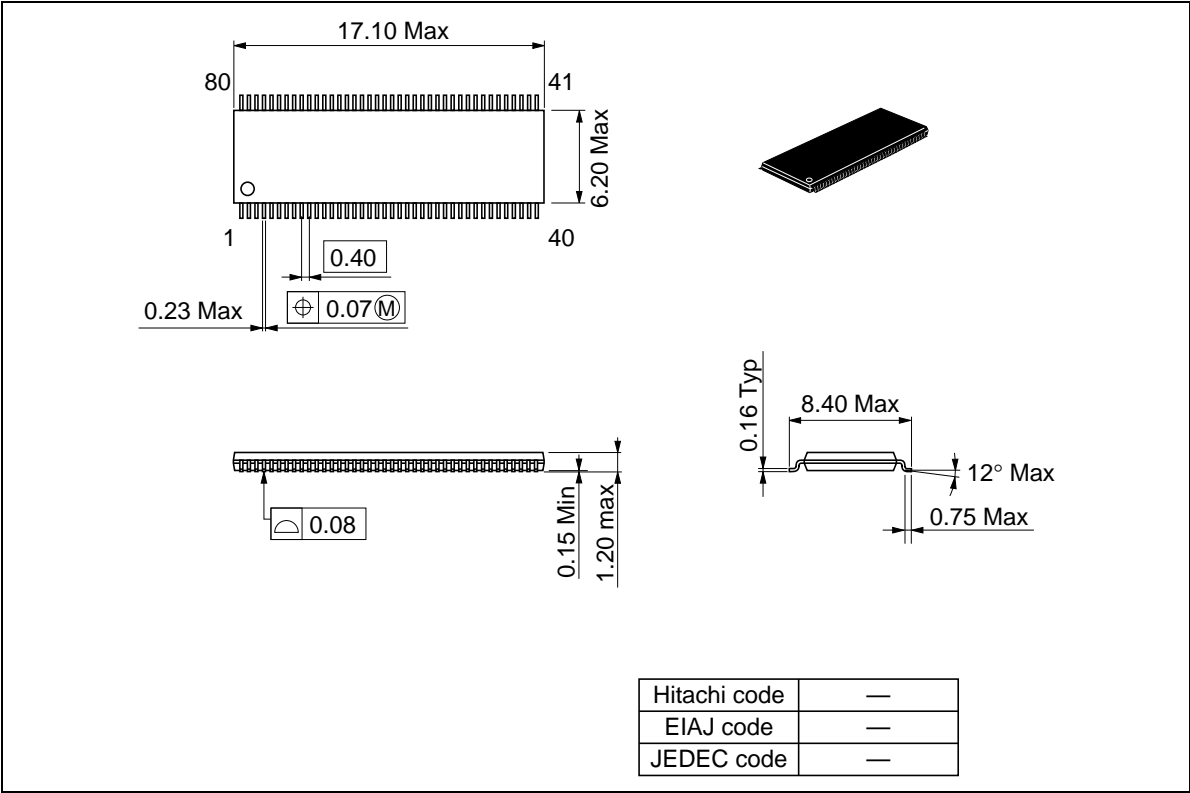
When using this document, keep the following in mind:

1. This document may, wholly or partially, be subject to change without notice.
2. All rights are reserved: No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without Hitachi's permission.
3. Hitachi will not be held responsible for any damage to the user that may result from accidents or any other reasons during operation of the user's unit according to this document.
4. Circuitry and other examples described herein are meant merely to indicate the characteristics and performance of Hitachi's semiconductor products. Hitachi assumes no responsibility for any intellectual property claims or other problems that may result from applications based on the examples described herein.
5. No license is granted by implication or otherwise under any patents or other rights of any third party or Hitachi, Ltd.
6. MEDICAL APPLICATIONS: Hitachi's products are not authorized for use in MEDICAL APPLICATIONS without the written consent of the appropriate officer of Hitachi's sales company. Such use includes, but is not limited to, use in life support systems. Buyers of Hitachi's products are requested to notify the relevant Hitachi sales offices when planning to use the products in MEDICAL APPLICATIONS.

HITACHI