Helium 210-80 Communications Processor

Virata
Product Profile

September 2001

KEY FEATURES

- **ATM switching and Layer 2/3 processing device**
- **USB for external modem applications**
- **Ethernet 10/100 BaseT for router applications**
- **Utopia 1/2 for interface to external PHYs**
- **Dual ARM RISC processor architecture**

Product Applications

- DSL Modem
- DSL Gateway/Router
- DSL/ATM Line Cards
- ATM Access
- ATM CSU/DSU
- Bridging/Routing

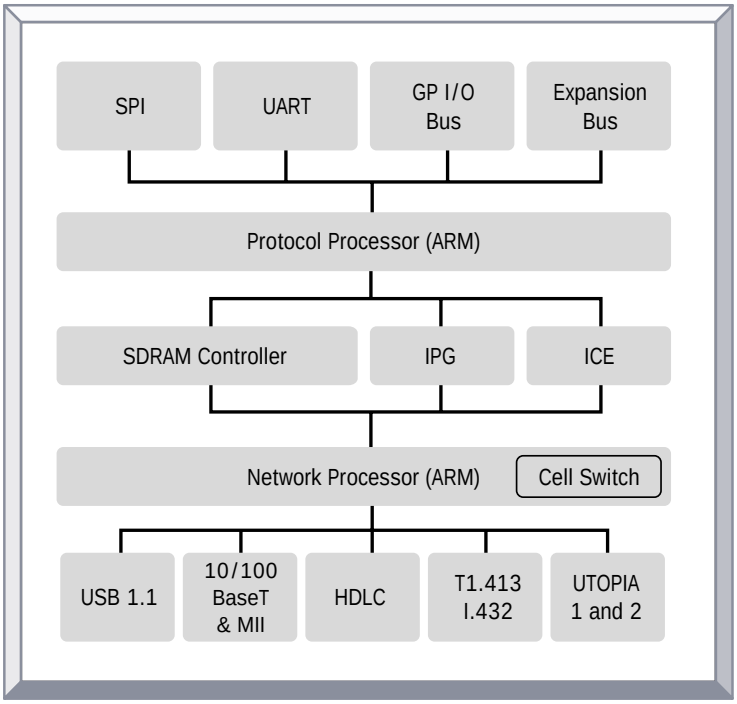
Application

The Helium™ 210-80 is a single-chip communications processor, performing ATM switching and Layer 2/3 processing. A general purpose RISC Protocol Processor runs higher layer protocols, while a higher performance microcoded RISC Network Processor is used for cell and frame handling, switching traffic at up to 120 Mbps.

Integrating many common interface functions, Helium 210-80 is designed for flexible, low-cost, high-functionality, high-performance products. It may be used in a DSL router/gateway, ATM access device, or USB modem customer premises equipment (CPE) or central office (CO) equipment.

Helium 210-80 contains a Network Processor that controls the direct connections to Ethernet and USB, physical interfaces for Utopia 1 and 2, HDLC and I.432 Framer.

The Network Processor has 16K of microcode RAM and a high-speed interface to external SDRAM. This supports both ATM cells and packets, OAM cell handling, policing, shaping and accounting. The two processors communicate via the inter-processor gateway IPG.



Helium 210-80 System Interfaces

Helium 210-80 extends Virata's ATOM architecture and runs the complete suite of Virata networking software including support for routing, bridging, signaling, and SNMP Management.

Software flexibility, high-integration and built-in hardware debugging (ICE) support allow rapid product development.

This combination of hardware and software, Integrated Software on Silicon™ (ISOS™), provides a unique time to market advantage.

Reference Platform

The BD6220 is the development platform for Virata's Helium 210-80 ASSP, providing a wealth of hardware and software debug tools to assist partners in rapid development and deployment of their products. Training, documentation and support are also available.

Specifications

Processors

- Protocol Processor (PP) is an ARM7TDMI RISC core that includes a 8K cache providing:
  - Modem PHY Management (depending on application)
  - Initialization code
  - Soft real-time tasks
- Network Processor (NP) is an ARM7TDMI RISC core with 16K of SRAM performing:
  - Data Transfer
    - Framing
    - Interleaving
    - CRC Generation
    - Switching
  - Hard real-time tasks

USB

USB 1.1 slave interface — up to 12 Mbps using Control, Interrupt, Bulk, and Isochronous endpoints and transfers.

10/100 BaseT Ethernet

Helium 210-80 contains a 10/100 Ethernet MAC with a low power integrated PHY. The MII signals from the MAC are also available.

Utopia

Utopia 1 and 2 (master/slave) interfaces with 31 ports, configuration:

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Product Profile

Interfaces

- USB 1.1
- 10/100 BaseT Ethernet
- Utopia 1/2
- HDLC/I.432
- GPIO
- Expansion Bus
- UART
- SDRAM
- Flash PROM
- EEPROM
- PCMCIA (Master)

- 8 ports dual-latency, or
- 2 ports dual-latency and 29 ports single latency
- 2 ports dual-latency and 12 ports single latency

I.432 Framer

Helium 210-80 implements all the framing requirements I.432 of T1.413, allowing full duplex data interface to external ADSL PHY.

HDLC

The HDLC interface uses the same pins as the I.432 Framer. The HDLC interface conforms to Q.921 at a frame rate of 25MHz with 16-bit CRC generation.

SDRAM

SDRAM interface conforms to JEDEC requirements, supporting 2 to 32 Mbytes of address space with a selectable 16 or 32 bit data bus.

GPIO

The General Purpose I/O bus contains 28 pins. Of these pins, two are used for the UART serial interface (Tx and Rx at a speed of 38,462 baud) and three for the serial boot EEPROM. Five pins can also be configured as Ethernet status indicators. Seven pins are used to support the PCMCIA mode of the expansion bus.

Expansion Bus

The expansion bus can support 8-bit Motorola, 16-bit Intel or 16-bit multiplexed modes. Helium 210-80 also has extended modes supporting i960 and PCMCIA-master. The expansion bus is also used to control external devices and boot Helium 210-80 from memory, typically Flash PROM. Up to 4 devices are supported using 4 pins as programmable chip selects – more with additional decoder.

Boot Options

- USB interface
- UART
- Flash PROM
- Ethernet Network Boot
- Serial EPROM

Software

Helium 210-80's Protocol Processor runs Virata's extensive networking software suite, including:

- OS Kernel and C/C++ Library (either ATMOS™ or VxWorks)
- Non-zero VPI support
- OAM I.610 full implementation
- SNMP v1, v2, and v3
- Flash-FS and In Store-FS
- USB drivers for Windows® 98, ME and 2000
- QOS: UBR, CBR, nrt-VBR , rt-VBR
- ATM Forum UNI 3.0, 3.1 and 4.0 Signaling
- ILMI 4.0
- SSCOP and AAL-2 CPCS
- Bridge-mode RFC1483 PVC and SVC
- PPP over ATM PVC (RFC 2364)
- Classical IP - RFC1577, RFC1483, RFC1755
- Classical IP ARP server
- MAC-layer Bridge (Spanning Tree 802.1d)
- ATM Forum LEC
- TCP/IP Stack
- IP Router - RIP1, RIP2
- TFTP Client and Server
- PPTP and L2TP
- DHCP Client, Server, and Relay
- NAT with extensive ALG
- DNS Relay and Client
- PPPoE Client and Relay Agent
- FRF.12 Frame Relay fragmentation
- LMI for Frame Relay PVC link management

See latest ISOS datasheet for full list of software features.

Package

272 PBGA

Environmental

80 MHz clock
Core Supply 1.8V, +/- 10%
I/O Supply 3.3V, +/- 10%
Temperature range 0 C to +70 C

Ordering Information

VC-45210-PBC80
The development system for Helium 210-80 is the BD6220. Databook available upon request.
DO-008538-PS

H2180_P0901v4

For more information, please contact us:

E-mail: info@virata.com
Web site: www.virata.com

VIRATA, USA
Corporate Headquarters
2700 San Tomas Expressway
Santa Clara, CA 95051
USA
Tel. 408-566-1000
Fax 408-566-1194

VIRATA, UK
230 Cambridge Science Park
Milton Road
Cambridge CB4 0WB
United Kingdom
Tel. +44-1223-707400
Fax +44-1223-707447

VIRATA, Taiwan
17F-2 No.77 Hsin Tai Wu Road
Sec. 1
Hsichih, Taipei County
Taiwan
Tel. +886-2-2698-3500
Fax +886-2-2698-3566

VIRATA, Israel
11 Shenkar Street
Herzelia Pituach 46725
Israel
Tel. +972-9-9717-400
Fax +972-9-9717-444