

GaAS MMIC LOW DISTORTION DIVERSITY SWITCH DC - 2.0 GHZ

SEPTEMBER 1999

Features

HIGH THIRD ORDER INTERCEPT: +54 dBm

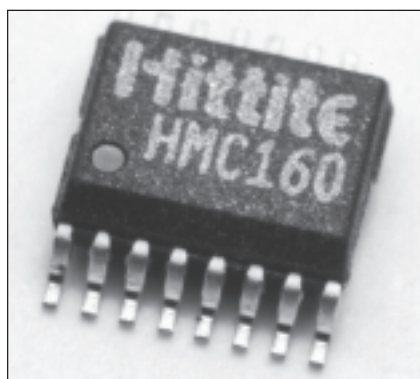
SINGLE POSITIVE SUPPLY: +3 TO +8V

HIGH POWER CAPABILITY

TTL/CMOS CONTROL

General Description

The HMC160QS16 is a low-cost diversity switch in a 16-lead QSOP package for use in transmit-receive applications which require very low distortion at high signal power levels. The device can control signals up to 2.0GHz and is especially suited for 900MHz and 1500 MHz applications. The switch is used to exchange two antennae between transmitter and two receivers, providing system diversity. The design has exceptional intermodulation performance; providing a +54 dBm third order intercept at 8 Volt bias. On-chip circuitry allows single positive supply operation at very low DC current with control inputs compatible with CMOS and most TTL logic families. The QSOP 16-lead package occupies the same area as an 8-lead SOIC.



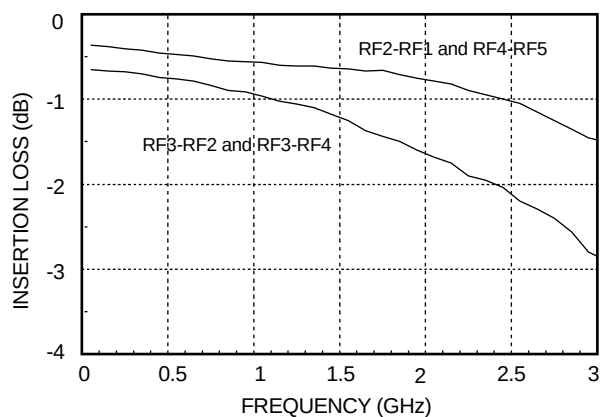
Guaranteed Performance, $V_{dd} = +5 V_{dc}$, 50 Ohm System, -40 to +85 deg C

Parameter	Path	Frequency	Min.	Typ.	Max.	Units
Insertion Loss	RF2-RF1, RF4-RF5	DC - 1.0GHz		0.5	0.8	dB
		DC - 1.5GHz		0.7	1.0	dB
		DC - 2.0GHz		0.8	1.1	dB
	RF3-RF2, RF3-RF4	DC - 1.0GHz		0.9	1.2	dB
		DC - 1.5GHz		1.2	1.5	dB
		DC - 2.0GHz		1.7	2.0	dB
Isolation	ALL	DC - 1.0GHz	21	24		dB
		DC - 1.5GHz	21	24		dB
		DC - 2.0GHz	19	22		dB
Return Loss	RF2-RF1, RF4-RF5	DC - 1.0GHz	24	28		dB
		DC - 1.5GHz	18	22		dB
		DC - 2.0GHz	14	17		dB
	RF3-RF2, RF3-RF4	DC - 1.0GHz	14	17		dB
		DC - 1.5GHz	11	14		dB
		DC - 2.0GHz	8.0	11		dB
Input Power for 1dB Compression 0/8V Ctl	ALL	0.5 - 1.0GHz	33	35		dBm
		0.5 - 2.0GHz	31	33		dBm
Input Third Order Intercept 0/8V Ctl	ALL	0.5 - 1.0GHz	50	55		dBm
		0.5 - 2.0GHz	47	54		dBm
Switching Characteristics	ALL	DC - 2.0GHz		22		ns
				50		ns

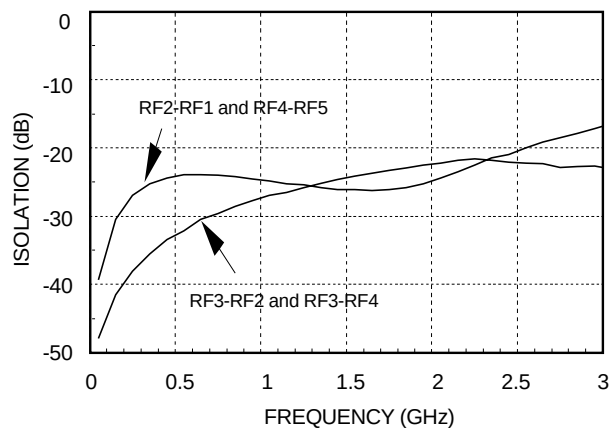
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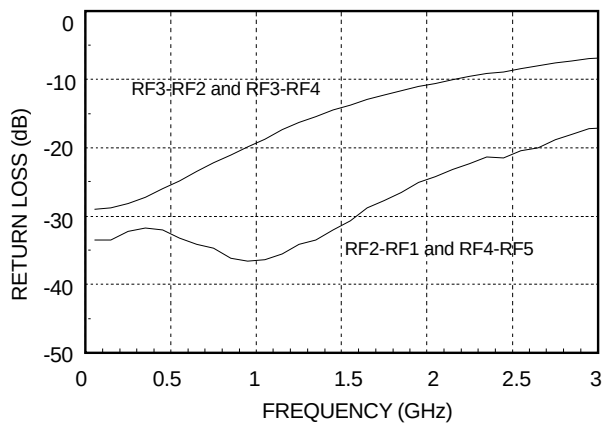
Insertion Loss



Isolation



Return Loss

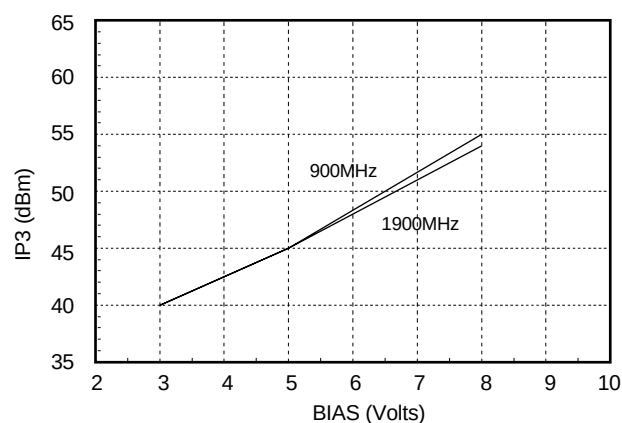


S - Parameter data is available On-Line at www.hittite.com

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Input 0.1 and 1.0 dB Compression vs Bias Voltage



Input Third Order Intercept vs Bias Voltage

Bias	1 Watt Carrier at 900MHz			1 Watt Carrier at 1900MHz		
	Third Order Intercept	Second Order Intercept	Second Harmonic	Third Order Intercept	Second Order Intercept	Second Harmonic
(Volts)	(dBm)	(dBm)	(dBc)	(dBm)	(dBm)	(dBc)
3	40	68	43	40	81	56
5	45	77	51	45	90	62
8	55	84	60	54	90	66

Compression vs Bias Voltage RF1 - RF2 and RF4 - RF5

RF Path RF1-RF2 and RF4-RF5				
Bias	Carrier at 900MHz		Carrier at 1900MHz	
	Input Power for 0.1dB Compression	Input Power for 1dB Compression	Input Power for 0.1dB Compression	Input Power for 1dB Compression
(Volts)	(dBm)	(dBm)	(dBm)	(dBm)
3	25	29	24	28
5	29	34	28	32
8	32	36	31	35

Compression vs Bias Voltage RF2 - RF3 and RF3 - RF4

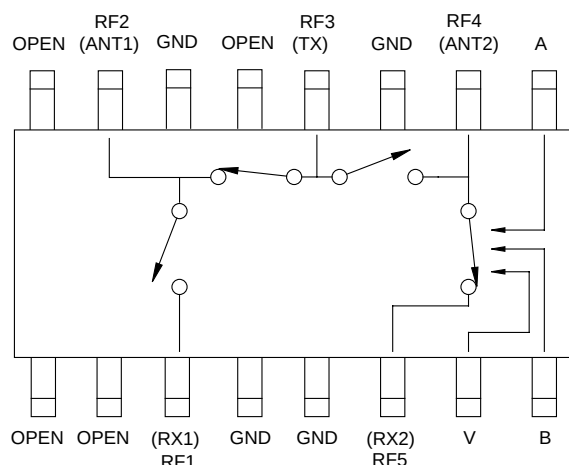
RF Path RF2-RF3 and RF3-RF4				
Bias	Carrier at 900MHz		Carrier at 1900MHz	
	Input Power for 0.1dB Compression	Input Power for 1dB Compression	Input Power for 0.1dB Compression	Input Power for 1dB Compression
(Volts)	(dBm)	(dBm)	(dBm)	(dBm)
3	24	28	23	27
5	28	33	27	31
8	31	35	30	33

Caution: Do not operate in 1dB compression at power levels above +35dBm and do not "Hot Switch" power levels greater than +23 dBm with a +5 Vdc bias.

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Functional Diagram



Absolute Maximum Ratings

Bias Voltage Range (Vdd)	-0.2 to +12 Vdc
Control Voltage Range (A & B)	-0.2 to +Vdd Vdc
Storage Temperature	-65 to +150 deg C
Operating Temperature	-40 to +85 deg C

Truth Table

Control Input		Signal Path State			
A	B	RF1-RF2	RF2-RF3	RF3-RF4	RF4-RF5
Low	High	ON	OFF	ON	OFF
High	Low	OFF	ON	OFF	ON

Control Voltage

State	Bias Condition
Low	0 to -0.2V @ 20uA Max.
High	+3V@50uA Typ to +8V@500uA Max

Logic High control voltage must be in the range of $V-0.2$ to V where V is the applied bias voltage. Recommended bias voltage V is +3 to +8 Volts.

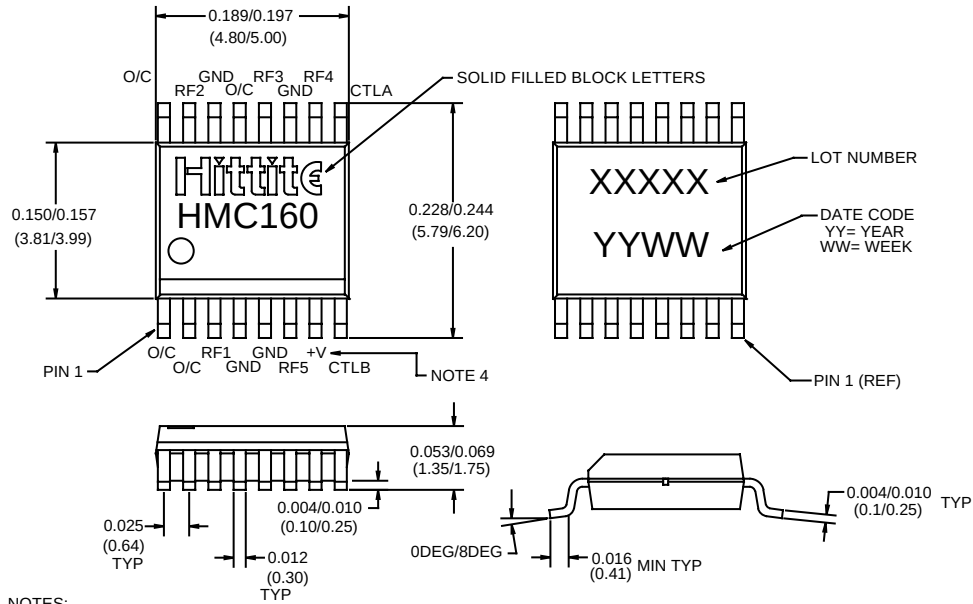
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Switches

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Outline



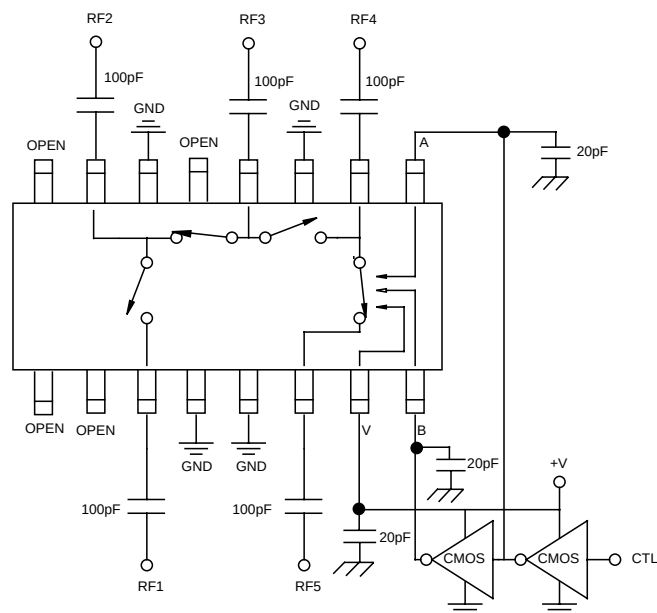
NOTES:

- 1) MATERIAL:
 - A) PACKAGE BODY LOW STRESS INJECTION MOLDED PLASTIC, SILICA & SILICONE IMPREGNATED
 - B) LEADFRAME MATERIAL: COPPER ALLOY
2. PLATING: LEAD-TIN SOLDER PLATE
3. DIMENSIONS ARE IN INCHES (MILLIMETERS) UNLESS OTHERWISE SPECIFIED TOL. ARE ± 0.005 (± 0.13)

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Typical Application Circuit



Notes:

1. Control inputs A and B can be driven directly with CMOS logic (HC) with V of 3 to 8 Volts applied to the CMOS logic gates and to pin V of the RF switch.
2. DC Blocking capacitors are required for each RF port as shown. Capacitor value determines lowest frequency of operation. 20 pF decoupling caps are recommended on pins V, A, and B.
3. Highest RF signal power capability is achieved with V set to +8V. However, the switch will operate properly (but at lower RF power capability) at bias voltages down to +3V.
4. Set V to 5 Volts and use HCT series logic to provide a TTL driver interface.