HD74LS194A ●4-bit Bidirectional Universal Shift Registers

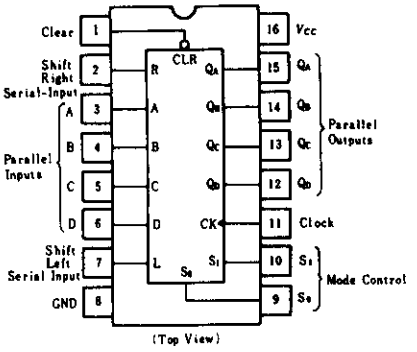
This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs. Operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in direction Q_D toward Q_A)
Inhibit clock (do nothing)

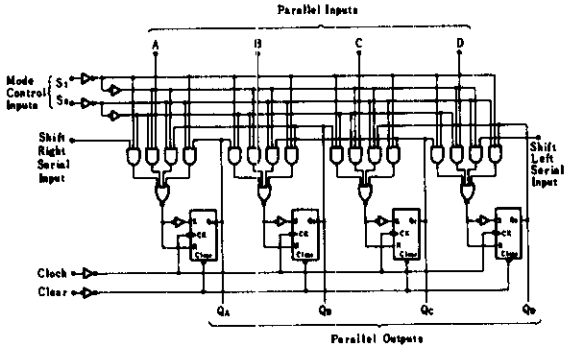
Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low.

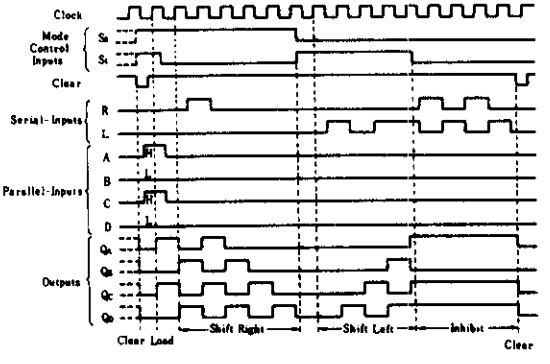
■PIN ARRANGEMENT



■BLOCK DIAGRAM



■COUNT SEQUENCE



■FUNCTION TABLE

CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Outputs			
	S1	S0		LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	×	×	×	×	×	×	×	×	×	L	L	L	L
H	×	×	L	×	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	×	×	a	b	c	d	a	b	c	d
H	L	H	↑	×	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	×	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	×	×	×	×	×	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	×	×	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. ↓; transition from high to low level
4. a~d; the level of steady-state input at inputs A,B,C, or D, respectively
5. Q_{A0}~Q_{D0}; the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
6. Q_{An}~Q_{Dn}; the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↑ transition of the clock.

■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Clock frequency		f_{clock}	0	–	25	MHz
Clock pulse width		$t_{w(CK)}$	20	–	–	ns
Clear pulse width		$t_{w(CLR)}$	20	–	–	ns
Setup time	Mode Control	t_{su}	30	–	–	ns
	A, B, C, D, R, L		20	–	–	ns
	CLR (inactive state)		25	–	–	ns
Hold time		t_h	0	–	–	ns

■ELECTRICAL CHARACTERISTICS ($Ta=-20\sim+75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
			$I_{OL}=8mA$	–	–	0.5	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$		–	15	23	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* V_{CC}=5V, Ta=25°C

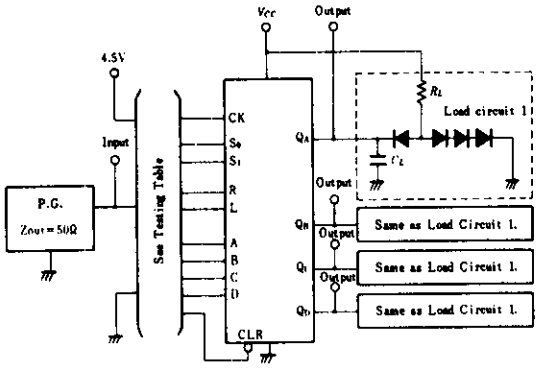
** With all outputs open, inputs A through D grounded, and 4.5V applied to S_0, S_1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5V, applied to clock.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$ $R_L=2k\Omega$	25	36	–	MHz
Propagation delay time	t_{PHL}	Clear	Q		–	19	30	ns
	t_{PLH}	Clock			–	14	22	ns
	t_{PHL}	Clock			–	17	26	ns

■TESTING METHOD

1) Test Circuit

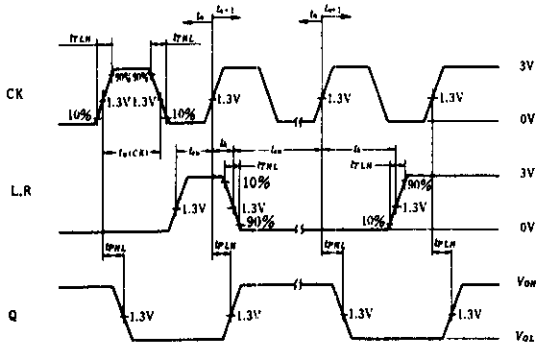


Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 Ⓗ.

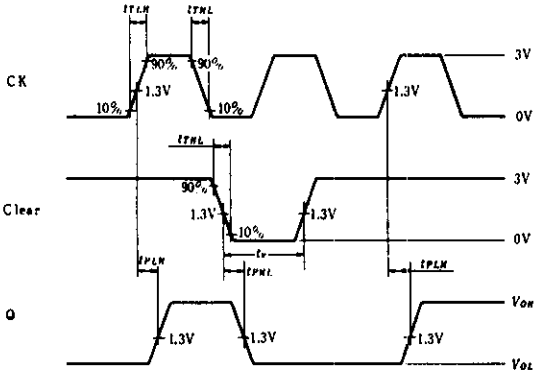
2) Testing Table

Item	From input to output	Inputs										Outputs			
		CLR	S_1	S_0	CK	L	R	A	B	C	D	Q_A	Q_B	Q_C	Q_D
f_{max}	right-shift	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT
	left-shift	4.5V	GND	4.5V	IN	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT
t_{PHL} t_{PLH}	Clear→Q	IN	4.5V	4.5V	IN	GND	GND	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT
	Clock→Q	4.5V	4.5V	GND	IN	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT
		4.5V	4.5V	GND	IN	IN	4.5V	GND	GND	GND	GND	OUT	OUT	OUT	OUT

Waveform—1 (f_{max}, CK→Q)



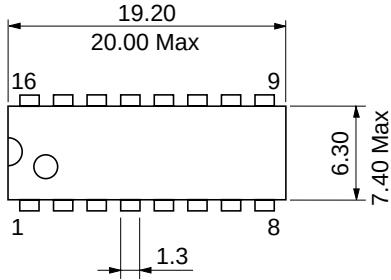
Waveform—2 (Clear→Q)

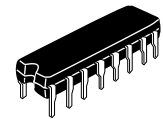


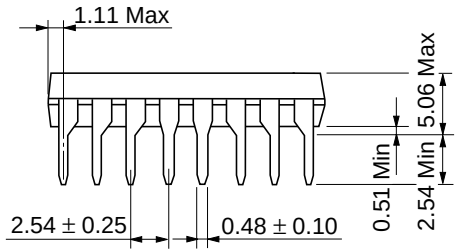
Notes) 1. Right-shift is measured with Q_A at t_{n+1}, Q_B at t_{n+2}, Q_C at t_{n+3}, and Q_D at t_{n+4}. Left-shift is measured with Q_A at t_{n+4}, Q_B at t_{n+3}, Q_C at t_{n+2}, and Q_D at t_{n+1}.

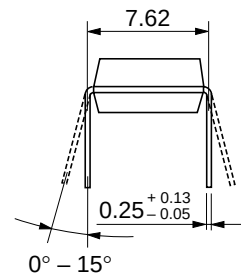
Input pulse: $t_{TLH} \leqq 15ns$, $t_{THL} \leqq 6ns$

Unit: mm



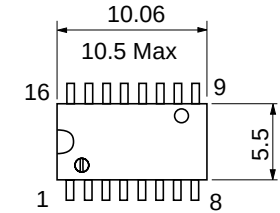


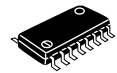


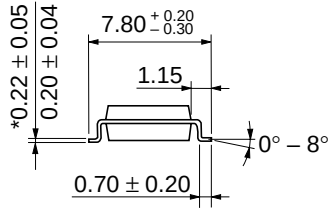


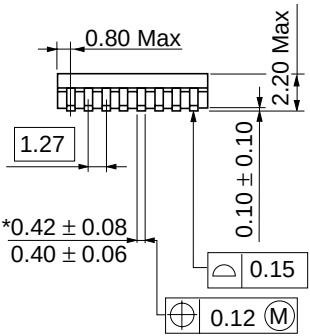
Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm









*Dimension including the plating thickness
Base material dimension

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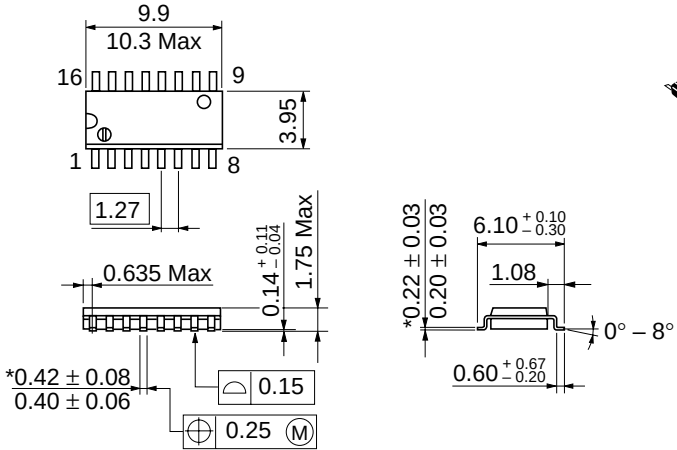
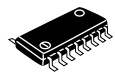
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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