
HD74ACT161/HD74ACT163

Synchronous Presetable Binary Counter

HITACHI

ADE-205-402 (Z)
1st. Edition
Sep. 2000

Description

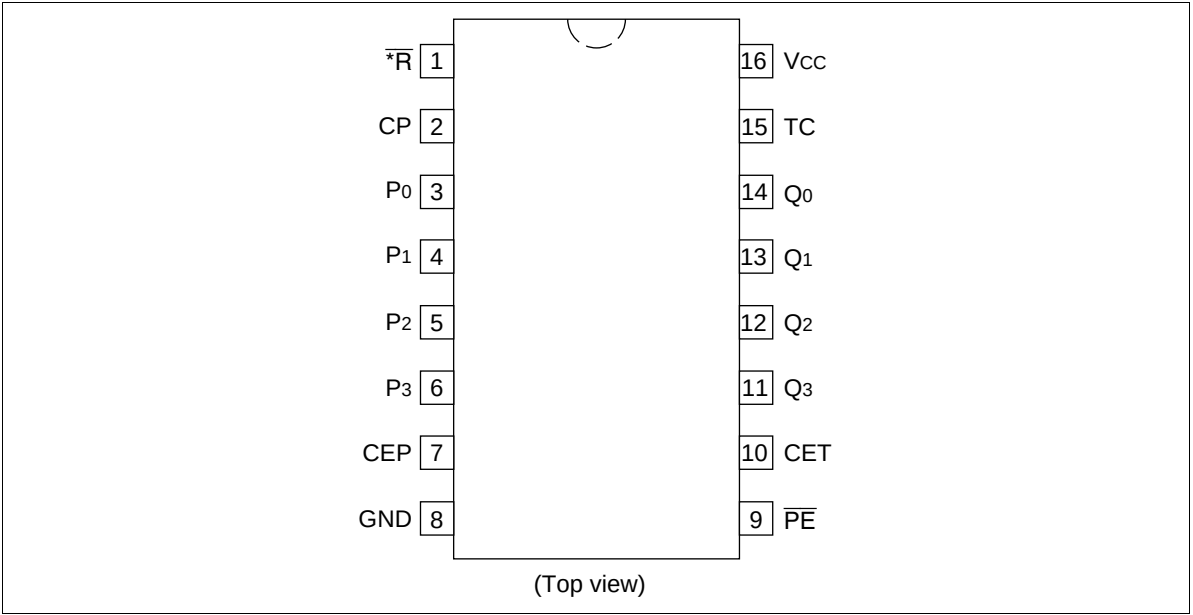
The HD74ACT161 and HD74ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presetable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The HD74ACT161 have an asynchronous Master Reset input that overrides all other inputs and forces the outputs Low. The HD74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

Features

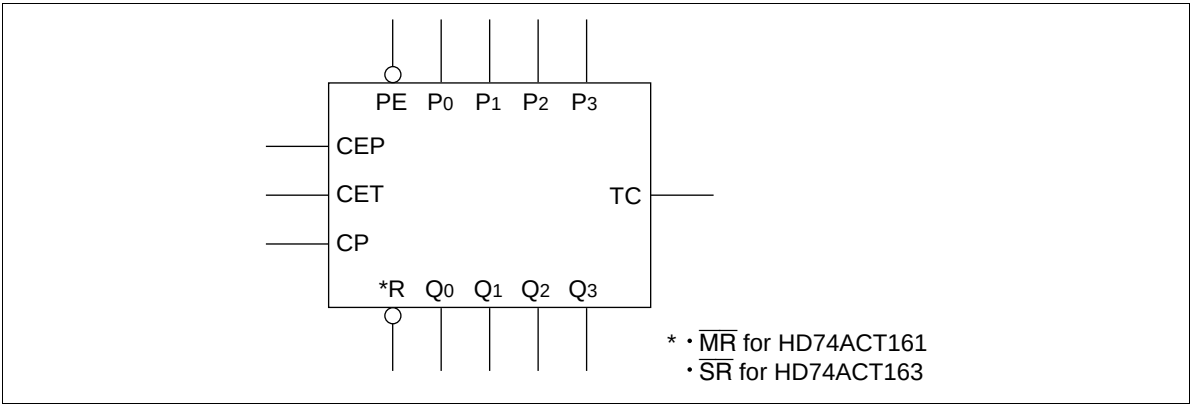
- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- HD74ACT161 and HD74ACT163 have TTL-Compatible Inputs

HD74ACT161/HD74ACT163

Pin Arrangement



Logic Symbol



Pin Names

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{\text{MR}}$ (HD74ACT161)	Asynchronous Master Reset Input
$\overline{\text{SR}}$ (HD74ACT163)	Synchronous Reset Input
P ₀ to P ₃	Parallel Data Inputs
$\overline{\text{PE}}$	Parallel Enable Input
Q ₀ to Q ₃	Flip-Flop Outputs
TC	Terminal Count Output

Functional Description

The HD74ACT161 and HD74ACT163 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the HD74ACT161) occur as a reset of, and synchronous with, the Low-to-High transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (HD74ACT161), synchronous reset (HD74ACT163), parallel load, countup and hold. Five control inputs – Master Reset ($\overline{\text{MR}}$, HD74ACT161), Synchronous Reset ($\overline{\text{SR}}$, HD74ACT163), Parallel Enable ($\overline{\text{PE}}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) – determine the mode of operation, as shown in the Mode Select Table. A Low signal on $\overline{\text{MR}}$ overrides all other inputs and asynchronously forces all outputs Low. A Low signal on $\overline{\text{SR}}$ overrides counting and parallel loading and allows all outputs to go Low on the next rising edge of CP. A Low signal on $\overline{\text{PE}}$ overrides counting and allows information on the Parallel Data (Pn) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{\text{PE}}$ and $\overline{\text{MR}}$ (HD74ACT161) or $\overline{\text{SR}}$ (HD74ACT163) High, CEP and CET permit counting when both are High. Conversely, a Low signal on either CEP or CET inhibits counting.

The HD74ACT161 and HD74ACT163 use D-type edge-triggered flip-flops and changing the $\overline{\text{SR}}$, $\overline{\text{PE}}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed. The Terminal Count (TC) output is High when CET is High and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP • CET • $\overline{\text{PE}}$

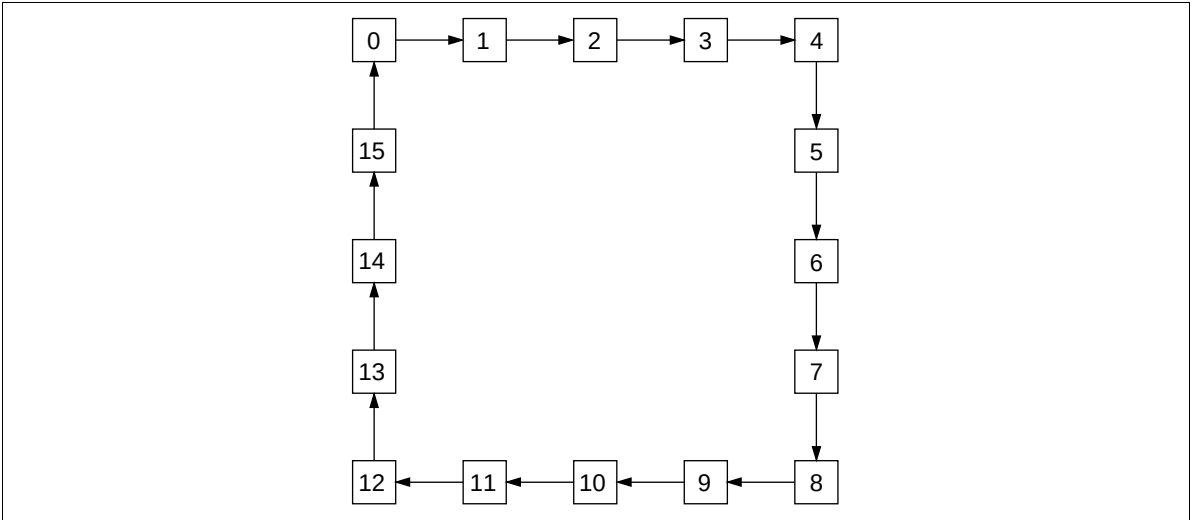
$$\text{TC} = \text{Q}_0 \cdot \text{Q}_1 \cdot \text{Q}_2 \cdot \text{Q}_3 \cdot \text{CET}$$

Mode Select Table

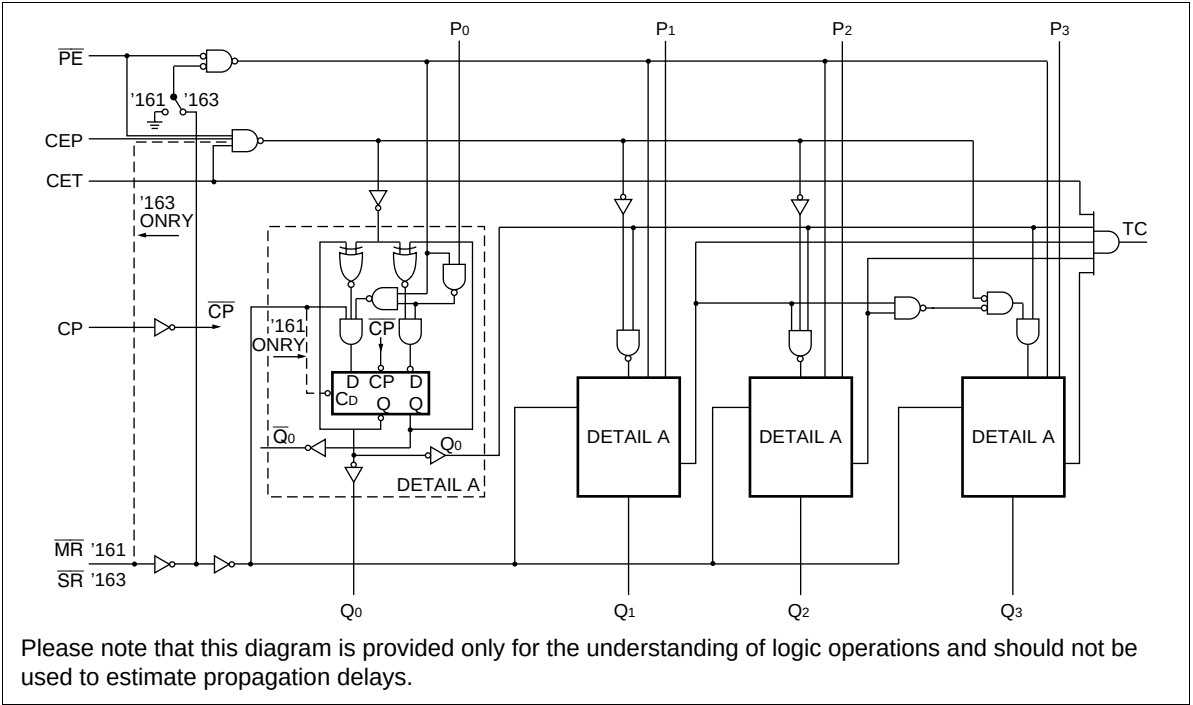
$\overline{SR}^{*1}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge ($\uparrow$)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No change (Hold)
H	H	X	L	No change (Hold)

Note: 1. For HD74ACT163
H : High Voltage Level
L : Low Voltage Level
X : Immaterial

State Diagram



Block Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^{\circ}C$
Maximum additional I_{CC}/input (HD74ACT161/HD74ACT163)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$

HD74ACT161/HD74ACT163

AC Characteristics: HD74ACT161

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = −40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum count frequency	f _{max}	5.0	115	125	—	100	—	MHz
Propagation delay CP to Q _n (PE Input HIGH or LOW)	t _{PLH}	5.0	1.0	5.5	9.5	1.0	10.5	ns
Propagation delay CP to Q _n (PE Input HIGH or LOW)	t _{PLH}	5.0	1.0	6.0	10.5	1.0	11.5	ns
Propagation delay CP to TC	t _{PLH}	5.0	1.0	7.0	11.0	1.0	12.5	ns
Propagation delay CP to TC	t _{PHL}	5.0	1.0	8.0	12.5	1.0	13.5	ns
Propagation delay CET to TC	t _{PLH}	5.0	1.0	5.5	8.5	1.0	10.0	ns
Propagation delay CET to TC	t _{PHL}	5.0	1.0	6.0	9.5	1.0	10.5	ns
Propagation delay MR to Q _n	t _{PHL}	5.0	1.0	6.0	10.0	1.0	11.0	ns
Propagation delay MR to TC	t _{PHL}	5.0	1.0	8.0	13.5	1.0	14.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT161

Item	Symbol	V_{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = −40°C to +85°C C _L = 50 pF	
			Typ	Guaranteed Minimum		Unit
Set-up time, HIGH or LOW P _n to CP	t _{su}	5.0	4.0	9.5	11.5	ns
Hold time, HIGH or LOW P _n to CP	t _h	5.0	−5.0	0	0	ns
Setup time, HIGH or LOW MR to CP	t _{su}	5.0	4.0	8.5	9.5	ns
Hold time, HIGH or LOW MR to CP	t _h	5.0	−5.5	−0.5	−0.5	ns
Setup time, HIGH or LOW PE to CP	t _{su}	5.0	4.0	8.5	9.5	ns
Hold time, HIGH or LOW PE to CP	t _h	5.0	−5.5	−0.5	−0.5	ns
Setup time, HIGH or LOW CEP or CET to CP	t _{su}	5.0	2.5	5.5	6.5	ns
Hold time, HIGH or LOW CEP or CET to CP	t _h	5.0	−3.0	0	0	ns
Clock pulse width (Load) HIGH or LOW	t _w	5.0	2.0	3.0	3.5	ns
Clock pulse width (Count) HIGH or LOW	t _w	5.0	2.0	3.0	3.5	ns
MR pulse width, LOW	t _w	5.0	3.0	3.0	7.5	ns
Recovery time MR to CP	t _{rec}	5.0	0	0	0.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	45.0	pF	V _{CC} = 5.0 V

AC Characteristics: HD74ACT163

Item	Symbol	V _{CC} (V)* ¹	Ta = +25°C C _L = 50 pF			Ta = −40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum count frequency	f _{max}	5.0	120	128	—	105	—	MHz
Propagation delay CP to Q _n (PE Input HIGH or LOW)	t _{PLH}	5.0	1.0	5.5	10.0	1.0	11.0	ns
Propagation delay CP to Q _n (PE Input HIGH or LOW)	t _{PHL}	5.0	1.0	6.0	11.0	1.0	12.0	ns
Propagation delay CP to TC	t _{PLH}	5.0	1.0	7.0	11.5	1.0	13.5	ns
Propagation delay CP to TC	t _{PHL}	5.0	1.0	8.0	13.5	1.0	15.0	ns
Propagation delay CET to TC	t _{PLH}	5.0	1.0	5.5	9.0	1.0	10.5	ns
Propagation delay CET to TC	t _{PHL}	5.0	1.0	6.0	10.0	1.0	11.0	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT163

Item	Symbol	V _{cc} (V)*1	Ta = +25°C C _L = 50 pF	Ta = −40°C to +85°C C _L = 50 pF		Unit
			Typ	Guaranteed Minimum		
Set-up time, HIGH or LOW P _n to CP	t _{su}	5.0	4.0	10.0	12.0	ns
Hold time, HIGH or LOW P _n to CP	t _h	5.0	−5.0	0.5	0.5	ns
Setup time, HIGH or LOW SR to CP	t _{su}	5.0	4.0	10.0	11.5	ns
Hold time, HIGH or LOW SR to CP	t _h	5.0	−5.5	−0.5	−0.5	ns
Setup time, HIGH or LOW PE to CP	t _{su}	5.0	4.0	8.5	10.5	ns
Hold time, HIGH or LOW PE to CP	t _h	5.0	−5.5	−0.5	0	ns
Setup time, HIGH or LOW CEP or CET to CP	t _{su}	5.0	2.5	5.5	6.5	ns
Hold time, HIGH or LOW CEP or CET to CP	t _h	5.0	−3.0	0	0.5	ns
Clock pulse width (Load) HIGH or LOW	t _w	5.0	2.0	3.5	3.5	ns
Clock pulse width (Count) HIGH or LOW	t _w	5.0	2.0	3.5	3.5	ns

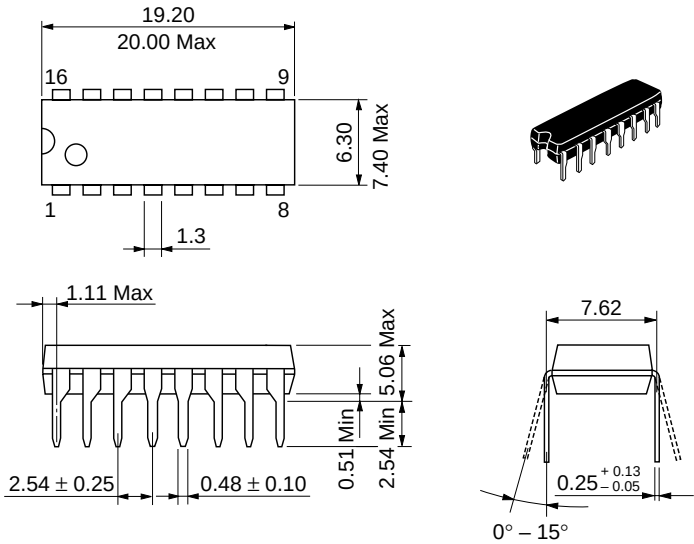
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	45.0	pF	V _{CC} = 5.0 V

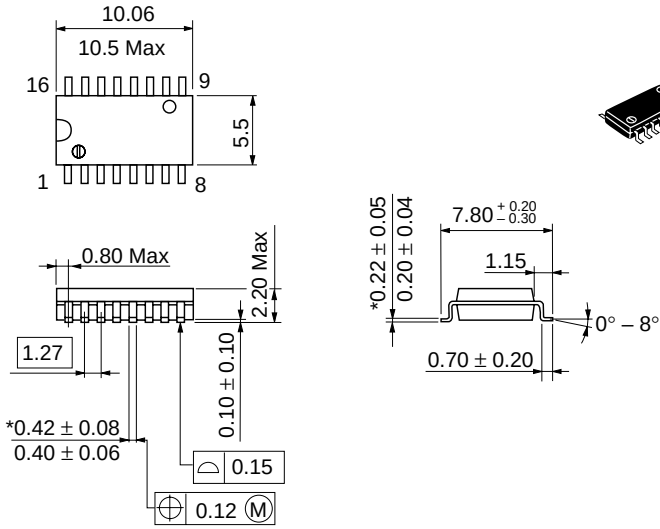
Package Dimensions

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	1.07 g

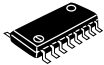
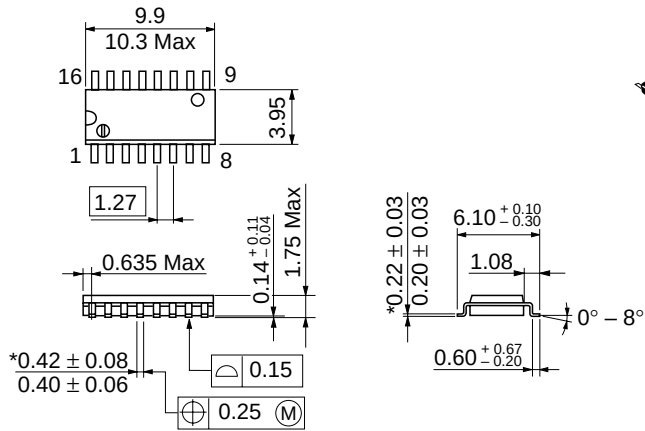
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.24 g

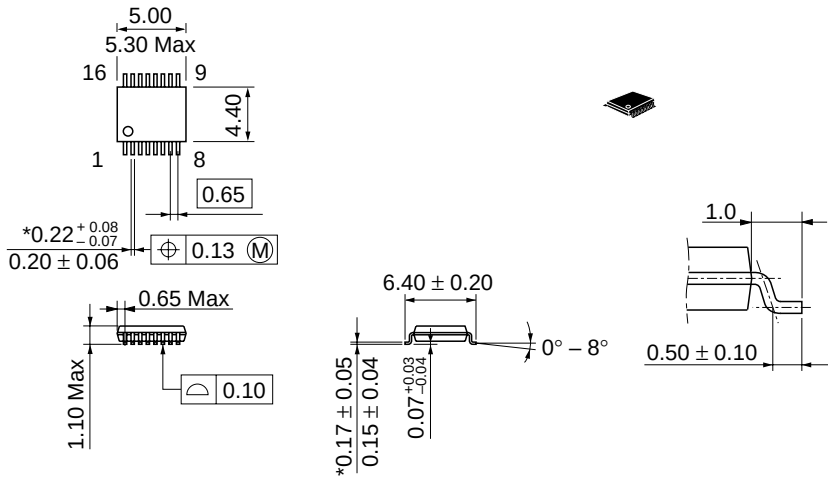
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Mass (reference value)	0.15 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Mass (reference value)	0.05 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.

2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.

3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.

4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.

5. This product is not designed to be radiation resistant.

6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.

7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	North America	: http://semiconductor.hitachi.com/
	Europe	: http://www.hitachi-eu.com/hel/ecg
	Asia	: http://sicapac.hitachi-asia.com
	Japan	: http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic Components Group Dornacher StraÙe 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 585160	Hitachi Asia Ltd. Hitachi Tower 16 Collyer Quay #20-00, Singapore 049318 Tel: <65>-538-6533/538-8577 Fax: <65>-538-6933/538-3877 URL: http://www.hitachi.com.sg Hitachi Asia Ltd. (Taipei Branch Office) 4/F, No. 167, Tun Hwa North Road, Hung-Kuo Building, Taipei (105), Taiwan Tel: <886>-(2)-2718-3666 Fax: <886>-(2)-2718-8180 Telex: 23222 HAS-TP URL: http://www.hitachi.com.tw	Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road Tsim Sha Tsui, Kowloon, Hong Kong Tel: <852>-(2)-735-9218 Fax: <852>-(2)-730-0281 URL: http://www.hitachi.com.hk
--	---	--	--

Copyright © Hitachi, Ltd., 2000. All rights reserved. Printed in Japan.
Colophon 2.0