HD74AC393

Dual Modulo-16-Counter

HITACHI

ADE-205-396 (Z) 1st. Edition Sep. 2000

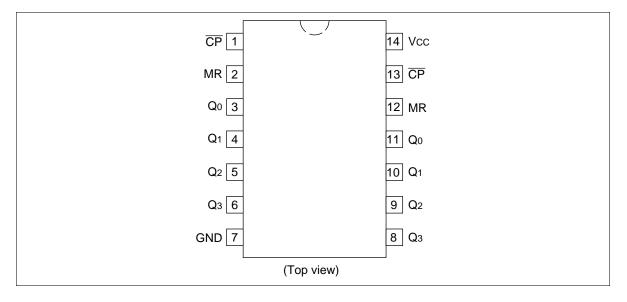
Description

The HD74AC393 contains a pair of high speed 4-stage ripple counters. Each half of the HD74AC393 operates as a modulo-16 binary divider, with the last three stages triggered in a ripple fashion. The flip-flops are triggered by a High-to-Low transition of their \overline{CP} inputs. Each half of each circuit type has a Master Reset input which responds to a High signal by forcing all four outputs to the Low state.

Feature

Outputs Source/Sink 24 mA

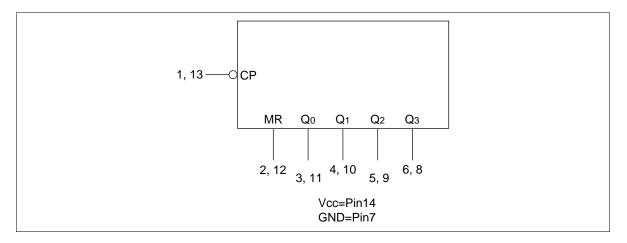
Pin Arrangement





HD74AC393

Logic Symbol (each half)



Pin Names

Clock Pulse Input (Active Falling Edge)

MR Asynchronous Master Reset Input (Active High)

 $Q_0 - Q_3$ Flip-flop Outputs

Functional Description

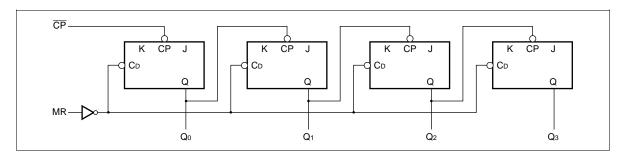
Each half of the HD74AC393 operates in the modulo-16 binary sequence, as indicated in the + 16 Truth Table. The first flip-flop is triggered by High-to-Low transitions of the $\overline{\text{CP}}$ input signal. Each of the other flip-flops is triggered by a High-to-Low transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A High signal on MR forces all outputs to the Low state and prevents counting.

Truth Table

| Count | Outputs | | | | | | | |
|-------|---------------------|-------|-------|---------------------|--|--|--|--|
| | $\mathbf{Q}_{_{3}}$ | Q_2 | Q_1 | $\mathbf{Q}_{_{0}}$ | | | | |
| 0 | L | L | L | L | | | | |
| 1 | L | L | L | Н | | | | |
| 2 | L | L | Н | L | | | | |
| 3 | L | L | Н | Н | | | | |
| 4 | L | Н | L | L | | | | |
| 5 | L | Н | L | Н | | | | |
| 6 | L | Н | Н | L | | | | |
| 7 | L | Н | Н | Н | | | | |
| 8 | Н | L | L | L | | | | |
| 9 | Н | L | L | Н | | | | |
| 10 | Н | L | Н | L | | | | |
| 11 | Н | L | Н | Н | | | | |
| 12 | Н | Н | L | L | | | | |
| 13 | Н | Н | L | Н | | | | |
| 14 | Н | Н | Н | L | | | | |
| 15 | Н | Н | Н | Н | | | | |

H: High Voltage Level
L: Low Voltage Level

Logic Diagram (one, half shown)



HD74AC393

DC Characteristics (unless otherwise specified)

| Item | Symbol | Max | Unit | Condition |
|----------------------------------|-----------------|-----|------|--|
| Maximum quiescent supply current | I _{cc} | 80 | μΑ | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, Ta = Worst case |
| Maximum quiescent supply current | I _{cc} | 8.0 | μΑ | $V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, Ta = 25°C |

AC Characteristics: HD74AC393

| | | | Ta = +25°C C _∟ = 50 pF | | | Ta = -40° C to $+85^{\circ}$ C C _L = 50 pF | | |
|--|------------------|-----------------------|--------------------------------------|------|------|---|------|--------------|
| Item | Symbol | V _{cc} (V)*1 | Min | Тур | Max | Min | Max | Unit |
| Maximum clock | f _{max} | 3.3 | 125 | _ | _ | 100 | _ | MHz |
| frequency | | 5.0 | 150 | | _ | 125 | _ | |
| Propagation delay | t _{PLH} | 3.3 | 1.0 | 8.5 | 12.0 | 1.0 | 13.0 | ns |
| \overline{CP} to $Q_{\scriptscriptstyle{0}}$ | | 5.0 | 1.0 | 6.5 | 9.0 | 1.0 | 10.0 | |
| Propagation delay | t _{PHL} | 3.3 | 1.0 | 8.0 | 11.5 | 1.0 | 12.5 | ns |
| \overline{CP} to $Q_{\scriptscriptstyle{0}}$ | | 5.0 | 1.0 | 6.0 | 8.5 | 1.0 | 9.5 | |
| Propagation delay | t _{PLH} | 3.3 | 1.0 | 12.0 | 15.0 | 1.0 | 16.0 | ns |
| CP to Q₁ | | 5.0 | 1.0 | 9.5 | 12.0 | 1.0 | 13.0 | |
| Propagation delay | t _{PHL} | 3.3 | 1.0 | 11.5 | 14.5 | 1.0 | 15.5 | ns |
| \overline{CP} to Q₁ | | 5.0 | 1.0 | 9.0 | 11.5 | 1.0 | 12.5 | |
| Propagation delay | t _{PLH} | 3.3 | 1.0 | 15.0 | 18.0 | 1.0 | 19.5 | ns |
| \overline{CP} to $Q_{\scriptscriptstyle 2}$ | | 5.0 | 1.0 | 12.0 | 14.5 | 1.0 | 16.0 | _ |
| Propagation delay | t _{PHL} | 3.3 | 1.0 | 14.5 | 17.5 | 1.0 | 19.0 | ns |
| \overline{CP} to Q_2 | | 5.0 | 1.0 | 11.5 | 14.0 | 1.0 | 15.5 | |
| Propagation delay | t _{PLH} | 3.3 | 1.0 | 18.0 | 20.5 | 1.0 | 22.0 | ns |
| CP to Q₃ | | 5.0 | 1.0 | 14.5 | 17.0 | 1.0 | 18.5 | |
| Propagation delay | t _{PHL} | 3.3 | 1.0 | 17.5 | 20.5 | 1.0 | 21.5 | ns |
| \overline{CP} to $Q_{\scriptscriptstyle 3}$ | | 5.0 | 1.0 | 14.0 | 16.5 | 1.0 | 17.5 | _ |
| Propagation delay | t _{PHL} | 3.3 | 1.0 | 10.5 | 14.0 | 1.0 | 15.0 | ns |
| MR to Q_0 , Q_1 , Q_2 or Q_3 | | 5.0 | 1.0 | 8.5 | 11.0 | 1.0 | 12.0 | |

Note: 1. Voltage Range 3.3 is $3.3 \text{ V} \pm 0.3 \text{ V}$ Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

AC Operating Requirements: HD74AC393

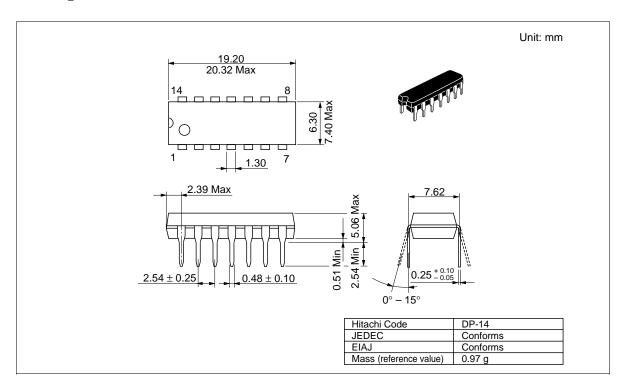
| | | V _{cc} (V)* ¹ | Ta = +25°C C _L = 50 pF | | $Ta = -40^{\circ}C$ to +85°C $C_{L} = 50 \text{ pF}$ | _ Unit |
|------------------------|------------------|-----------------------------------|--------------------------------------|------------|--|--------------|
| Item | Symbol | | Тур | Guaranteed | Minimum | |
| Pulse width CP | t _w | 3.3 | 3.5 | 5.5 | 7.0 | ns |
| | | 5.0 | 2.5 | 4.5 | 5.0 | _ |
| Recovery time MR to CP | t _{rec} | 3.3 | -2.5 | 0.0 | 0.0 | ns |
| | | 5.0 | -2.5 | 0.0 | 0.0 | |

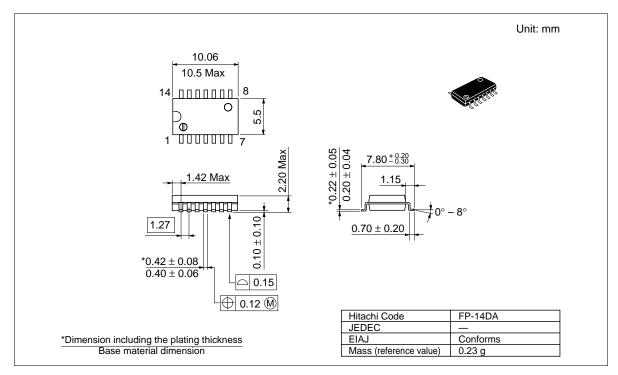
Note: 1. Voltage Range 3.3 is $3.3 \text{ V} \pm 0.3 \text{ V}$ Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

Capacitance

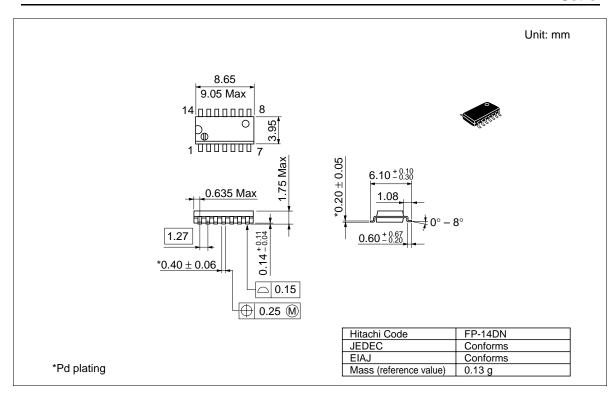
| Item | Symbol | Тур | Unit | Condition | |
|-------------------------------|-------------------|-----|------|--------------------------|--|
| Input capacitance | C _{IN} | 4.5 | pF | $V_{CC} = 5.5 \text{ V}$ | |
| Power dissipation capacitance | $C_{\mathtt{PD}}$ | 50 | pF | $V_{CC} = 5.0 \text{ V}$ | |

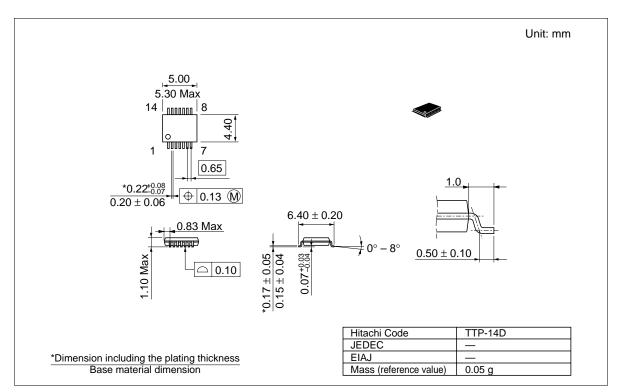
Package Dimensions





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