HD49429F

Preliminary Specification

HITACHI

Rev. 2
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General Description

HD49429F is a highly integrated MCNS compliant Upstream processor optimized for applications such as Cable Modems and Set-top boxes. It forms a complete and optimal solution with its companion HD49430F Down-stream processor. The HD49429F consists of a highly programmable encoder, Nyquist Filter and RF modulator using fully digital implementation. A highly accurate on-chip 10 bit D/A provides a RF analog output which can be used after simple low pass filtering. The HD49429F also has a highly optimized interface to a external MAC.

HD49429F is implemented in an advanced CMOS process and uses a single 3.3V (+/- 10%) power supply, and is packaged in a low cost 100pin PQFP.

Features

- State of the art QPSK/16 QAM MCNS Compliant Modulator using full digital Synthesis.
  - — Highly programmable architecture can provide modulated carrier from 1-42Mhz using programmable NCO with very high resolution.
  - — Fully programmable Nyquist filter can implement a variety of standards (25% excess BW nominal).
  - — Highly programmable interpolators can implement a large number of related baud rates from 160Kbaud to 3.2Mbaud using a single crystal.
  - — Burst or Continuous Mode operation. Continuous mode operation has no restrictions.
  - — Programmable Bit-stream Formatting and Encoding
    - Programmable preamble insertion of up to 1024 bits.
    - scrambling with Pseudo- Bit Random sequence (MCNS Specification).
    - Programmable RS encoder with up to 20 parity bytes (10 corrections).
  - — On-chip Buffer and Simplified Interface to External MAC.
  - — General Purpose Parallel Port and I^2C port for external control
- High Performance Analog circuits to optimize system implementation and reduce system cost.
  - — 102.4 MHz internal synthesis clock is derived from a on-chip 5x multiplier. This helps reduce EMI and RF interference problems.
  - — On-chip 10-bit DAC provides a high quality modulated carrier, and eliminates need for a expensive external DAC.

- .
  — Low Power
  — Surface -mount PQFP packaging

Simplified Chip Block Diagram

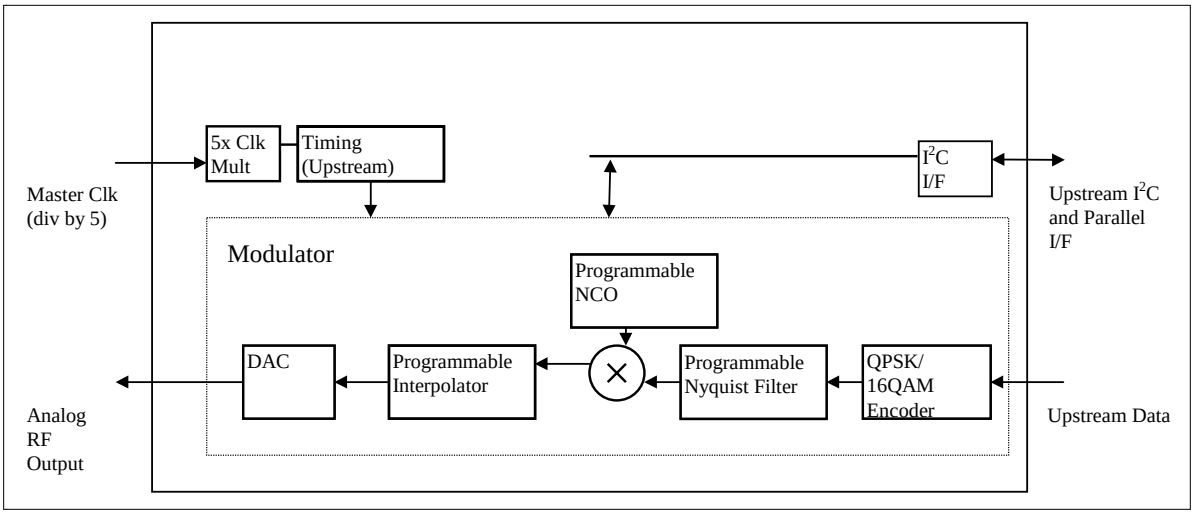

Figure 1 Simplified Block Diagram

Detailed System Specifications

QPSK Modulator Specifications

Table 1 Modulator Specifications

Parameter	Sym	Specification
Analog RF Signal to Out of band RMS noise ratio.	SNRo	50 dB (Noise measured in equivalent signal B/W).
Programmable Carrier Frequency Step Size		12 Hz
Master Clock Frequency	Fmax	102.4 MHz
Max Carrier Frequency	Fcmax	42 MHz
Max Baud Rate	Bmax	F/40 (for a given master frequency F)
Min Baud Rate	Bmin	F/640 (for a given master frequency F)
Baud Rate Steps	Bst	F/40, F/48,F/56.....F/640
Programmable Nyquist Filter Roll-off (excess B/W)	alpha	25% nominal
D/A Resolution	N	10 bits
D/A Slew Rate	SR	50V/uS
D/A Peak-Peak output	Vpp	0.5 V

Detailed Register Description

Table 2 Register Description

Register Name	Addr	Bits	Value	Description
REV_NO	0	[3:0]		Read-only register gives the revision number of the chip.
NYQ_MEM_ADDR	1	[7:0]	d0	Register used as a address pointer for programming the Nyquist RAM. The RAM is written/read using the READ_ROW and WRITE_ROW commands described later.
NYQ_MEM_B0	2	[7:0]	d0	Register used for reading/writing data from/to Nyquist RAM. This register represents the 0th byte in the 9 byte wide Nyquist RAM word.
NYQ_MEM_B1	3	[7:0]	d0	Register used for reading/writing data from/to Nyquist RAM. This register represents the 1st byte in the 9 byte wide Nyquist RAM word
NYQ_MEM_B2	4	[7:0]	d0	Register used for reading/writing data from/to Nyquist RAM. This register represents the 2nd byte in the 9 byte wide Nyquist RAM word
NYQ_MEM_B3	5	[7:0]	d0	Register used for reading/writing data from/to Nyquist RAM. This register represents the 3rd byte in the 9 byte wide Nyquist RAM word
NYQ_MEM_B4	6	[7:0]	d0	Register used for reading/writing data from/to Nyquist RAM. This register represents the 4th byte in the 9 byte wide Nyquist RAM word.
NYQ_MEM_B5	7	[7:0]	d0	Register used for reading/writing data from/to Nyquist RAM .This register represents 5th byte in the 9 byte wide Nyquist RAM word
NYQ_MEM_B6	8	[7:0]	d0	Register used for reading/writing data from/to Nyquist RAM This register represents the 6th byte in the 9 byte wide Nyquist RAM word.
NYQ_MEM_B7	9	[7:0]	d0	Register used for reading/writing data from/to Nyquist RAM This register represents the 7th byte in the 9 byte wide Nyquist RAM word
NYQ_MEM_B8	10	[5:0]	d0	Register used for reading/writing data from/to Nyquist RAM This register represents the 8th byte in the 9 byte wide Nyquist RAM word Only bits (5:0) are used, since only 70 bits are required for each half of the filter.
BUF_MEM_ADDR0	11	[7:0]	d0	These 2 registers combine to form a single 9 bit register BUF_MEM_ADDR, which is used as an address pointer register for accessing the Buffer RAM.
BUF_MEM_ADDR1	12	[7:0]	d0	
BUF_MEM_DATA	13	[7:0]	d0	This register is used to read/write data from/to Buffer RAM. When a byte is written/to read/from this register, the byte is written/to read/from the location in Buffer RAM pointed to by the BUF_MEM_ADDR. BUF_MEM_ADDR is automatically incremented when this register is addressed.

Register Name	Addr	Bits	Value	Description
PR_MEM_ADDR	14	[7:0]	d0	Address Pointer register for accessing Profile/Preamble RAM .
PR_MEM_DATA	15	[7:0]	d0	Data Register for writing/reading Profile/Preamble RAM. When a byte is written/to read/from this register, the byte is written/to read/from the location in Preamble RAM pointed to by PR_MEM_ADDR. PR_ME.M_ADDR is automatically incremented when this register is accessed
NYQ_OVERRIDE	16	[0:0]	**0**	Normal Operation
			1	When accessing NYQ_RAM using microprocessor I/F, this bit must be set to 1.
PR_OVERRIDE	16	[1:1]	**0**	Normal Operation
			1	When accessing PR_RAM using microprocessor I/F, this bit must be set to 1.
BUF_OVERRIDE	16	[2:2]	**0**	Normal Operation
			1	When accessing BUF_RAM using microprocessor I/F, this bit must be set to 1.
AUTO_INC_DIS	16	[3:3]	**0**	Address Pointer register is auto-incremented after each read/write access.
			1	This bit turns off the auto increment feature of the micro i/f pointer register. This bit is set to 1 when bursting data into/out of PR_RAM or BUF_RAM using micro i/f.
ON_DELAY0	17	[7:0]	d0	These 2 registers form the 12 bit ON_DELAY register. This register is used to delay the start of the XMIT_EN pulse. An internal clock with frequency equal to (5*REF_CLK_FREQ/4) is used to generate delay.
ON_DELAY1	18	[3:0]	d0	
OFF_DELAY0	19	[7:0]	d0	These 2 registers form the 12 bit OFF_DELAY register. This register is used to delay the end of the XMIT_EN pulse. An internal clock with frequency equal to (5*REF_CLK_FREQ/4) is used to generate delay.
OFF_DELAY1	20	[3:0]	d0	
FEC_T	21	[3:0]	d3	This register programs T, the error correction capability of the Reed-Solomon encoder. The encoder will introduce 2T parity bytes in each packet.
RAND_EN	21	[4:4]	d1	This bit enables the on-chip Randomizer.
BUF_EN	21	[5:5]	d1	This bit enables the use of on-chip buffer to store the payload data. In this mode, the external controller can blast data into the on-chip 2Kbyte buffer. When this bit is 0, the external controller must present a byte of data as it is requested by the encoder
CONT_MODE	21	[6:6]	d0	This bit enables the continuous mode when set to ‘1’. In continuous mode, the modulator transmits continuously (and expects continuous payload data). The payload is encoded and packetized as programmed using other registers.
FEC_K	22	[7:0]	d53	This register programs the payload of the Reed-Solomon block (number of bytes). The total block length is K + 2T.
PAYLOAD0	23	[7:0]	d59	These 3 registers are concatenated to form the 20 bit PAYLOD register. This defines the total size of the payload in bytes.

Register Name	Addr	Bits	Value	Description
PAYLOAD1	24	[7:0]	d0	PAYLOAD2[3] must be set to “0” , and hence the maximum programmable value is (2^{19} - 1)
PAYLOAD2	25	[3:0]	d0	
MASK_PAYLOAD	25	[4:4]	0	The register will be over-written by PAYLOAD value in profile RAM unless VALID_PR_RAM value is ‘0’.
			1	The register will not be over-written by PAYLOAD value in profile RAM.
ZERO_PAD0	26	[7:0]	d59	These 3 registers are concatenated to form the 20 bit ZEROPAD register. This defines the total size of the packet to be transmitted, including encoding overhead and zero-padding.
ZERO_PAD1	27	[7:0]	d0	
ZERO_PAD2	28	[3:0]	d0	ZERO_PAD2[3] must be set to “0” , and hence the maximum programmable value is (2^{19} - 1)
MASK_ZERO_PAD	28	[4:4]	0	The register will be over-written by ZEROPAD value in profile RAM unless VALID_PR_RAM value is ‘0’.
				The register will not be over-written by ZEROPAD value in profile RAM.
			1	
PRE_START0	29	[7:0]	d0	These 2 registers are concatenated to form the 9 bit PRE_START register. The 1024 bit preamble stored in the PR_RAM can be accessed on 2-bit symbol boundaries. The preamble can use any contiguous portion of this 1024 bit (512 symbols in QPSK, 256 symbols in 16-QAM) sequence. This register defines the starting address of the 2-bit symbol in the sequence. For QPSK, allowed values are (0,1,2,3,…511). The allowed values for 16-QAM are (0,2,4,6…510).
PRE_START1	30	[0:0]	d0	
PRE_STOP0	31	[7:0]	d15	These 2 registers are concatenated to form the 9 bit PRE_STOP register. The 1024 bit preamble stored in the PR_RAM can be accessed on 2-bit symbol boundaries. The preamble can use any contiguous portion of this 1024 bit (512 symbols in QPSK, 256 symbols in 16-QAM) sequence. This register defines the end address of the 2-bit symbol in the sequence. For QPSK, allowed values are (0,1,2,3,…511). The allowed values for 16-QAM are (0,2,4,6…510).
PRE_STOP1	32	[0:0]	d0	
INCREMENT	33	[7:0]	d31	This register defines the increment step required in the address generator for the Nyquist RAM. This value depends on the sub-sampling required in the filter stored in the Nyquist RAM. If Nx sub-sampling of stored filter is required, then the value programmed in this register is (2N-1). The default filter stored in the RAM is a 80-tap filter. Hence, if a interpolation ratio of 5 is requires, then a subsampling ratio of (80/5 = 16) is required , which in turn requires INCREMENT of (2*16 - 1= 31).
START_ADDR	34	[7:0]	d0	This register defines the starting address of the NYQ_RAM location where the filter pattern begins.
MODTYPE	35	[0:0]	**0**	QPSK
				16 QAM.
			1	
DIFF_EN	35	[1:1]	0	Non-Differential Encoding
				Differential Encoding

Register Name	Addr	Bits	Value	Description
			1	
PI_BY_4	35	[2:2]	0	Normal Operation
				MODTYPE register is overridden and pi/4 modulation is used
			1	
INTERP_RATIO	36	[6:0]	d5	This register defines the interpolation ratio to be used by the programmable interpolator. Since there is a fixed 8x interpolator, the total interpolation is 8*INTERP_RATIO.
SEED0	37	[7:0]	d255	These 2 registers are concatenated to get a 15 bit SEED register. This register is used to program a seed value into the data randomizer.
SEED1	38	[6:0]	d127]	
GBAND	39	[7:0]	d5	This register programs the number of symbols to be used a s guard band.
MINLOAD	40	[7:0]	d13	This register is used to program the level of emptiness of the buffer that is required before the RDY_LOAD signal will be asserted (after the buffer has been completely filled.). The emptiness required is equal to 8*MINLOAD bytes.
MINXMIT	41	[7:0]	d13	**ERRATA: This register is not usable.**
				Original Description is given below.
				The Buffer controller can be programmed so that it will indicate to the external controller when certain level of fullness of buffer is reached . 8*MINXMIT is the minimum fullness (in bytes) that is required when the RDY_XMIT signal will be asserted.
DIG_EN	42	[0:0]	**0**	Digital outputs are masked
				This bit enables the digital outputs of the modulator.
			1	
IQ_SWAP	42	[1:1]	**0**	Normal Operation
				I,Q channels are swapped.
			1	
VALID_PR_RAM	42	[2:2]	**0**	Selected Profile RAM data will not be transferred to program registers as soon as XMIT input is asserted.
				Selected Profile RAM data will be transferred to program registers as soon as XMIT input is asserted
			1	
SCALE	43	[7:0]	d58	This register is used to scale the output of the Nyquist filter. 64 is the center value.
AMP_CTL	44	[7:0]	d0	This register value is output as the 1-bit output of a sigma-delta converter. This then may be used as a gain control voltage of the external amplifier.
PROFILE	45	[2:0]	d0	This register is OR'd with the external PROFILE[2:0} pins to determine the profile to be used.
ATTENUATE	45	[4:3]		This register controls attenuation of the modulator output into the

Register Name	Addr	Bits	Value	Description
				on-chip DAC.
			00	No attenuation
			01	_ attenuation
			10	_ attenuation
			11	unused
DELAY	46	[7:0]	d0	There is a fixed delay and a programmable delay after which the encoder will respond to the XMIT pulse. This register defines the programmable delay in clock cycles whose frequency is (REF_CLK_FREQ*5/4).
OUT_FREQ_0	47	[7:0]	d0	These 3 registers are concatenated to give the 24 bit OUT_FREQ register. This controls the RF frequency.
OUT_FREQ_1	48	[7:0]	d25	
OUT_FREQ_2	49	[7:0]	d0	
INIT_BUF	192	[7:0]		When this value is written into the micro i/f address pointer register, the on-chip buffer is initialized. This may also be done using the INIT_BUF_BAR pin.
READ_ROW	221	[7:0]		When this value is loaded into the micro i/f address pointer register, the data contained in the location pointed to by NYQ_MEM_ADDR register is read into the NYQ_MEM_DATA register.
WRITE_ROW	238	[7:0]		When this value is loaded into the micro i/f address pointer register, the data contained in NYQ_MEM_DATA register is written to the location pointed to by NYQ_MEM_ADDR register.
RESET	255	[7:0]		When this value is written into the micro i/f address pointer register, the modulator is reset, without disturbing the programmed values.

Detailed Pin Description

Table 3 Detailed Pin List

Modulator Pins(39)

DATAIN[7:0]	I	Upstream Data.	8
RDY_LOAD	O	When high, Indicates that there is vacancy in the buffer. When this signal goes from low to high, it means that there is a vacancy equal to greater than 8*MINLOAD bytes.	1
RDY_XMIT	O	**Errata:** **Indicates that no transmission is currently in the pipeline**. Original Description: Indicates that one packet of data is stored in internal buffer, and a transmit operation may be done.	1
INIT_BUF_BAR	I	Initializes internal Data Buffers	1
DATAIN_EN_BAR	I	Enable from data source indicating new byte to be loaded (active low)	1
PROFILE[2:0]	I	Selects one out of 6 profiles	3
REF_CLK_IN	I	Master Crystal Oscillator input	1
REF_CLK_OUT	O	Master Crystal Oscillator output	1
CPOUT	O	External Filter for on-chip Multiplier	1
CBL	I	Analog Pin	1
CBU	I	Analog Pin	1
PLL_BYPASS_BAR	I	Bypasses on-chip Clock Multiplier when active(low).	1
XMIT_BAR	I	Transmit Enable Input (active Low)	1
POWER_ADJ_SL	O	Sigma Delta output to control Amp power.	1
XMIT_EN	O	Transmit Enable Output (Delayed XMIT_IN)	1
DA_DIG[9:0]	Bi	Digital RF Output (can be disabled via programming). DAC Test input when TEST_DAC_BAR = 0	10
TEST_DAC_BAR	I	RF_D port becomes a input port for DAC testing.	1
CLK_DA	O	Output Sampling Clock for external D/A (High Speed)	1
DA_OUT	O	Analog RF Output	1
REXT	I	DAC Reference Voltage	1
RFREQ	I	DAC Analog Pin	1
Upstream Control Interface (13)			
SELI2C	I	Selects I^2C mode for control Interface when high. Selects GP uP when low.	1
CS_BAR[SCL]	I	Chip Select Input for general purpose uP interface when SELI2C is low.	1

		I^2C Clock input when SELI2C is high.	
GP_READ	I	Read/Write indicator for general purpose uP I/F	1
RDY_BAR	O	Open Drain Output for general purpose uP I/F. De-assertion (low) of this signal after start of a transaction indicates to the master that the slave chip is ready to complete the transaction.	1
ADREGEN	I	Chooses accessing of internal address pointer register or the register pointed to for general purpose uP I/F	1
MICRODATA[7:0]	Bi	General Purpose uP Interface bi-directional Data bus when SELI2C is low. D[0] acts as I^2C Data I/O when SELI2C is high D[7:1] acts as I^2C Device address input.	8
Upstream Control Pins(3)			
RESET_BAR	I	Power-on Reset	1
SCAN_BAR	I	For Test Purposes only	1
TEST_BAR	I	For Test Purposes only	1
Power and Ground Pins(45)			
VDD	P		17
VSS	P		24
AVDD	P		2
AVSS	P		2
NC			0
TOTAL			100

Package Pin Assignment

Name	Package Pin No.
vss	1
vss	2
vdd	3
pwr_adj_sl	4
xmit_en	5
datain[0]	6
vdd	7
datain[1]	8
vss	9
datain[2]	10
datain[3]	11
datain[4]	12
datain[5]	13
datain[6]	14
vddr	15
datain[7]	16
vss	17
profile[2]	18
profile[1]	19
vdd	20
profile[0]	21
reset_bar	22
vdd	23
vss	24
vss	25
vss	26
vss	27
datain_en_bar	28
xmit_bar	29
vdd	30
init_buf_bar	31
da_dig[0]	32
da_dig[1]	33
vss	34
da_dig[2]	35
da_dig[3]	36

Name	Package Pin No.
vdd	37
da_dig[4]	38
da_dig[5]	39
da_dig[6]	40
da_dig[7]	41
vss	42
da_dig[8]	43
vdd	44
da_dig[9]	45
clk_da	46
test_dac_bar	47
vdd	48
vss	49
vss	50
vss	51
vss	52
vss	53
ref_clk_in	54
ref_clk_out	55
vdd	56
vdd	57
vdd	58
pll_bypass_bar	59
scan_bar	60
test_bar	61
vdd	62
vss	63
pllavss	64
cpout	65
pllavdd	66
rfreq	67
rext	68
da_out	69
cbu	70
cbl	71
dacavss	72
dacavdd	73

Name	Package Pin No.
vss	74
vss	75
vss	76
vss	77
vdd	78
seli2c	79
gp_read	80
adregen	81
vdd	82
cs_bar	83
vss	84
microdata[0]	85
microdata[1]	86
microdata[2]	87
microdata[3]	88
vdd	89
microdata[4]	90
data[5]	91
vss	92
microdata[6]	93
microdata[7]	94
ready_bar	95
vdd	96
rdy_load	97
rdy_xmit	98
vss	99
vss	100

Theory of Operation (Upstream Channel)

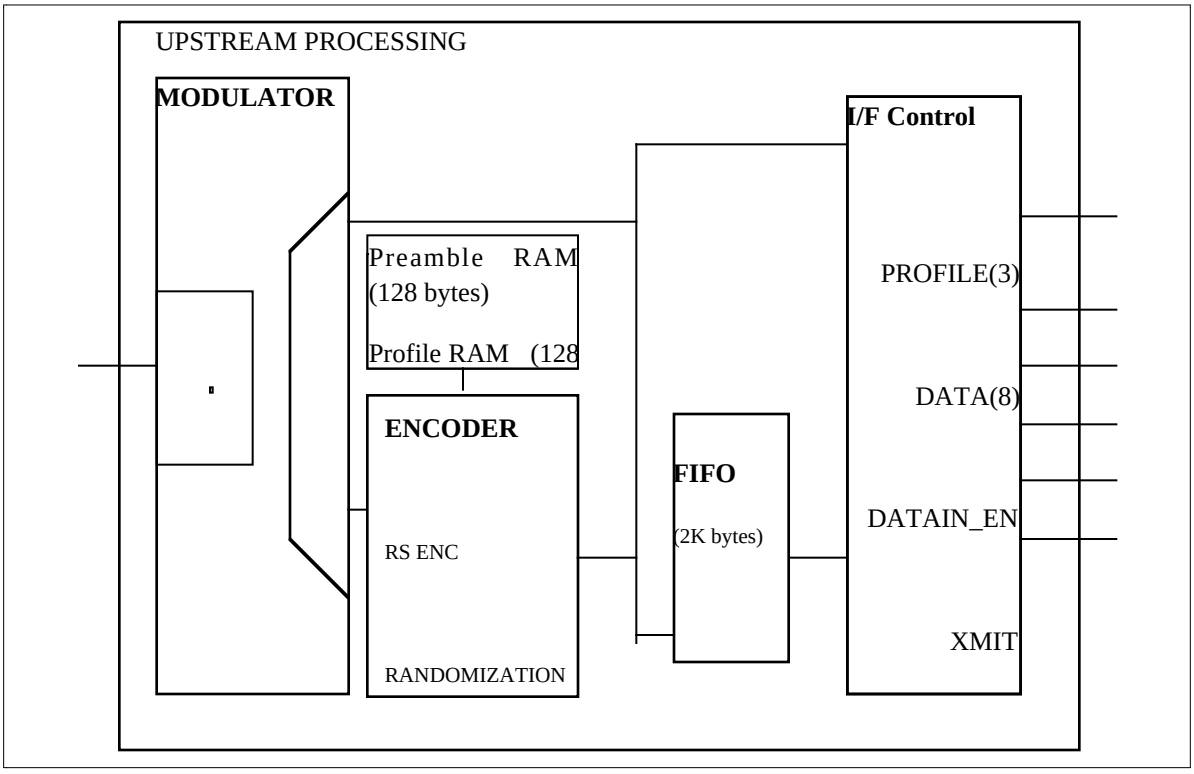

Figure 2 Upstream Modulator Block Diagram

The above block diagram depicts the major components of the HD49429F upstream processing unit.

The Modulator block accepts bits encoded into symbols (QPSK/16QAM) and modulates these symbols onto a internally generated RF carrier after appropriately interpolating and filtering the symbols. The RF carrier is generated using a on-chip NCO whose frequency is programmable as explained later. Symbol interpolation ratios and pulse shapes are also highly programmable as explained later.

The encoder block consists of a programmable Reed-Soloman encoder, a MCNS compliant Randomizer, a programmable Preamble Inserter (up to 1024 bits) and QPSK/16QAM symbol mapper. Each of these functions is fully under user control and can be disabled if desired.

The 2 Kbyte FIFO and the Interface control blocks are helpful in implementation of a cost-effective upstream channel by simplifying the interface to the Medium Access Controller (MAC). This interface is optimized for a MCNS transmission system, but is programmable enough to be useful in implementing any standard.

Modulator

The HD49429F is a versatile high performance modulator which allows a very high degree of programmability of the following parameters:

Modulation Type

QPSK, 16 QAM, pi/4 QPSK

Modulation type is controlled by registers MODTYPE, DIFF_EN, and PI_BY_4.

Following table defines the behavior of the modulator.

Table 4 Mapper Control Registers

MODTYPE	DIFF_EN	PI_BY_4	Description
0	0	0	QPSK non-differentially encoded.
0	**1**	**0**	QPSK Differentially encoded (Default)
1	0	0	QAM16 non-differentially encoded
1	1	0	QAM16 differentially encoded
X	X	1	Pi/4 encoding

Nyquist Filter

A fully programmable FIR filter can be programmed for any Excess Bandwidth between 25 -100% .

The Nyquist filter is implemented as a 14-tap programmable filter, with a filter tap coefficients stored in a on-chip RAM. The RAM is loaded with a default filter coefficient set on power-up reset for a 25% excess bandwidth Nyquist Filter. The Nyquist Filter is also a programmable interpolator, with a maximum Interpolation Ratio of 80. The output of the Nyquist Filter/Programmable Interpolator is further interpolated by a fixed 8x Interpolator.

The Default Filter programmed can be used to get programmable interpolation ratios of 5x, 10x, 20x, 40x and 80x. It is also possible to load a filter for any interpolation ratio between 4x and 80x, with any excess bandwidth between 25% and 100%.

Baud Rates

The baud rate is set by programming the Interpolation Ratio for the Programmable Interpolator/Nyquist Filter. Since there is a fixed interpolator of 8x, the total interpolation ratio is 8 x n where n is the programmed interpolation ratio.

Theoretically, any baud rate which satisfies the following expression is possible

$$B = F/(8 \times n)$$

where **B** is the baud rate, **F** is the Master clock frequency (5 times Reference Clock Frequency) and **n** is any integer between 4 and 80.

The registers INTERP_RATIO and INCREMENT are used to control the baud rate of the modulator. The following table lists the values for these registers for MCNS baud rate This programmability allows the use of the HD49429F modulator to implement virtually any standard. Following table lists some of the standardized baud rates.

Table 5 Register Program Values for MCNS Baud Rates

INTERP_RATIO	ICREMENT	Baud Rate (B)
5	31	2560 Kbaud
10	15	1280 Kbaud
20	7	640 Kbaud
40	3	320 Kbaud
80	1	160 Kbaud

Carrier Frequency

HD49429F includes a programmable high precision Numerically Controlled Oscillator. This allows choice of any carrier frequency between **0** and **F/2** where **F** is the master clock frequency (5 times Reference Clock Frequency). With a maximum master clock frequency of about 100Mhz, any carrier frequency in the 0-45Mz band can be easily obtained with inexpensive external analog filter.

The Carrier Frequency is programmed using the OUT_FREQ_0, OUT_FREQ_1, and OUT_FREQ_2 registers. These three registers form a single 24 bit word (where OUT_FREQ_2 is the most significant byte and OUT_FREQ_0 is the least significant byte).

Modulator Interface and Data Encoding

The Upstream Modulator uses a highly programmable Interface which is optimized for a MCNS compliant modulator, but also can be tailored to the needs of any system being implemented. The interface consists of a 2K byte FIFO which can be completely bypassed, or configured to work optimally in the system. It also contains a programmable Encoder which can be either entirely bypassed, or selectively programmed to implement a wide range of systems, including MCNS (default). The interface is designed to yield a highly optimized MCNS compliant upstream system, but the on-chip hardware is programmable enough to allow the designer to implement any arbitrary system using external encoding.

The following block diagram depicts the main components of the HD49429F upstream modulator.

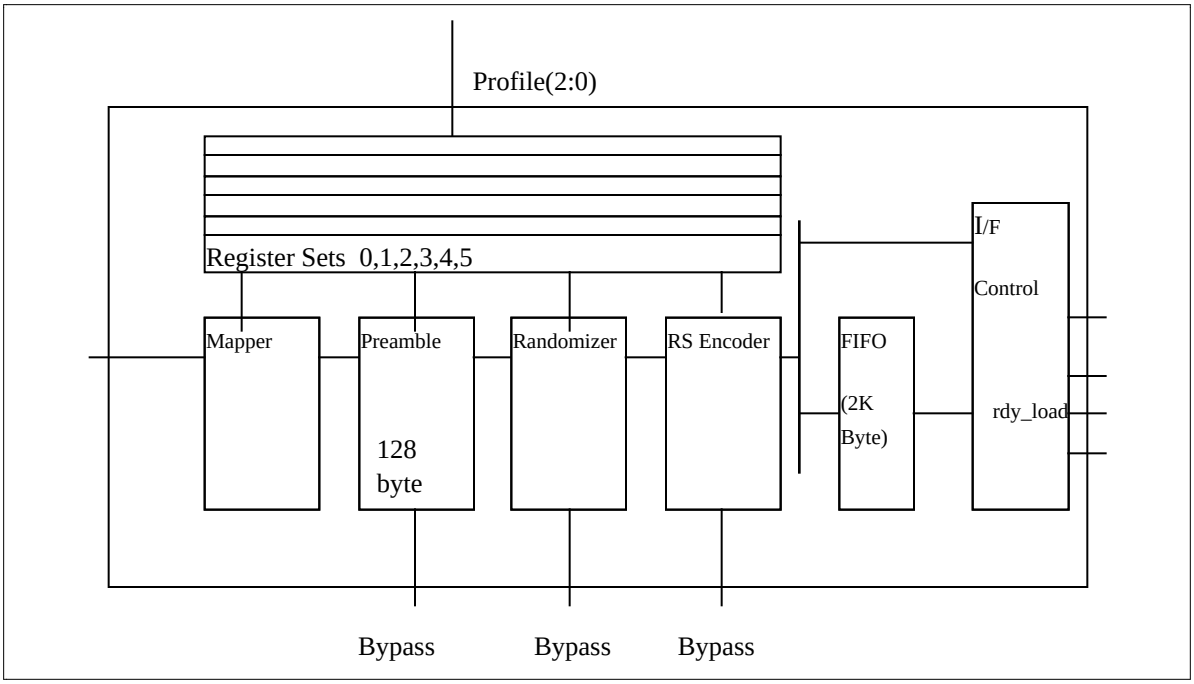

Figure 3 Encoder Block Diagram

Before describing the details of the various modes in which the HD49429F upstream processor interfaces with the Medium Access Controller (MAC), it is important to understand the 2 basic system implementation modes.

MCNS upstream communication uses frequency and time multiplexing to allow multiple nodes (modems) to communicate to the head-end. Each node is assigned a RF frequency and a time-slot. The RF carrier frequency can be easily programmed using the on-chip programming registers. It is the responsibility of the MAC to indicate the exact start time of the node's time slot so that the modulator can begin a transmission precisely during the assigned time-slot. The HD49429F Upstream Interface and the FIFO are designed to simplify this time-critical interaction between the modulator and the MAC.

Non-MCNS Mode: In this System implementation, the MAC uses the XMIT input to indicate the exact temporal location of the time-slot. The modulator pulls a byte of data each time it needs a new byte (The frequency of a new byte will depend on baud rate and modulation type). The MAC must respond immediately and provide a new byte. In this mode, the on-chip FIFO is not used. This is intended for proprietary system implementation.

MCNS Mode: In this system implementation, the MAC uses the XMIT signal only to indicate the start of a new time-slot. The Modulator then uses the data already stored in the FIFO along with pre-programmed profile information to packetize the data (with optional Randomizing, RS encoding, and preamble insertion) and complete the transmission of this packet.

In both cases, the HD49429F upstream processor will generate a time slot signal which can be used to turn on the external output amplifier.

Non-MCNS System

This mode is useful in implementation of a proprietary system, where encoding of data is done off-chip. In this system, the HD49429F Upstream processor Interface is used as follows:

Table 6 Buffer Interface in Non-MCNS Mode

DATA_IN	Byte Input	Byte-wide data input to the modulator
RDY_LOAD	out	This output is used to clock in new bytes. MAC interprets a low transition as a request for a new byte. This new byte must be ready before the high transition of this signal.
XMIT_BAR	in (active low)	The MAC uses this input to start the transmission.
XMIT_EN	out	This is a delayed version of the Xmit_bar signal. The delay is programmable and is required to take into account the processing delay in the HD49429F as well as other delays and transients in the path. This signal is used to activate the external upstream output amplifier.

The following diagram depicts the operation in this mode.

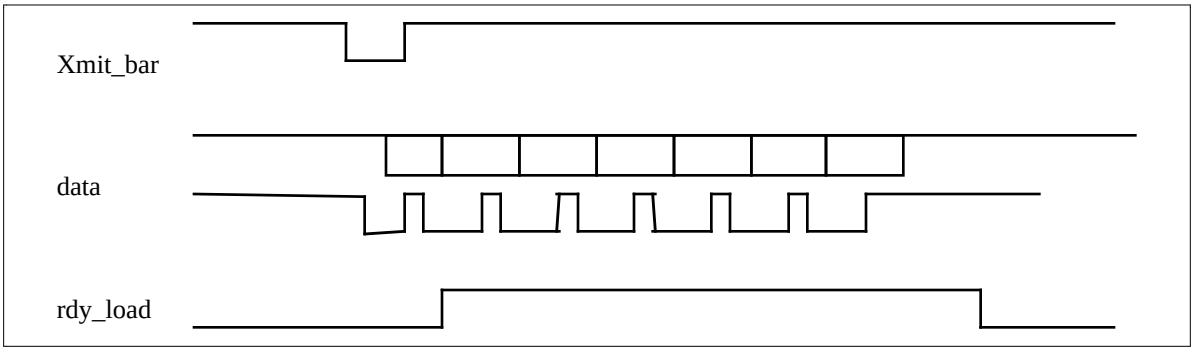

Figure 4 Buffer Interface (MCNS Mode)

MCNS System

This mode is the preferred mode for implementing a MCNS compliant upstream channel.

In a MCNS system, the external controller that implements the MAC layer protocol maintains a local system clock synchronized to the head-end clock (done using information contained in special packets that are broadcast by the head-end CMTS). When the cable modem needs upstream bandwidth, it makes a request to the CMTS using a upstream frequency and time-slot reserved for making new requests. The CMTS assigns a upstream channel and time-slot (variable length) to the cable modem, and also specifies various parameters such as baud rate, modulation type, FEC parameters, preamble length and value etc. The MAC controller must then be able to load the payload data into the upstream modulator buffers and reprogram the upstream modulator for baud rate and encoding parameters as specified by the CMTS. It then triggers the modulator at the start of the assigned time-slot (corrected for pipeline delay though the

modulator). The modulator encodes the data, modulates it on RF and presents it to the local cable termination exactly during the duration of the assigned time-slot.

The HD49429F supports easy implementation of a MCNS system as follows:

1. On-chip 2Kbyte buffer can be used to pre-load the payload data. While MCNS burst packet can contain more than 2Kbytes of data, in most cases it is expected that packet size will be smaller than 2K. In case of payload larger than 2Kbytes, buffer is managed automatically as a FIFO, and as vacancy occurs in the Buffer (as data is used up by the modulator), more payload data can be streamed into the buffer. This data is encoded and packetized, mapped into symbols and used to modulate a RF carrier.
2. 6 sets of programmable parameters (Profiles) can be stored in an on-chip RAM. Any one of these transmission profiles can be made active by either controlling 3 external control pins or programming the PROFILE register via the control interface. This enables transmission profiles to be changed between bursts with practically zero delay.

The buffer interface

In this mode, the HD49429F is ready to accept new data bytes when the FIFO reaches a programmed level of emptiness. This is communicated to the external controller using the RDY_LOAD signal. Data is clocked into HD49429F using a clock input signal(D_CLK) which is under external control and can have a maximum frequency of 5Mhz.

In case of payload data less that 2Kbytes, the complete payload can be transferred to the buffer, and then a Transmit trigger is supplied to start transmission.

In case of a payload greater than 2K bytes, the buffer is automatically managed to run as a FIFO. A programmable register called MINLOAD is associated with the buffer. When the buffer has vacancy equal to or exceeding this level, the RDY_LOAD output is asserted, and can be used by the external controller to stream in new chunk of payload at least as big as MINLOAD bytes. To maintain proper continuity, the payload loading rate must be significantly larger than the data transmit rate.

Table 7 Buffer Interface Pins in MCNS Mode

DATA	Byte Input	Byte-wide Data Input to the Modulator
DATAIN_EN_BAR	in	This is a asynchronous clock input DATA_IN bus is sampled on the negative edge of this clock signal. Max Frequency : 5 MHz
RDY_LOAD	out	This output makes a 0→1 transition when the buffer vacancy exceeds 8*MINLOAD bytes. It makes a 1→0 transition when the buffer becomes full.
XMIT_BAR	in (active low)	The MAC uses this input to start transmission process.
XMIT_EN	out	This signal is asserted when the modulator output is active. This signal is intended to turn on the external amplifier. The start of the signal can also be delayed by programming ON_DELAY register to match modulator pipeline delays and other external delays. The end of this signal can similarly be delayed by programming the OFF_DELAY register.

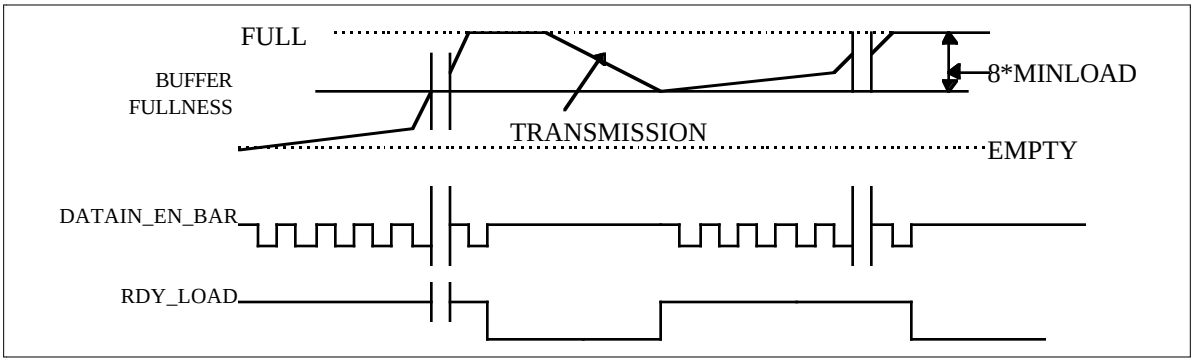

Figure 5 Buffer Interface

Modulator Programming Registers

The encoder registers on HD49429F are of two types.

1. Channel Specific Registers: These registers are unique for a given channel, and change only when the modem is assigned a new upstream channel. These registers are programmed using the general purpose parallel port or the I^2C serial port. Generally, this reprogramming will require a few microseconds. However, this is not a problem since a modem is allowed 100 ms of setup time when a new channel is assigned.
2. Profile Registers: These registers are loaded with the contents of the Profile RAM at the start of each transmission. Depending on the PROFILE control pins (or registers as explained later) the specific profile is loaded. Hence, there is virtually no setup time required (assuming the Profile RAM has been loaded during initialization).

HD49429F contains on-chip RAM to store 6 sets of programmable parameters . Each register set represents a transmission “profile”. MCNS requires that the modulator be capable of reconfiguration into any one of these profiles with minimal delay. This is achieved by 3 external control pins PROFILE(2:0) which select 1 out of 6 profiles. Alternately, the profile can be chosen by programming the on-chip PROFILE register. (In case external pins are to be used, then internal registers must be held at “000” and vice-a-versa). When the VALID_PR_RAM bit set to ‘1’, the register data for the selected profile is streamed into the profile registers when the XMIT signal is pulsed, indicating start of a new transmission. If the VALID_PR_RAM register contains a ‘0’, then register data from profile RAM is not transferred to the profile registers.

A 128 byte RAM also stores a preamble word providing 512 QPSK or 256 QAM16 symbols. A profile may use any part of this preamble word as its preamble. This is done by specifying a start address and length for each profile.

The Profile and Preamble RAMs are physically implemented as a single RAM and this RAM is loaded using the general purpose parallel port or I^2C serial port as part of the setup.

Each profile contains values for the registers described in the following table. At the start of transmission, the profile (stored in the RAM) selected by PROFILE (pins or internal registers) is downloaded into the actual register, and becomes effective immediately.

Table 8 Registers Programmable by Profile RAM

Parameter	Description	Bits
MODTYPE	Modulation type of QPSK , QAM16	1
DIFF_EN	Differential encoding enabled	1
PI_BY_4	Enables pi/4 encoding	1
INTERP_RATIO	Sets the baud rate. MCNS allows following rates. 160K, 320K, 640K, 280K, 2560K (baud)	3
INCREMENT	Sets the Interpolation factor for the Nyquist Filter.	8
START_ADDR	Selects starting address for the Nyquist Filter RAM. This should be 0 for the default Filter.	8
PRE_START0 (8 bits) PRE_START1(1 bit)	Defines the starting symbol position in the preamble word.	9
PRE_STOP0 (8 bits) PRE_STOP1(1 bit)	Defines the end symbol position in the preamble word. (*If start position is less than end position, no preamble is inserted)	9
FEC_T	Gives the number of corrections (0-10). 0 indicates no FEC.	4
FEC_K	Information payload of Reed-Soloman block.	8
RAND_EN	Enables Randomization	1
SEED0(8 bits) SEED1(7 bits)	15 bit Randomization seed.	15
PAYLOAD0(8 bits) PAYLOAD1(8 bits) PAYLAOD2(4 bits)	Indicates the payload size in bytes (before any zero padding is done). Bit PAYLOAD[19] should be zero. *This parameter will not be loaded from Profile RAM if PAYLOAD_MASK register is set to 1.	20
ZERO_PAD0(8 bits) ZERO_PAD1(8 bits) ZERO_PAD2(4 bits)	Indicates the payload size in bytes after the required amount of zero padding. (Note that zero padding is done by the encoder and should not be done by the user). Bit ZERO_PAD[19] must be 0. * This parameter will not be loaded from Profile RAM if ZERO_PAD_MASK register is set to 1.	20
GBAND	Guard Band size in symbols	8

Following are other registers that are unique for a given channel.

Table 9 Registers Unique to Each Channel

Parameter	Description	Bits
AMP_CNTL	The value programmed in this register is converted to a analog voltage using a sigma-delta converter. This voltage level may be used to control the gain of a external amp to adjust the power level. **However, the present MCNS spec for accuracy of power control may not be met with this output.**	8
OUT_FREQ_0 OUT_FREQ_1 OUT_FREQ_2	This 24 bit register controls the NCO frequency with a accuracy of +-6 Hz providing a frequency range of 0 to 45Mhz.	24
IQ_SWAP	Causes spectrum inversion	1

The Preamble Word (128 bytes) and 6 profiles are stored in a single 256 byte RAM. The RAM is used in the following manner.

Table 10 Profile RAM Organization

Address	Register	Comments
0	Preamble	Start of Preamble word
	Preamble	
127	Preamble	End Of Preamble word
128	FEC_T	Start Of Profile 0
129	FEC_K	
130	PAYLOAD0	
131	PAYLOAD1	
132	PAYLOAD2	
133	ZERO_PAD0	
134	ZERO_PAD1	
135	ZERO_PAD2	
136	PRE_START0	
137	PRE_START1	
138	PRE_STOP0	
139	PRE_STOP1	
140	INCREMENT	
141	START_ADDR	
142	MODTYPE,DIFF_EN,PI_BY_4	
143	INTRP_RATIO	
144	SEED0	
145	SEED1	
146	GBAND	
147	BLANK	End of profile 0
148		Start profile 1
167		End profile 1
168		Start profile 2
187		End profile 2
188		Start profile 3
207		End profile 3
208		Start profile 4

Address	Register	Comments
227		End profile 4
247		End profile 5
248	BLANK	Unused
255	BLANK	

Detailed Encoder Description

FIFO

The use of the on-chip 2K byte FIFO is enabled when the BUF_EN register is programmed to '1'. When the FIFO is enabled, the external MAC controller can stream payload data into the FIFO at up to 5 Mbytes/s. Once the payload data is in the FIFO, the modulator can use it to encode and transmit when the pin XMIT is asserted. The MINLOAD register is used to fine-tune the behavior of the FIFO. Pin RDY_LOAD can be used by the external MAC controller to interact with the FIFO. When RDY_LOAD transitions from 0→1, it indicates that there is a FIFO vacancy equal to or greater than (8 x MINLOAD) bytes. Once the external controller sees the RDY_LOAD output asserted, it can stream in at least (8 x MINLOAD) bytes without overflowing the buffer.

When BUF_EN is '0', the FIFO is inactive and the encoder uses the RDY_LOAD signal to clock a new byte in directly from the DATA_IN[7:0] pins. The data should be stable at the rising edge of the RDY_LOAD output.

Table 11 FIFO Related Registers

Register Name	Width	Description
BUF_EN	**1**	FIFO is enabled when = '1' FIFO is disabled when = '0'
MINLOAD	8	Effective only when BUF_EN = '1' RDY_LOAD signal is asserted when FIFO vacancy is equal to or greater than 4*MINLOAD bytes

MCNS Burst Packet Structure

Each MCNS burst starts with a preamble of 0 to 512 symbols, followed by a variable number of Reed-Soloman Blocks carrying information payload and parity bytes , followed by a guard band of up to 255 symbols. (the modulator output is quiet during the guard band period).

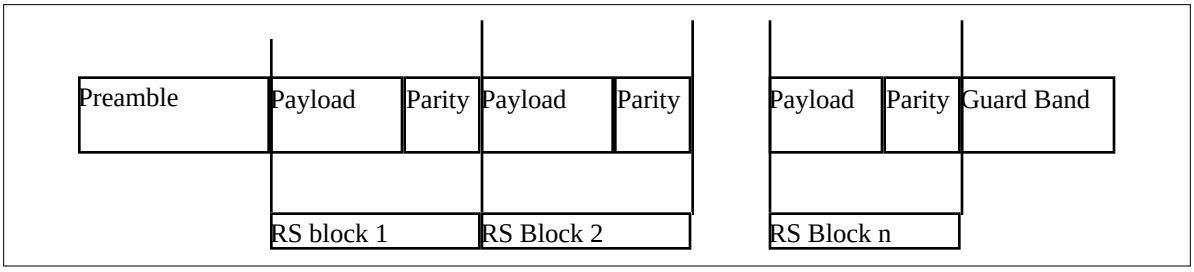

Figure 6 MCNS Packet Structure

Modulator Pipe-line Delay

The falling edge of the XMIT_BAR input initiates a new transmission. The encoder begins drawing data from the buffer (if buffer is enabled) , encodes the data , and feeds it to the pulse shaping filter (nyquist filter). This signal is interpolated and mixed with a RF carrier and then presented to the on-chip D/A converter.

The latency from when the XMIT_BAR input is asserted to the appearance of the 1st symbol in the transmission depends on the baud rate selected and the value programmed in the DELAY register. Since the MCNS transmissions must occur in the time slot allocated by the CMTS, the MAC controller must take the transmission latency of the modulator into account, and generate the pulse on the XMIT_BAR input accordingly. Since the XMIT_BAR signal is sampled by an internal clock with a frequency around 25 Mhz, there is an inherent uncertainty of 40 ns in this latency.

A burst transmission out of the modulator will have a ramp-up and ramp-down at the beginning and end of the transmission respectively. Both these ramps are equal to 7 symbol periods. To preserve the spectral purity of the transmission, both the ramp-up and ramp-down must be included in the transmission waveform.

MCNS Baud Rate	Interpolation Ratio	Number of Output Clock Cycles in Symbol Period	Tx Delay(in output clock cycles)
2.56 M Baud	5x	40	650 (= 330 + 8*40)
1.28 M Baud	10x	80	970 (= 330 + 8*80)
640 K Baud	20x	160	1610 (= 330 + 8*160)
320 K Baud	40x	320	2890 (= 330 + 8*320)
160 K Baud	80x	640	5450 (=330 + 8*640)

Tx Delay is a sum of fixed delay in the encoder and a variable delay (baud rate dependent) through the nyquist filters and interpolators. This can generally be expressed as:

Tx Delay = 330 cycles + 8*Cb

where Cb is the number of clock cycles contained in one symbol period.

To align the rising and falling edges of the TX_ENABLE signal with RF waveform on the DA_OUT pin, the ON_DELAY and OFF_DELAY registers should be programmed to 82.

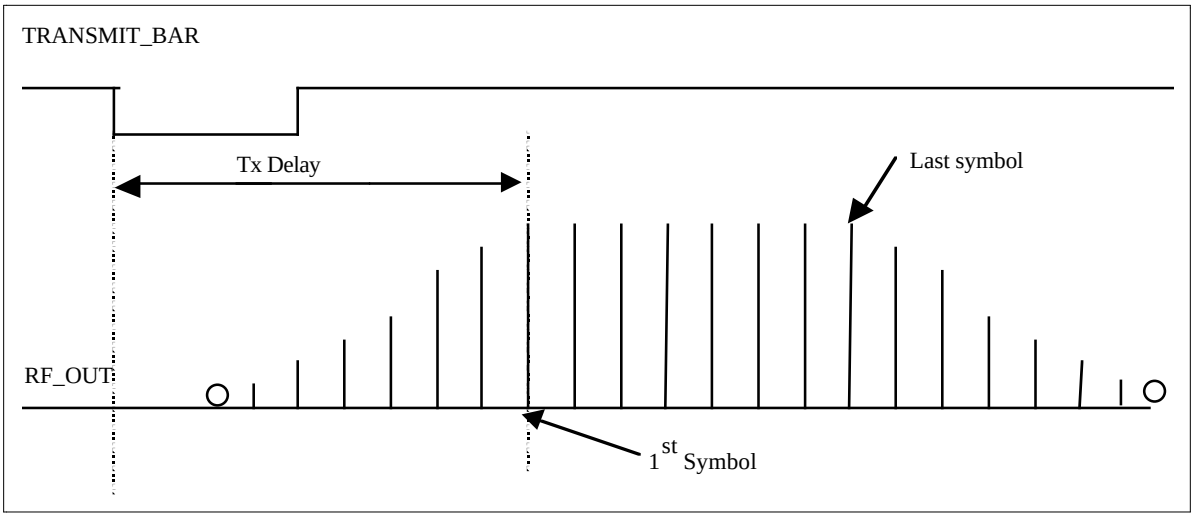

Figure 7 Modulator Latency

Control Interfaces

The programming and status registers can be accessed via the chip's control interface. For maximum System flexibility, a general purpose Microprocessor Interface and an I^2C (TM) compatible serial interface are available on the chip. The two interfaces share I/O pins, and only one Interface can be selected in a system implementation by hardwiring the SELI2C input appropriately. Details of each interface are given below.

General Purpose uP Interface

The following I/O pins constitute the uP Interface. The uP interface is available when the SELI2C pin is low. The following table gives a detailed description of the I/O pins involved.

Table 12 General Purpose uP Interface

Pin Name	Type	Description
CS_BAR	I	The chip select input activates a transaction. The type of the transaction is determined by the state of the GP_READ and ADREGEN pins. The READY_BAR output deasserts itself when the chip is ready to complete the transaction. The external micro-controller then finishes the transaction by de-asserting the CS_BAR pin.
GP_READ	I	This input indicates whether a transaction will be read or write transaction. In a read transaction, data from an on-chip register will be read by the external controller. In a write transaction, data will be written into one of the chip's on-chip registers.
ADREGEN	I	When this input is asserted during a write, data from the MICRODATA[7:0] bus is written into the on-chip address pointer register. When this input is de-asserted, an on-chip register pointed to by the address pointer register is read or written.
MICRODATA[7:0]	Bi	This bi-directional parallel bus is used to read and write on-chip registers.
READY_BAR	O	This is a tri-state output. It is driven only when the chip is selected (by asserting CS_BAR input). The chip indicates that it is ready to complete the transaction by de-asserting this pin. The transaction is formally complete when the external controller de-asserts CS_BAR input.

This interface uses an indirect addressing mode for accessing the on-chip registers. The Address Pointer Register acts as the pointer. Hence, a random register access typically will require 2 I/F transactions. During the first transaction, ADREGEN input is asserted, and the address of the register that needs to be accessed is written to the Address Pointer Register. During the next transaction, the appropriate register is accessed. However, if registers are to be accessed sequentially, then an auto-increment feature will allow one access per transaction for all subsequent sequential accesses. The auto-increment feature can be turned off by setting the AUTOINC_DISABLE register to '1'.

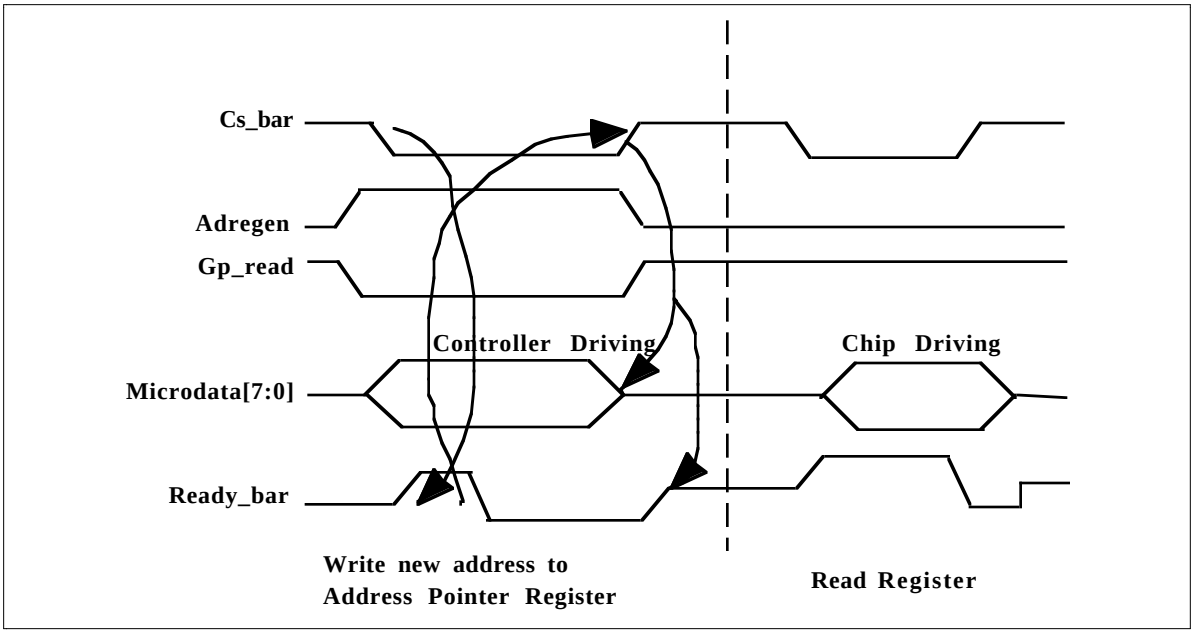

Figure 8 uP Interface Protocol

Serial Interface

The Serial interface is active when the SELI2Cinput pin is wired high. The serial interface is I^2C (TM) compatible and involves the following I/O pins.

Table 13 Serial Interface

Pin Name	Type	Description
SDA (MICRODATA[0])	I/O	This is the bi-directional data pin of the I2C (TM) compatible serial interface.
SCL (CS_BAR)	I	This is the clock pin of the I2C (TM) compatible interface. Since the chip is programmed to be a slave only, this is an input pin.

The I^2C compatible serial interface is configured to be a slave.

I²C Protocol

The following figure describes the I²C protocol that is implemented and timing relationship between various pins in a serial transfer. As shown, the SDA pin can change state during the low period of the SCL pin. The two exceptions to this rule occur during the start and stop conditions. During the "start" condition, SDA pin makes a high to low transition while the SCL pin is high. A low to high transition of SDA pin while SCL is high represents a "stop" condition. I²C(TM) specification requires that each transaction is in multiples of 8 serial clocks with the MSB bit transmitted first. Each 8-bit transaction is ended by the receiver sending an acknowledgment by driving the SDA pin low as shown.

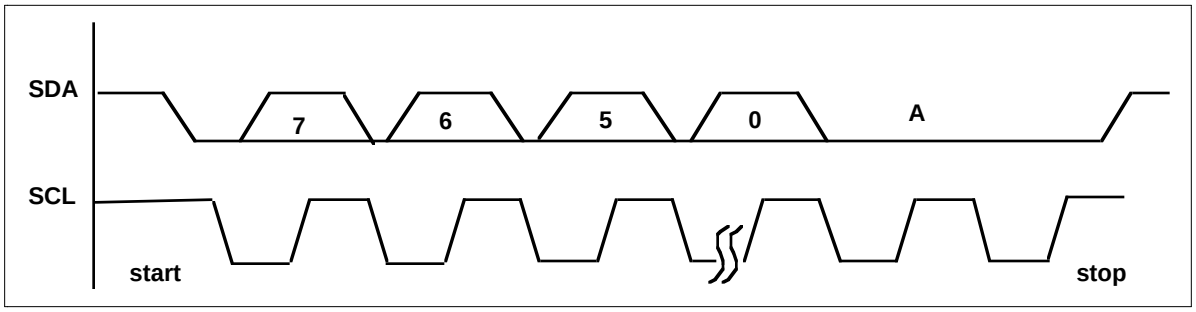

Figure 9 I²C Serial Transfer

An I²C serial transfer begins with a I²C master (usually a micro-controller) starting a new transaction. Each such transaction is composed of multiple transfers, each of which involves a 8-bit serial transfer followed by an acknowledgment from the receiver, as described in the previous paragraph. The first serial transfer in a transaction involves the I²C master broadcasting a 7-bit I²C device address over the bus. The 8th bit of this transfer indicates the direction of subsequent transfers. A "1" indicates that the I²C master wants to read from a slave device and a "0" indicates that the I²C master wants to write to a slave device. The addressed device sends an acknowledgment if it is available. A typical transaction is shown in figure 4. The address byte (7 bits of address and read/write bit) is referred to as byte A. Subsequent data bytes are referred to as D0 to Dn. This terminology is used in all subsequent discussions.

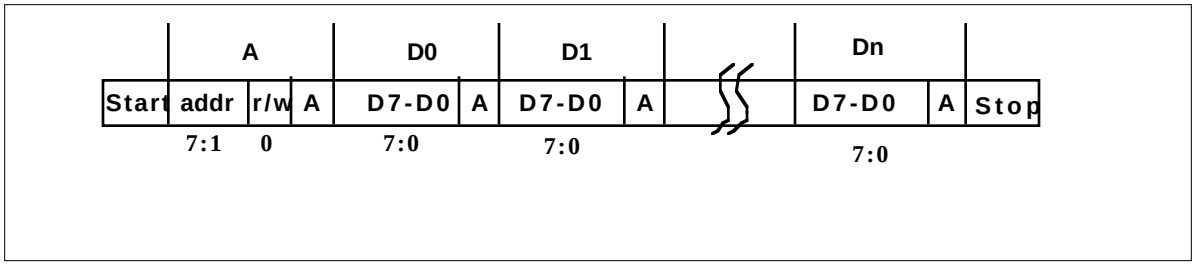

Figure 10 I²C Address and Data Protocol

Programming Protocol

I^2C is a serial transfer protocol that specifies how bytes of data are transferred over a serial interface. However the interpretation of what these bytes mean and the specification of the order in which they are sent is unique to each system.

The HD49429F uses the I^2C bus to allow an external controller to access its on-chip registers. The on-chip registers are accessed using the address pointer register. A transaction can contain an arbitrary number of byte transfers. The direction of the transfer is set by the read/write bit (bit 0 in byte A).

Write Transactions: A transaction is determined to be a write transaction when bit A[0] equals "0". During a write transaction, data is written to HD49429F on-chip registers by the I^2C master. The 7 LSBs of the 1st data byte (D0) are written to the address pointer register. We will refer to this address as A0. Byte D1 is written to register A0, byte D2 is written to register A0 + 1 and so on.

Read Transactions: A transaction is determined to be a read transaction when bit A[0] equals "1". During a read transaction, data is read from HD49429F on-chip registers by the I^2C master. During the first data transaction, the 7 LSBs of data byte D1 read from HD49429F represent the contents of the address pointer register. We will refer to this address location as A0. Byte D1 represents data from register at location A0, byte D2 represents data from location A0 + 1 and so on.

The following table specifies the semantics.

Table 14 HD49429F Serial Protocol Specification

Byte Name	Specification (Write)	Specification (read)
A	This is the address byte with following specification A[7:1] : IIC slave address	
	A[0] = 0	A[0] = 1
D0	Byte is written to address pointer register and points to register A0.	Byte is read from address pointer register and points to register A0
D1	Byte is written to register at address A0	Byte is read from register at address A0
D2	Byte is written to register at address (A0 + 1)	Byte is read from register at address (A0 + 1)
D3	Byte is written to register at address (A0 + 2)	Byte is read from register at address (A0 + 2)
Dn	Byte is written to register at address (A0 + n - 1)	Byte is read from register at address (A0 + n - 1)

Electrical Specifications

Following are electrical specifications:

- Operating Voltage: 3.3v +/- 10%
- Operating Current: 360 ma max.
- Power Dissipation: 1W max.

DC Characteristics

Table 15 Absolute Maximum Ratings

Parameter	Abs Maximum
Supply Voltage	4 V
Input Voltage	-0.3 ~ VDD+0.3 V.
Operating Temperature	0 ~70° C
Storage Temperature	125° C

AC Characteristic

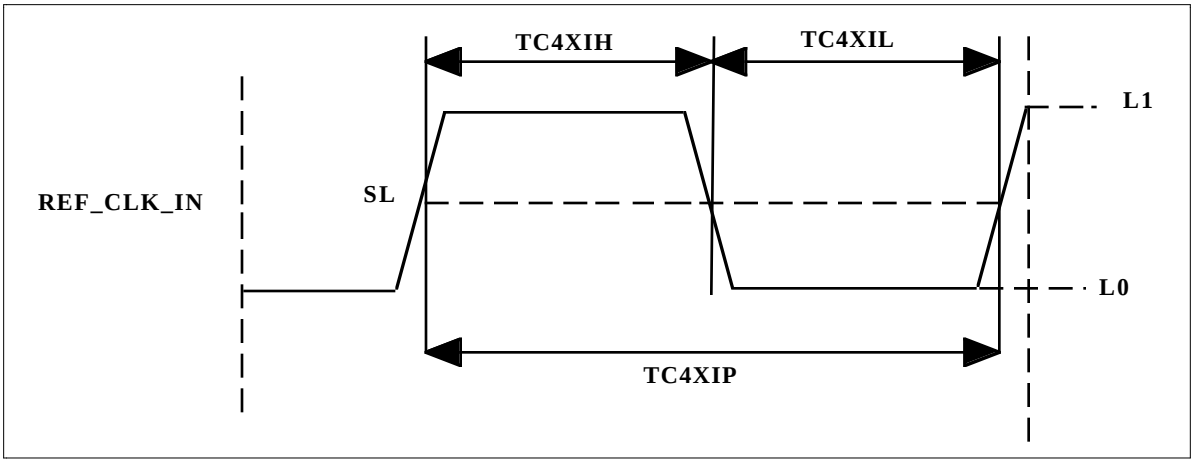

Figure 11 Clock Inputs

Table 16 Clock Inputs

Sym	PIN	Min	Typ	Max	U	Test Conditions[2]	Description
TC4XIP	REF_CLK_IN[1]	49			ns	SL= 0.5Vdd L1 = 0.7Vdd	REF_CLK_IN Period
TC4XIH	REF_CLK_IN	15			ns	L0 = 0.3Vdd	REF_CLK_IN HighTime
TC4XIL	REF_CLK_IN	15			ns		REF_CLK_IN LowTime

Note: 1. This specification applies when an external clock is input. Normally, a crystal may be used.

2. This specification assumes the MCNS clock rate. Delays will proportionately increase if a slower clock is employed.

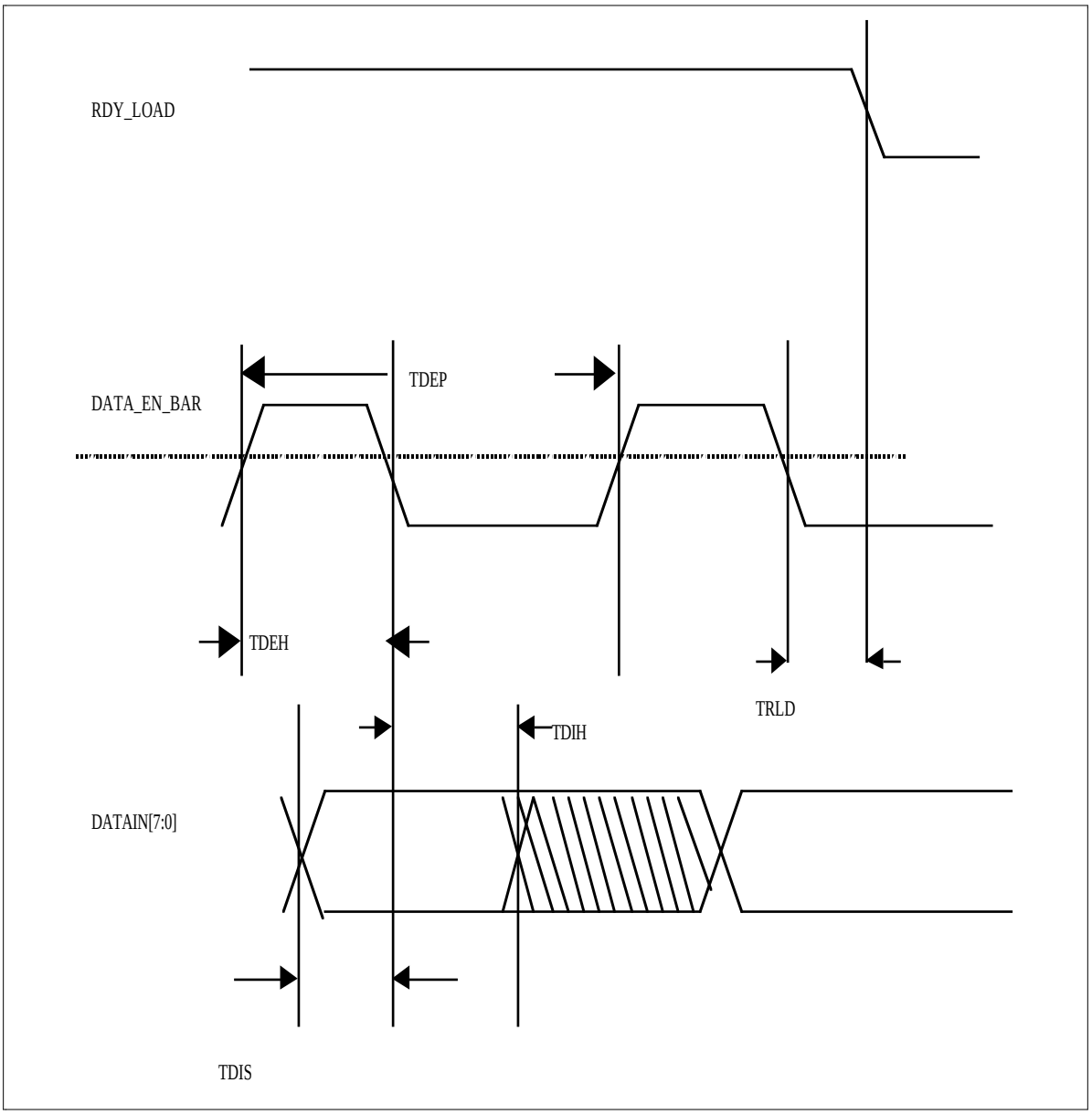

Figure 12 DATAIN Timing

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TDEH	DATA_EN_BAR	50			ns	SL= 0.5Vdd L1 = 0.7Vdd L0=0.3Vdd	Hi time of DATA_EN_BAR input.
TDEP	DATA_EN_BAR	200			ns		Period of DATA_EN_BAR signal
TDIS	DATAIN[7:0]	25			ns	SL=0.5Vdd Cload=100pf Rpullp = 1K	Setup time of DATAIN[7:0] wrt DATA_EN_BAR falling edge
TDIH	DATAIN[7:0]	50			ns	Rpullup = 1K	hold time of DATAIN[7:0] wrt DATA_EN_BAR falling edge
TRLD	RDY_LOAD			100	ns	SL= 0.5Vdd L1 = 0.7Vdd L0=0.3Vdd	Delay between de-assertion of RDY_LOAD SIGNAL and DATA_EN_BAR falling edge corresponding to the byte theat fills the buffer.

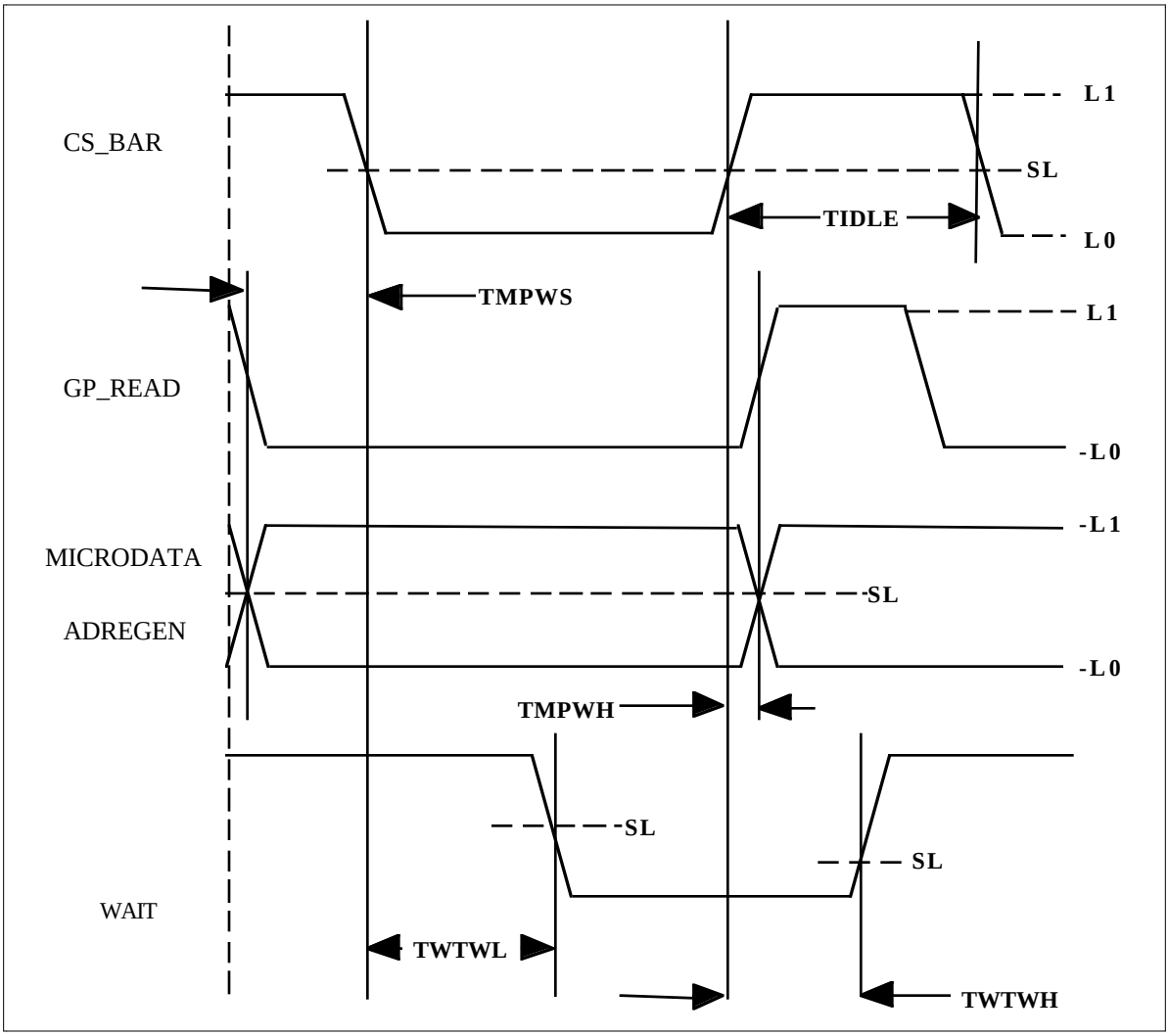

Figure 13 Microprocessor Write Cycle

Table 17 Microprocessor Write Cycle

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TMPWS	MICRODATA[7:0] ADREGEN GP_READ	TC4XIP			ns	SL= 0.5Vdd L1 = 0.7Vdd L0=0.3Vdd	Setup Time of GP_READ,ADREGEN, and MICRODATA[7:0] wrt CS_BAR.
TMPWH	MICRODATA[7:0] ADREGEN GP_READ	TC4XIP			ns		Hold Time of GP_READ,ADREGEN, and MICRODATA[7:0] wrt CS_BAR.
TWTWL	READY_BAR			TC4XIP *2 + 18	ns	SL=0.5Vdd Cload=100pf Rpullp = 1K	Delay from falling edge of CS_BAR to falling edge of READY_BAR.
TWTWH	READY_BAR			10	ns	Rpullup = 1K	Delay from rising edge of CS_BAR to rising edge of READY_BAR.
TIDLE	CS_BAR	TC4XIP *2			ns	SL= 0.5Vdd L1 = 0.7Vdd L0=0.3Vdd	Delay between consecutive microprocessor transactions.

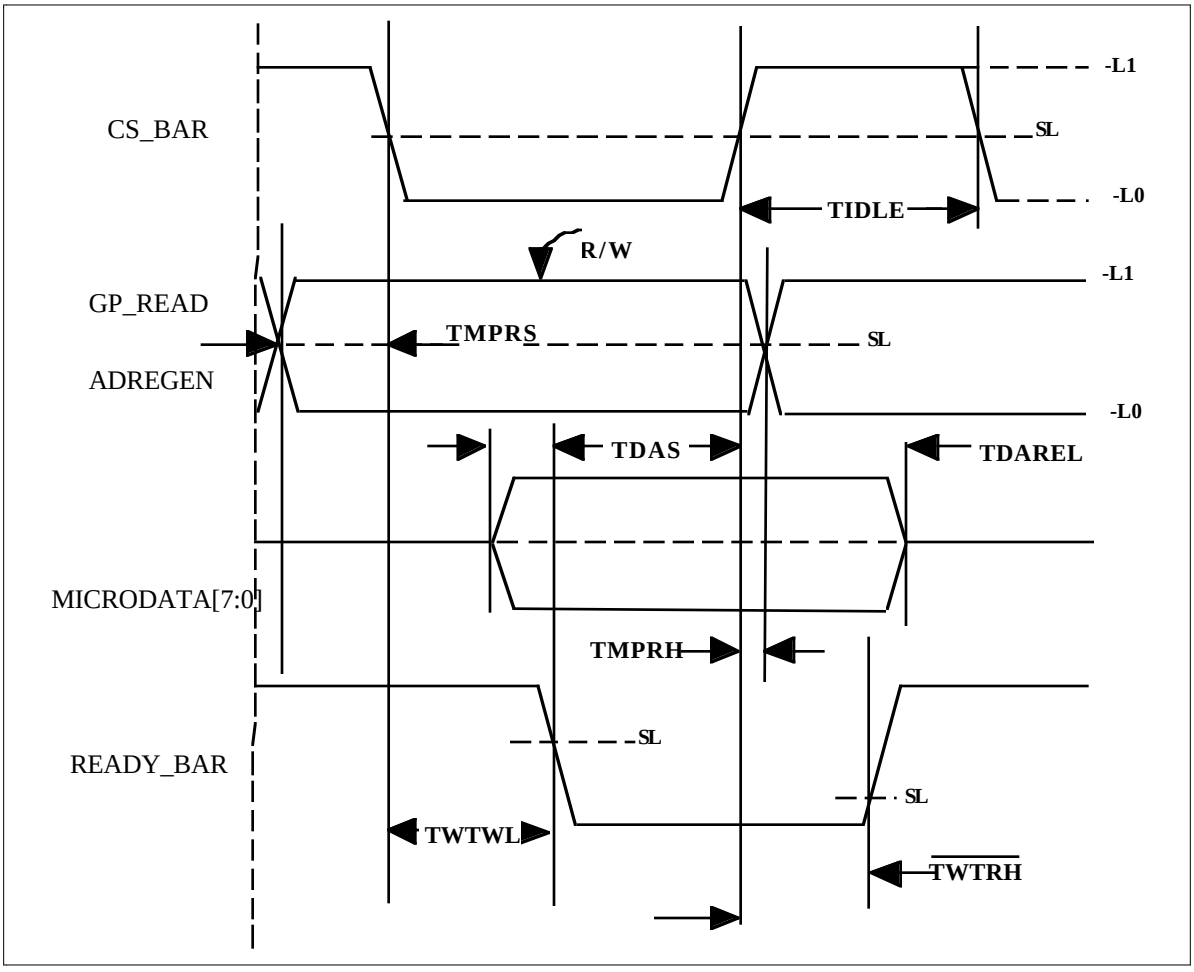

Figure 14 Microprocessor Read Cycle

Table 18 Microprocessor Read Cycle

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TMPRS	ADREGEN GP_READ	TC4XIP			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Setup Time of GP_READ,ADREGEN, and MICRODATA[7:0] wrt CS.
TMPRH	ADREGEN GP_READ	TC4XIP			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Hold Time of GP_READ,ADREGEN, and MICRODATA[7:0] wrt CS.
TWTRL	READY_BAR			TC4XIP *6+ 18	ns	SL=0.5Vdd Cload=100pf Rpullup=1K	Delay from falling edge of CS_BAR to falling edge of READY_BAR.
TWTRH	READY_BAR			10	ns	SL=0.5V Cload=100pf Rpullup=1K	Delay from rising edge of CS_BAR to rising edge of READY_BAR.
TDAS	MICRODATA[7:0]	0			ns	SL=0.5V Cload=100pf	Setup time of DATA[7:0] wrt falling edge of READY_BAR.
TDAREL	MICRODATA[7:0]	10			ns	SL=0.5V Cload=100pf	Delay between rising edge of CS_BAR and tristating of MICRODATA
TIDLE	CS_BAR	TC4XIP *2			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Delay between consecutive microprocessor transactions.

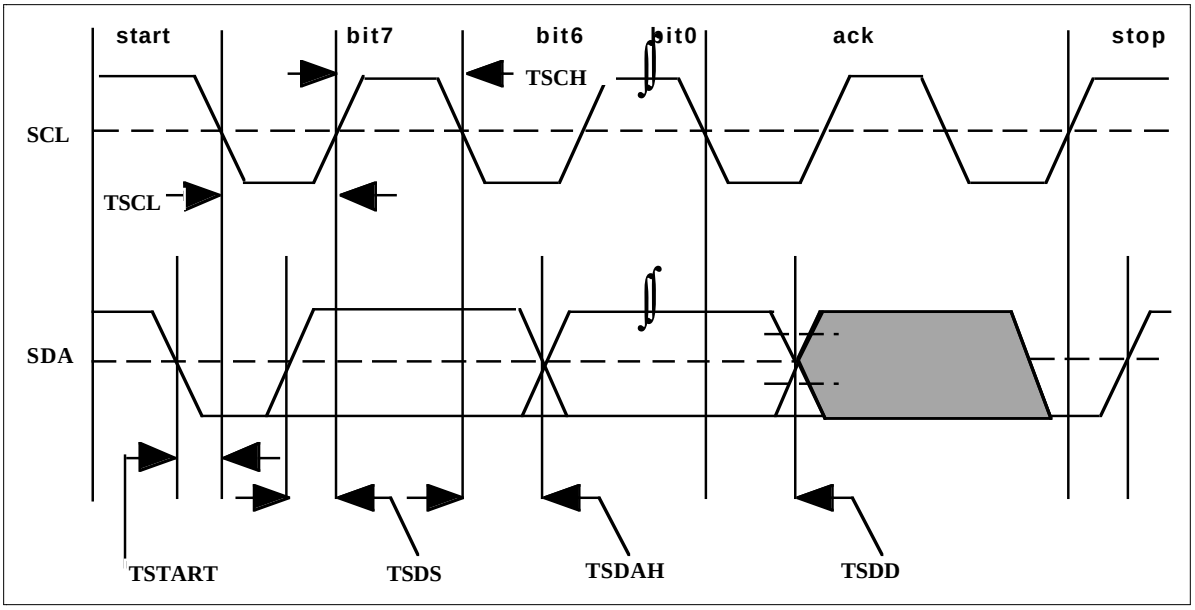

Figure 15 I²C Interface

Table 19 I^2C Interface Timing

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TSTART	CS_BAR (SCL)	60			ns	SL= 0.5Vdd L1=0.7Vdd L0=0.3Vdd	Setup time of SDA falling edge(start) with respect to falling edge of SCL.
TSTOP	MICRODATA(0) (SDA)	60			ns		Setup time of SCL rising edge wrt rising edge of SDA(stop).
TSCL	CS_BAR (SCL)	120			ns		Low time of SCL clock pulse.
TSCH	CS_BAR (SCL)	120			ns		High time of SCL clock pulse.
TSDS	MICRODATA(0) (SDA)	60			ns		Setup time of SDA wrt rising edge of SCL.
TSDH	MICRODATA(0) (SDA)	30			ns		Hold time of SDA wrt falling edge of SCL.
TSDD	MICRODATA(0) (SDA)	80			ns	SL=0.5V (0-1 Transition) SL+0.5Vdd (1-0 Transition) Rpullup=1K CLoad=100pf	Delay from falling edge of SCL to SDA valid when HD49430F is driving SDA (eg acknowledge on write).

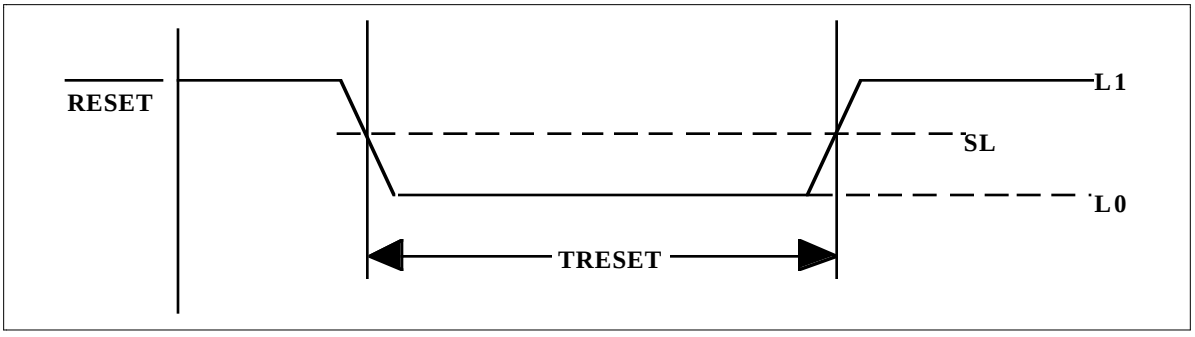

Figure 16 Reset

Table 20 Reset

Sym	Pin	Min	Typ	Max	U	Test Conditions	Description
TRESET	RESET_BAR	TC4XIP	*10		ns	SL=0.5Vdd L1=0.7Vdd L0= 0.3Vdd	Low time of RESET_BAR signal

Package and Mechanical Specifications

HD49429F is packaged in a low cost 100-pin PQFP package.

System Implementation

TBD