
HD74ALVC162334

16-bit Universal Bus Driver with 3-state Outputs

HITACHI

ADE-205-205A (Z)

2nd. Edition

December 1999

Description

This HD74ALVC162334 is a 16-bit universal bus driver is designed for 2.3 V to 3.6 V V_{CC} operation.

Data flow from A to Y is controlled by the output enable ($\overline{OE}$) input. The device operates in the transparent mode when the latch enable ($\overline{LE}$) input is low. When $\overline{LE}$ is high, the A data is latched if the clock (CLK) input is held at a high or low logic level. If $\overline{LE}$ is high, the A data is stored in the latch/flip flop on the low to high transition of CLK. When $\overline{OE}$ is high, the outputs are in the high impedance state.

To ensure the high impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver.

All outputs, which are designed to sink up to 12 mA, include equivalent 26 Ω resistors to reduce overshoot and undreshoot.

Features

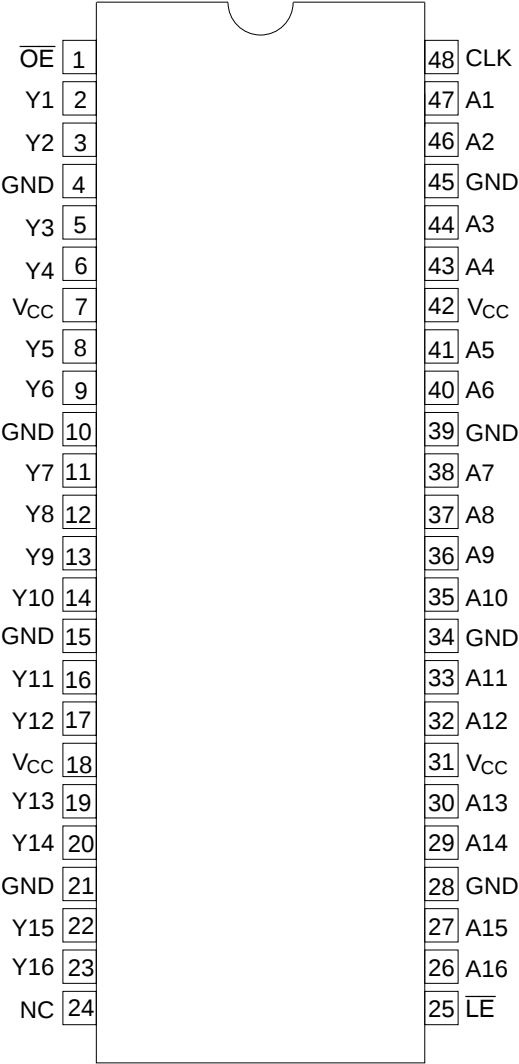
- $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$
- Typical V_{OL} ground bounce $< 0.8 \text{ V}$ ($@V_{CC} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.0 \text{ V}$ ($@V_{CC} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- High output current $\pm 12 \text{ mA}$ ($@V_{CC} = 3.0 \text{ V}$)
- All outputs have equivalent 26 Ω series resistors, so no external resistors are required

Function Table

Inputs				Output Y
OE	LE	CLK	A	
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y ₀ ^{*1}

H : High level
L : Low level
X : Immaterial
Z : High impedance
↑ : Low to high transition
Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC}	−0.5 to 4.6	V	
Input voltage ^{*1}	V _I	−0.5 to 4.6	V	
Output voltage ^{*1, 2}	V _O	−0.5 to V _{CC} +0.5	V	
Input clamp current	I _{IK}	−50	mA	V _I < 0
Output clamp current	I _{OK}	±50	mA	V _O < 0 or V _O > V _{CC}
Continuous output current	I _O	±50	mA	V _O = 0 to V _{CC}
V _{CC} , GND current / pin	I _{CC} or I _{GND}	±100	mA	
Maximum power dissipation at Ta = 55°C (in still air) ^{*3}	P _T	0.85	W	TSSOP
Storage temperature	T _{stg}	−65 to 150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

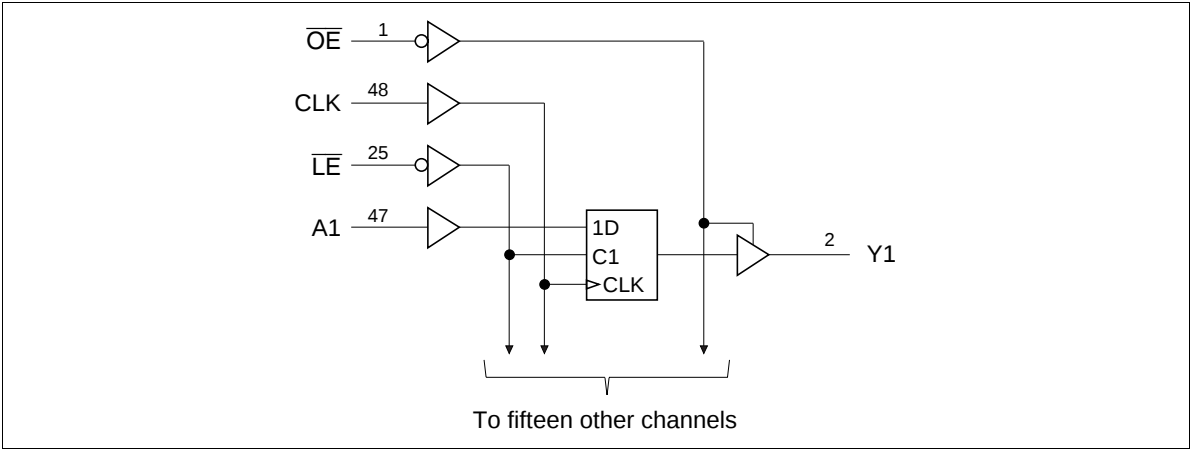
- 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- 2. This value is limited to 4.6 V maximum.
- 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V _{CC}	2.3	3.6	V	
Input voltage	V _I	0	V _{CC}	V	
Output voltage	V _O	0	V _{CC}	V	
High level output current	I _{OH}	—	−6	mA	V _{CC} = 2.3 V
		—	−8		V _{CC} = 2.7 V
		—	−12		V _{CC} = 3.0 V
Low level output current	I _{OL}	—	6	mA	V _{CC} = 2.3 V
		—	8		V _{CC} = 2.7 V
		—	12		V _{CC} = 3.0 V
Input transition rise or fall rate	Δt / Δv	0	10	ns / V	
Operating temperature	T _a	−40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



Electrical Characteristics (Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Max	Unit	Test Conditions
Input voltage	V _{IH}	2.3 to 2.7	1.7	—	V	
		2.7 to 3.6	2.0	—		
	V _{IL}	2.3 to 2.7	—	0.7		
		2.7 to 3.6	—	0.8		
Output voltage	V _{OH}	2.3 to 3.6	V _{CC} -0.2	—	V	I _{OH} = -100 μA
		2.3	1.9	—		I _{OH} = -4 mA, V _{IH} = 1.7 V
		2.3	1.7	—		I _{OH} = -6 mA, V _{IH} = 1.7 V
		3.0	2.4	—		I _{OH} = -6 mA, V _{IH} = 2.0 V
		2.7	2.0	—		I _{OH} = -8 mA, V _{IH} = 2.0 V
		3.0	2.0	—		I _{OH} = -12 mA, V _{IH} = 2.0 V
	V _{OL}	2.3 to 3.6	—	0.2		I _{OL} = 100 μA
		2.3	—	0.4		I _{OL} = 4 mA, V _{IL} = 0.7 V
		2.3	—	0.55		I _{OL} = 6 mA, V _{IL} = 0.7 V
		3.0	—	0.55		I _{OL} = 6 mA, V _{IL} = 0.8 V
		2.7	—	0.6		I _{OL} = 8 mA, V _{IL} = 0.8 V
		3.0	—	0.8		I _{OL} = 12 mA, V _{IL} = 0.8 V
Input current	I _{IN}	3.6	—	±5	μA	V _{IN} = V _{CC} or GND
Off state output current	I _{OZ}	3.6	—	±10	μA	V _{OUT} = V _{CC} or GND
Quiescent supply current	I _{CC}	3.6	—	40	μA	V _{IN} = V _{CC} or GND
	ΔI _{CC}	3.0 to 3.6	—	750	μA	V _{IN} = one input at (V _{CC} -0.6) V, other inputs at V _{CC} or GND

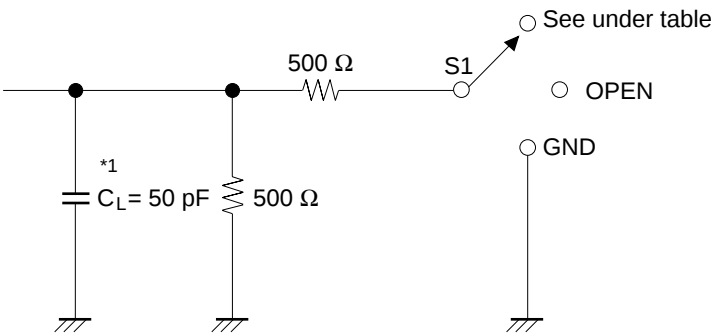
Switching Characteristics (Ta = −40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)		
Maximum clock frequency	f _{max}	2.5±0.2	150	—	—	MHz				
		2.7	150	—	—					
		3.3±0.3	150	—	—					
Propagation delay time	t _{PLH}	2.5±0.2	1.0	—	3.9	ns	A	Y		
		2.7	—	—	4.5					
		3.3±0.3	1.1	—	3.9					
	t _{PHL}	2.5±0.2	1.0	—	5.0		$\overline{\text{LE}}$	Y		
		2.7	—	—	6.0					
		3.3±0.3	1.3	—	5.0					
		2.5±0.2	1.0	—	4.9		CLK	Y		
		2.7	—	—	5.4					
		3.3±0.3	1.0	—	4.9					
Output enable time	t _{ZH}	2.5±0.2	1.0	—	5.4	ns	$\overline{\text{OE}}$	Y		
		2.7	—	—	6.4					
		3.3±0.3	1.1	—	5.4					
Output disable time	t _{HZ}	2.5±0.2	1.0	—	4.7	ns	$\overline{\text{OE}}$	Y		
		2.7	—	—	5.1					
		3.3±0.3	1.7	—	5.0					
Input capacitance	C _{IN}	3.3	—	5.5	—	pF	Control inputs			
		3.3	—	6.0	—		Data inputs			
Output capacitance	C _O	3.3	—	8.0	—	pF	Outputs			

Switching Characteristics (Ta = -40 to 85°C) (cont)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t _{su}	2.5±0.2	1.4	—	—	ns	Data before CLK↑
		2.7	1.7	—	—		
		3.3±0.3	1.5	—	—		
		2.5±0.2	1.2	—	—		Data before $\overline{LE}$ ↑
		2.7	1.6	—	—		CLK "H"
		3.3±0.3	1.3	—	—		
		2.5±0.2	1.4	—	—		Data before $\overline{LE}$ ↑
		2.7	1.5	—	—		CLK "L"
		3.3±0.3	1.2	—	—		
Hold time	t _h	2.5±0.2	0.9	—	—	ns	Data after CLK↑
		2.7	0.8	—	—		
		3.3±0.3	0.9	—	—		
		2.5±0.2	1.1	—	—		Data after $\overline{LE}$ ↑
		2.7	1.1	—	—		CLK "H" or "L"
		3.3±0.3	1.1	—	—		
Pulse width	t _w	2.5±0.2	3.3	—	—	ns	$\overline{LE}$ "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		
		2.5±0.2	3.3	—	—		CLK "H" or "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		

Test Circuit

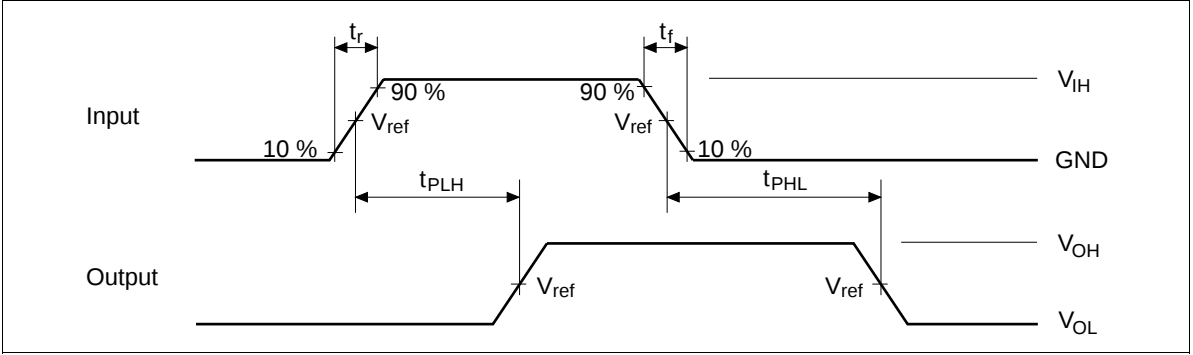


Load Circuit for Outputs

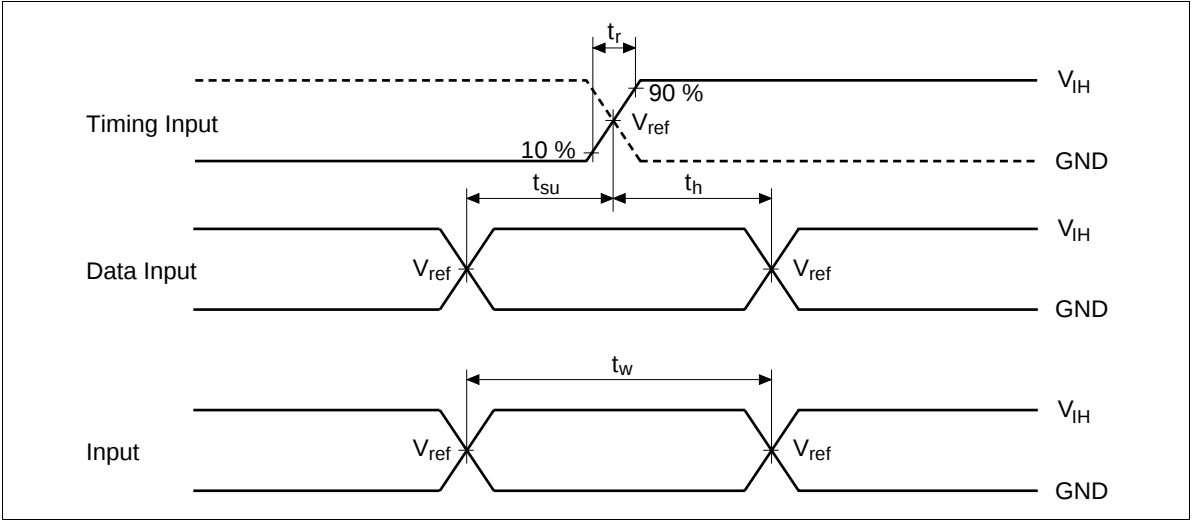
Symbol	V _{CC} =2.5±0.2V	V _{CC} =2.7V, 3.3±0.3V
t _{PLH} /t _{PHL}	OPEN	OPEN
t _{su} /t _h /t _w		
t _{ZH} /t _{HZ}	GND	GND
t _{ZL} /t _{LZ}	2 × V _{CC}	6.0 V

Note: 1. C_L includes probe and jig capacitance.

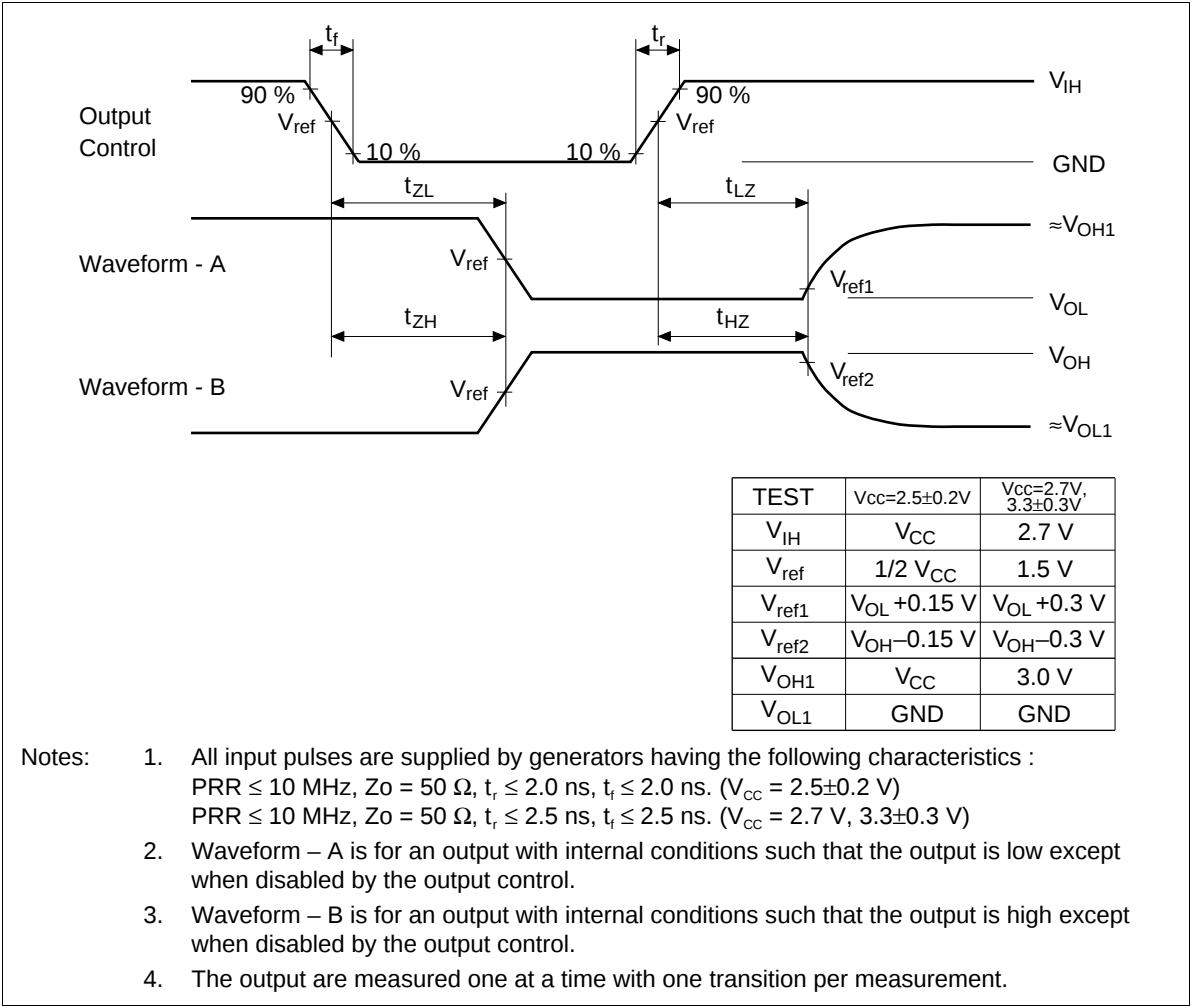
Waveforms – 1



Waveforms – 2

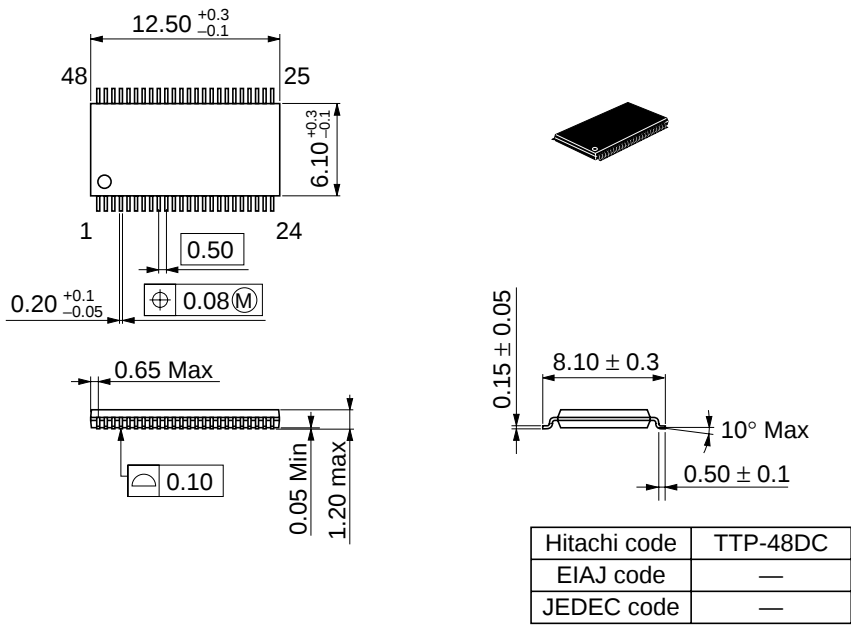


Waveforms – 3



Package Dimensions

Unit : mm



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