Agilent Technologies
Innovating the HP Way

1.5 – 2.5 GHz LNA Switch PA

Technical Data

HPMX-3003

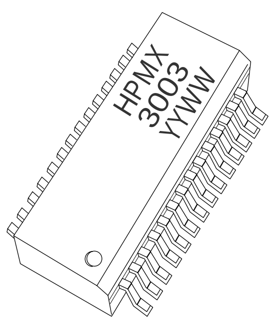
Features

- **GaAs MMIC LNA-Switch-Power Amp for 1.5 – 2.5 GHz Transceiver Use**
- **LNA: 2.2 dB NF, 13 dB G_a @ 1.9 GHz**
- **Switch: 55 dBm OIP @ 1.9 GHz**
- **Power Amp: +4 dBm in, +27.5 dBm out, 23.5 dB Gain, 35% η_{add} @ 1.9 GHz**
- **3 or 5 V Operation**
- **JEDEC Standard SSOP-28 Surface Mount Package**

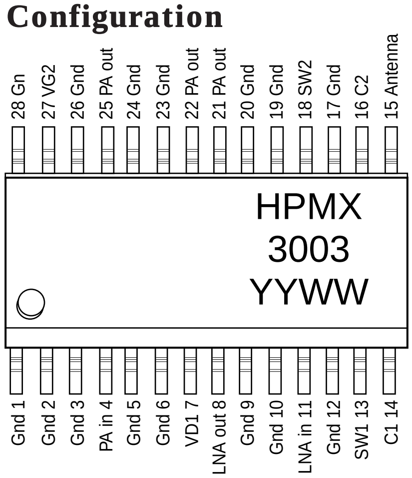
Applications

- **Personal Communications Systems (PCS)**
- **Cordless Telephone Systems**
- **2400 MHz Wireless LANs and ISM Band Spread Spectrum Applications**

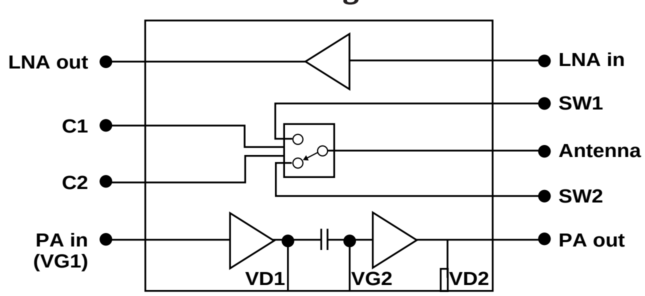
Plastic SSOP-28



Package Pin Configuration



Functional Block Diagram



Description

Agilent's HPMX-3003 combines a Low Noise Amplifier, GaAs MMIC switch, and 27.5 dBm power amp in a single miniature 28 lead surface mount plastic package. This RFIC would typically serve as the "front end" and power stage of a battery operated wireless transceiver for PCS or ISM band use. Each section of the RFIC can also be used independently.

The single-supply LNA makes use of the low noise characteristics of GaAs to create a matched, broad-band amplifier with target performance of 13 dB gain and 2.2 dB noise figure. The switch provides +55 dBm IP3 for linear operation. The power amplifier produces up to 820 mW with 35% power added efficiency.

The HPMX-3003 is fabricated with Agilent's GaAs MMIC process, and features a nominal 0.5 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to produce MMICs with superior performance, uniformity and reliability.

HPMX-3003 Absolute Maximum Ratings[1]

Symbol	Parameter	Units	Absolute Maximum[1] LNA	Absolute Maximum[1] Switch	Absolute Maximum[1] Power Amp
P_{diss}	Power Dissipation[2,3]	mW	250[2,3]		1500[2,3]
P_{in}	CW RF Input Power	dBm	+20	+33	+20
V_d	Device Voltage	V	8	—	8
V_{cont}	Control Voltage	V	—	-6	—
T_{ch}	Channel Temperature	°C	175	175	175
T_{STG}	Storage Temperature	°C	-65 to 150	-65 to 150	-65 to 150

Notes:
1. Operation of this device above any of these limits may cause permanent damage.
2. T_{case} = 25°C
3. Derate at 18.2 mW/°C for T_C > 78°C

Thermal Resistance[2]:
θ_{jc} = 55°C/W

Recommended operating range of V_{cc} = 2.7 to 5.5 V, T_a = -40 to + 85 °C

HPMX-3003 Standard Test Conditions

Unless otherwise stated, all test data was taken on packaged parts under the following conditions:

T_a= 25 °C, Z_o = 50 Ω

V_{cc} = +3.0 V DC, $V_{control}$ = -3.0 V DC, V_{D1} = +3.6 V DC

LNA P_{in} = -20 dBm, PA P_{in} = +4 dBm, frequency = 1.9 GHz

Perfomance cited is performance in test circuit shown in Figure 17.

HPMX-3003 Guaranteed Electrical Specifications

Standard test conditions apply unless otherwise noted.

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
G_{test}	LNA gain through switch	dB	9.0	11	
P_{out}	Output power through switch	dBm	24.0	25.5	
I_d LNA	LNA bias current	mA		6.5	9.5

HPMX-3003 Summary Characterization Information

Standard test conditions apply unless otherwise noted. All information tested in 1900 MHz Test Circuit, and reflects performance of test circuit at 1900 MHz.

Symbol	Parameters and Test Conditions	Units	Typ
LNA			
NF	Noise Figure	dB	2.2
$\|S_{21}\|^2$	50 Ω Gain	dB	13
IRL	Input Return Loss	dB	15
ORL	Output Return Loss		12
IIP_3	Input Third Order Intercept	dBm	-1
Switch			
P_{1dB}	Output Power where insertion loss is increased by 1 dB — ΔC1 to C2 = 3 V	dBm	+23
P_{1dB}	Output Power where insertion loss is increased by 1 dB[1] — ΔC1 to C2 = 5 V	dBm	+29
IP_3	Third Order Intercept	dBm	+55
S_{21} on	Insertion Loss, on channel	dB	0.8
S_{21} off	Isolation, off channel	dB	15
IRL_{on}	Return Loss, on channel	dB	26
IRL_{off}	Return Loss, off channel	dB	0.5
Power amp (Vg = -.8 V required)			
GP	Gain — V_{D1} = 3.6 V, P_{in} = +4 dBm	dB	23.5
η_{PAadd}	Power Added Efficiency — V_{D1} = 3.6 V	%	35
P_{out}	Output Power — V_{D1} = 3.6 V, P_{in} = +4 dBm	dBm	+27.5
I_d PA	Transmit Current — V_{D1} = 3.6 V, P_{in} = +4 dBm	mA	450

Note:
1. The P_{1dB} of the switch can be improved by increasing the difference between the values of C1 and C2 from the normal 3 V (+23 dB P_{1dB}) to 5 V (+29 dB P_{1dB}).

HPMX-3003 Pin Description

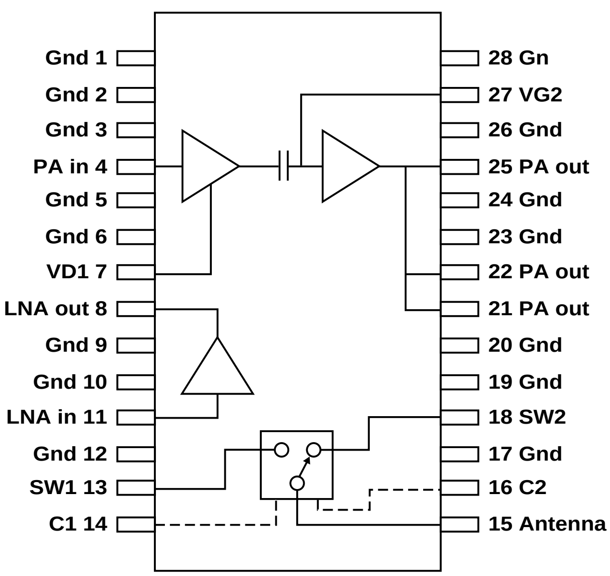


Figure 1. HPMX-3003 Pin Outs and Schematic.

HPMX-3003 Pin Description Table

No.	Mnemonic	Description	Typical Signal	Description
1 2 3	Gnd Gnd Gnd	ground ground ground	0 V 0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
4	PA_{in}	input to Power Amplifier	DC: -0.75 V RF: +4 dBm	Bias through 500 Ω resistor and 100 pF capacitor. 50 Ω transmission line with DC blocking capacitor (>24 pF) to input. Shunt 2.7 pF used on test board to match input at 1.9 GHz.
5 6	Gnd Gnd	ground ground	0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
7	VD1	Drain bias of PA stage 1	+3 V, 100 mA	Set drain bias to 3 V (can be tied to same rail as PA out). Bypass with 100 pF capacitor at pin.
8	LNA out	output of LNA	DC: +3 V, 5 mA RF: -7 dBm	Bias through 5 nH choke (printed on PC board) and 100 pF bypass capacitor to 10 Ω resistor and 1000 pF bypass capacitor. Can be operated from 3 to 5 V supply line. 50 Ω transmission line with DC block (>24 pF) to receiver.
9 10	Gnd Gnd	ground ground	0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
11	LNA in	input of LNA	DC: 0 V RF: -20 dBm	50 Ω transmission line from switch. Input blocking capacitor (24 pF) and shunt 5 nH inductor to ground (noise match at 1.9 GHz) required. Typically a filter is employed between the LNA input and the switch.
12	Gnd	ground	0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
13	SW1	switch terminal 1	DC: 0 V RF: -20 dBm	Switch input or output. Symmetrical with SW2. 50 Ω transmission line to LNA (or PA). Line should not carry DC voltage.
14	C1	switch control 1	closed: 0 V open: -3 to -5 V	High impedance line to control switch, used in conjunction with C2. C2 should be open when C1 is closed.
15	Antenna	switch center pole	DC: 0 V RF: +26 dBm	50 Ω transmisson line to/from antenna. Line should not carry DC voltage.
16	C2	switch control 2	closed: 0 V open: -3 to -5 V	High impedance line to control switch, used in conjunction with C1. C1 should be open when C2 is closed.
17	Gnd	ground	0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
18	SW2	switch terminal 2	DC: 0 V RF: +4 dBm	Switch input or output. Symmetrical with SW1. 50 Ω transmission line to PA (or LNA). Line should not carry DC voltage.
19 20	Gnd Gnd	ground ground	0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
21 22	PA out PA out	output of PA output of PA	DC: 3 V, 350 mA RF: +27 dBm	2.7 pF chip capacitor to ground provides 1.9 GHz output match for PA. 50 Ω transmission line to switch. LC choke and blocking C used. Typically a filter is employed between the PA output and the switch input.
23 24	Gnd Gnd	ground ground	0 V 0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
25	PA out	output of PA	DC: 3 V, 350 mA RF: +27 dBm	Leave unconnected; use pins 21 & 22 for PA out.
26	Gnd	ground	0 V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.
27	VG2	Gate bias on PA stage 2	-0.75 V	Provide bias through 10 Ω resistor. Bypass to ground at pin with 10 pF capacitor, and on power supply side of resistor with 1000 pF capacitor.
28	Gnd	ground	0V	Short path with minimal parasitics. Ground pins are also the primary thermal path for heatsinking the device.

HPMX-3003 Typical Performance

Standard test conditions apply unless otherwise noted. 2.4 GHz performance is performance in test circuit shown in Figure 18. Some aspects of performance are determined by the test circuit impedances.

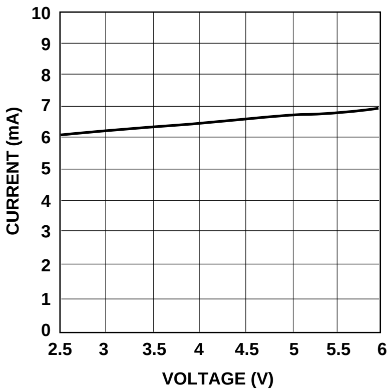


Figure 2. LNA Current vs. Device Voltage at 1900 MHz.

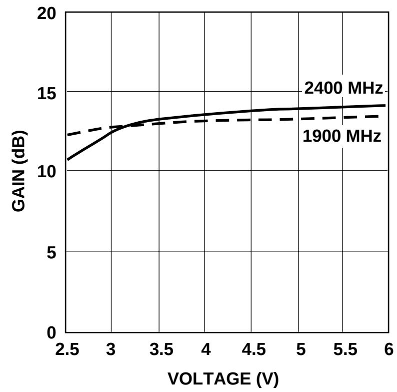


Figure 3. LNA Gain vs. Device Voltage and Frequency.

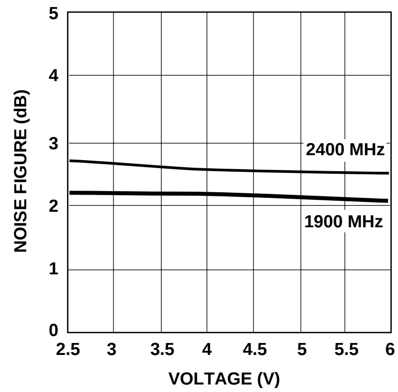


Figure 4. LNA Noise Figure vs. Device Voltage and Frequency.

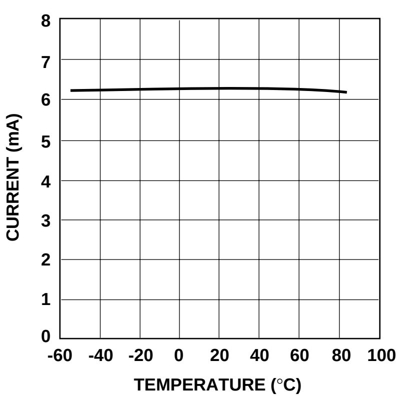


Figure 5. LNA Current vs. Temperature at 1900 MHz.

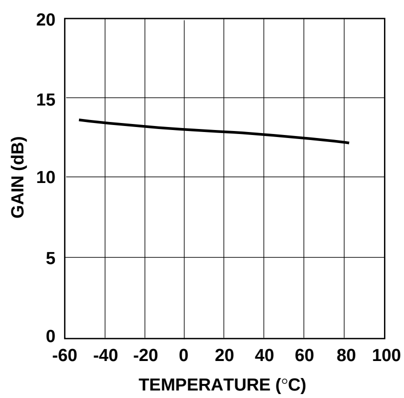


Figure 6. LNA Gain vs. Temperature at 1900 MHz.

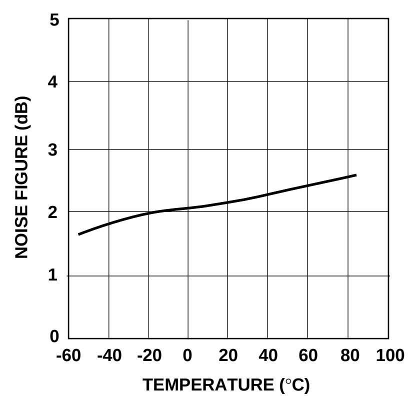


Figure 7. LNA Noise Figure vs. Temperature at 1900 MHz.

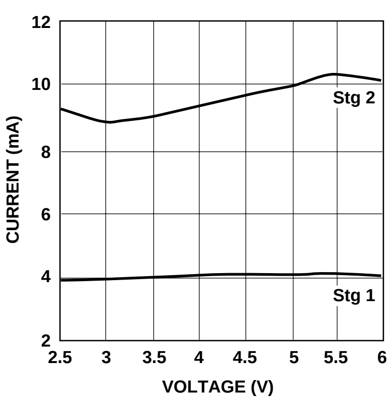


Figure 8. PA Current vs. Device Voltage at 1900 MHz.

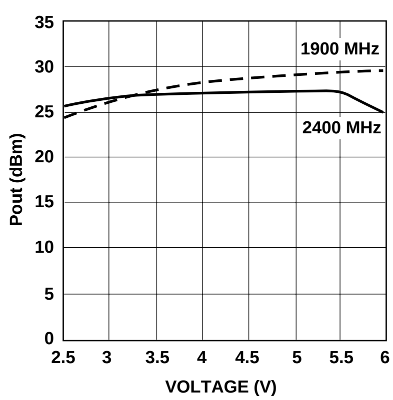


Figure 9. PA Output Power vs. Supply Voltage and Frequency.

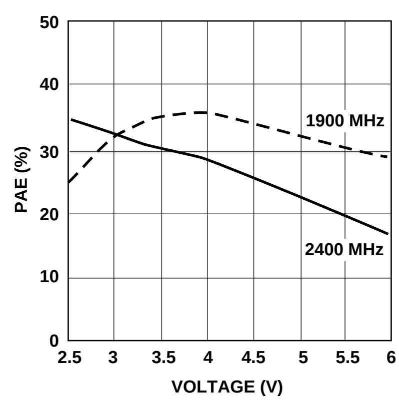


Figure 10. PA Power Added Efficiency vs. Supply Voltage and Frequency.

HPMX-3003 Typical Performance, continued

Standard test conditions apply unless otherwise noted. 2.4 GHz performance is performance in test circuit shown in Figure 18. Some aspects of performance are determined by the test circuit impedances.

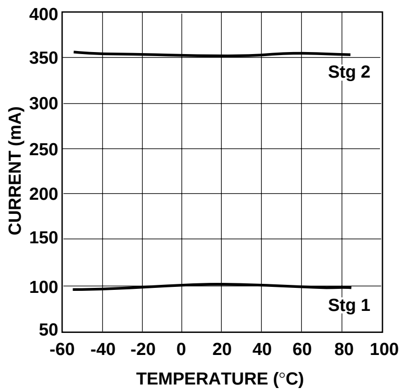


Figure 11. PA Current vs. Temperature at 1900 MHz and VD1 = 3.6 V.

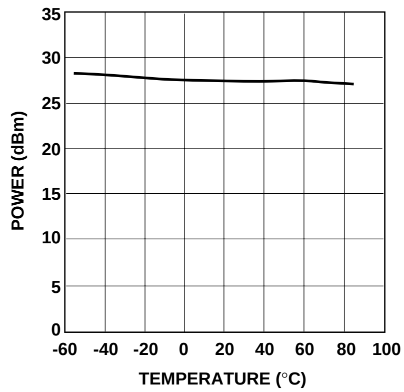


Figure 12. PA Output Power vs. Temperature at 1900 MHz and VD1 = 3.6 V.

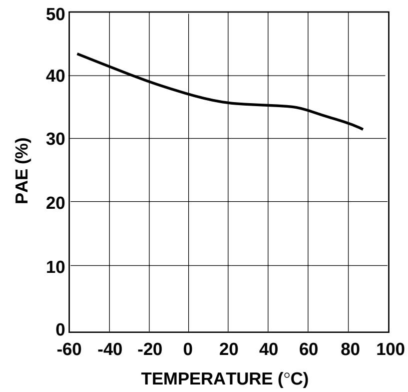


Figure 13. PA Power Added Efficiency vs. Temperature at 1900 MHz and VD1 = 3.6 V.

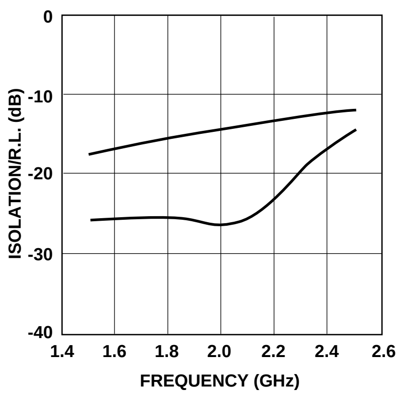


Figure 14. Switch Isolation and “ON” State Return Loss vs. Frequency.

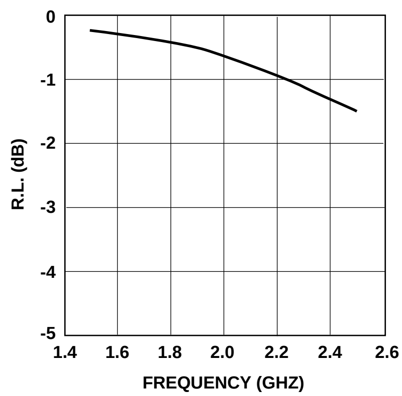


Figure 15. Switch “OFF” State Return Loss vs. Frequency.

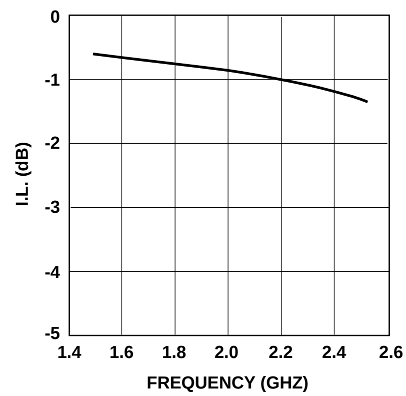


Figure 16. Switch “ON” State Insertion Loss vs. Frequency.

HPMX-3003 Typical Scattering Parameters for the LNA,

Common Source, Z_O = 50 Ω, V_D = 3 V, I_D = 5 mA

Frequency	S_{11}		S_{21}		S_{12}		S_{22}	
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
1.0	0.97	-27	2.00	158	0.035	-12	0.91	-22
1.2	0.96	-33	2.06	150	0.036	-17	0.91	-27
1.4	0.95	-40	2.13	142	0.037	-23	0.90	-31
1.6	0.94	-47	2.20	134	0.038	-30	0.88	-36
1.8	0.92	-54	2.28	125	0.038	-39	0.87	-41
2.0	0.90	-62	2.36	117	0.039	-49	0.86	-46
2.2	0.88	-70	2.45	109	0.039	-62	0.84	-50
2.4	0.85	-79	2.54	100	0.040	-77	0.83	-55
2.6	0.82	-89	2.63	90	0.042	-95	0.81	-60
2.8	0.78	-99	2.71	81	0.045	-115	0.79	-65
3.0	0.75	-110	2.79	71	0.050	-135	0.78	-71

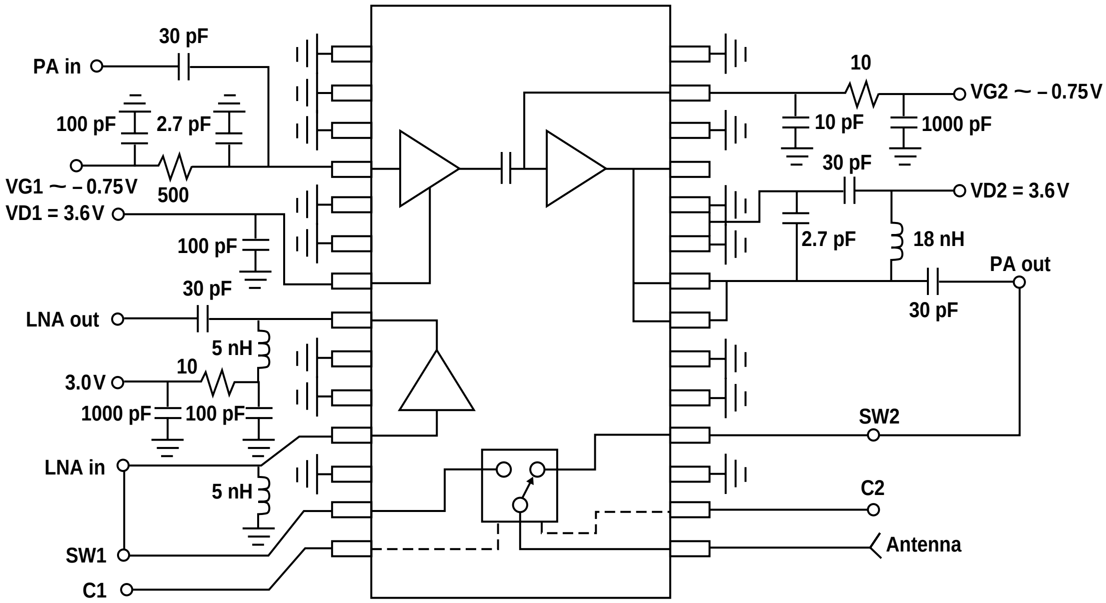


Figure 17. HPMX-3003 Test Circuit (1900 MHz).

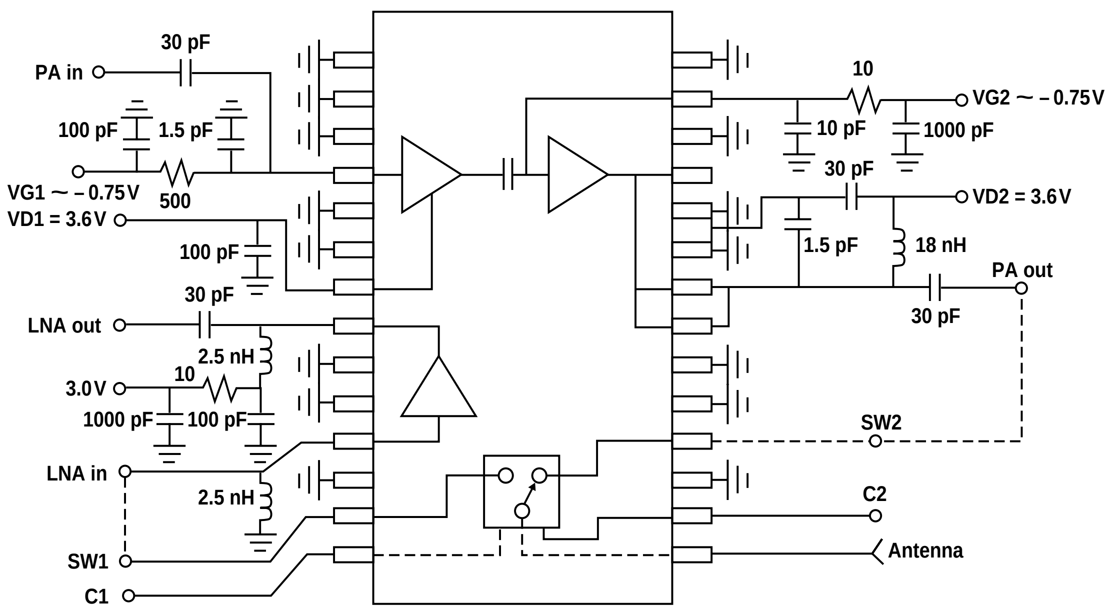


Figure 18. HPMX-3003 Test Circuit (2400 MHz).

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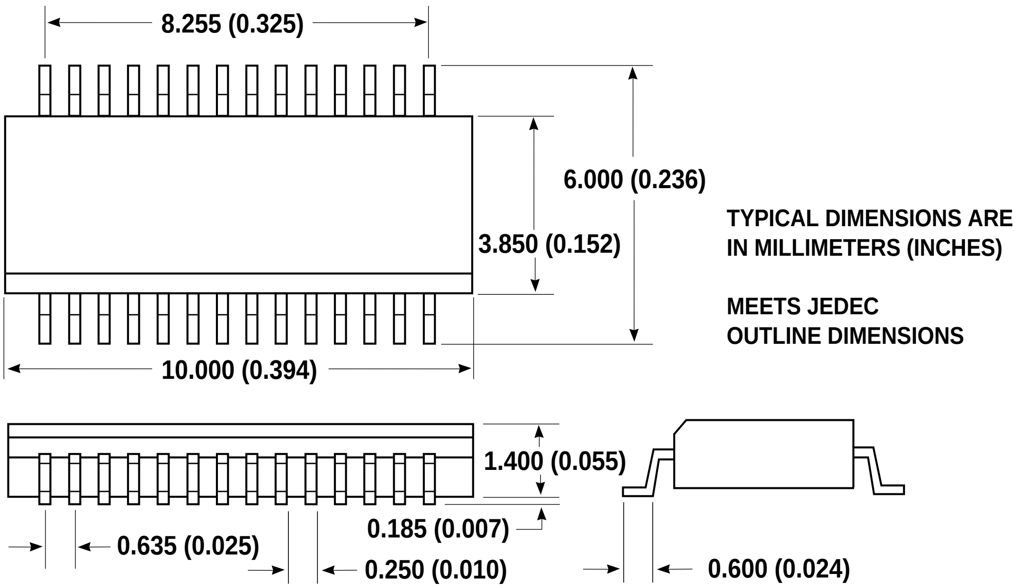
JEDEC Standard SSOP-28 Package Outline Drawing



Part Number Ordering Information

Part Number	No. of Devices	Container
HPMX-3003-TR1	1000	Tape and Reel
HPMX-3003-BLK	25	Tape

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Data subject to change.

5965-1403E (11/99)