

DESCRIPTION

The HCPL-0700 and HCPL-0701 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector housed in a compact 8-pin small outline package.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler.

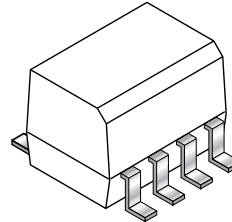
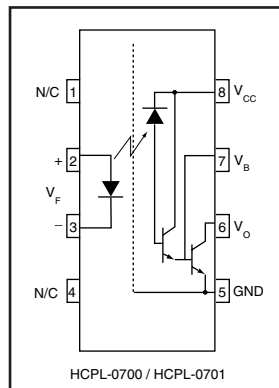
The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements.

FEATURES

- Low current - 0.5 mA
- Superior CTR-2000%
- Superior CMR-10 kV/μs
- CTR guaranteed 0-70°C
- *BSI, CSA and UL approval

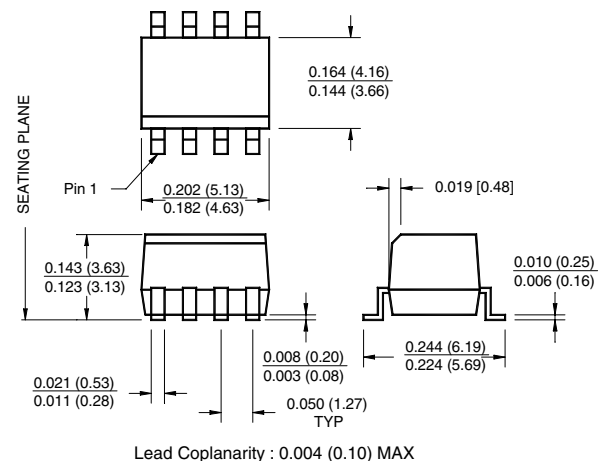
APPLICATIONS

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- μP bus isolation
- Current loop receiver



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Package Dimensions



NOTE

All dimensions are in inches (millimeters)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Value	Units
Storage Temperature	T _{STG}	-55 to +125	°C
Operating Temperature	T _{OPR}	-55 to +85	°C
Reflow Temperature Profile (Refer to fig. 11)			
EMITTER			
DC/Average Forward Input Current	I _F (avg)	20	mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	I _F (pk)	40	mA
Peak Transient Input Current - (≤ 1 μs P.W., 300 pps)	I _F (trans)	1.0	A
Reverse Input Voltage	V _R	5	V
Input Power Dissipation	P _D	35	mW
DETECTOR			
Average Output Current (Pin 6)	I _O (avg)	60	mA
Emitter-Base Reverse Voltage	V _{EBR}	0.5	V
Supply Voltage, Output Voltage	V _{CC} , V _O	-0.5 to 7	V
		-0.5 to 18	
Output power dissipation	P _D	100	mW

*Samples submitted for certification - Approval pending

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ELECTRICAL CHARACTERISTICS (T_A = 0 to 70°C unless otherwise specified.)

INDIVIDUAL COMPONENT CHARACTERISTICS

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
EMITTER							
Input Forward Voltage	T _A = 25°C	V _F	All	1.0	1.27	1.7	V
	(I _F = 1.6 mA)					1.75	
Input Reverse Breakdown Voltage	(T _A = 25°C, I _R = 10 µA)	BV _R	All	5.0	20		
Temperature coefficient of forward voltage	(I _F = 1.6 mA)	(ΔV _F /ΔT _A)	All		-1.8		mV/°C
DETECTOR							
Logic high output current	(I _F = 0 mA, V _O = V _{CC} = 18 V)	I _{OH}	HCPL-0701		0.01	100	µA
	(I _F = 0 mA, V _O = V _{CC} = 7 V)		HCPL-0700		0.01	250	
Logic low supply	(I _F = 1.6 mA, V _O = Open)	I _{CCL}	HCPL-0700		0.4	1.5	mA
	(V _{CC} = 18 V)		HCPL-0701				
Logic high supply	(I _F = 0 mA, V _O = Open)	I _{CCH}	HCPL-0700		0.05	10	µA
	(V _{CC} = 18 V)		HCPL-0701				

TRANSFER CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
COUPLED							
Current transfer ratio (Notes 1,2)	(I _F = 0.5 mA, V _O = 0.4 V, V _{CC} = 4.5 V)	CTR	HCPL-0701	400	2000	5000	%
	(I _F = 1.6 mA, V _O = 0.4 V, V _{CC} = 4.5 V)		HCPL-0701	500	1300	2600	
	(I _F = 1.6 mA, V _O = 0.4 V, V _{CC} = 4.5 V)		HCPL-0700	300	1300	2600	
Logic low output voltage output voltage (Note 2)	(I _F = 0.5 mA, I _O = 2 mA, V _{CC} = 4.5 V)	V _{OL}	HCPL-0701		0.05	0.4	V
	(I _F = 1.6 mA, I _O = 8 mA, V _{CC} = 4.5 V)				0.10	0.4	
	(I _F = 5 mA, I _O = 15 mA, V _{CC} = 4.5 V)				0.13	0.4	
	(I _F = 12 mA, I _O = 24 mA, V _{CC} = 4.5 V)				0.20	0.4	
	(I _F = 1.6 mA, I _O = 4.8 mA, V _{CC} = 4.5 V)		HCPL-0700		0.08	0.4	

ISOLATION CHARACTERISTICS (T_A = 0 to 70°C Unless otherwise specified)

Characteristics	Test Conditions	Symbol	Min	Typ**	Max	Unit
Input-output insulation leakage current	(Relative humidity = 45%) (T _A = 25°C, t = 5 s) (V _{I-O} = 3000 VDC) (Note 4)	I _{I-O}			1.0	µA
Withstand insulation test voltage	(RH ≤ 50%, T _A = 25°C) (Note 4, 5) (t = 1 min.)	V _{ISO}	2500			V _{RMS}
Resistance (input to output)	(Note 4) (V _{I-O} = 500 VDC)	R _{I-O}		10 ¹²		Ω

** All typicals at T_A = 25°C

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SWITCHING CHARACTERISTICS ($T_A = 0$ to 70°C unless otherwise specified., $V_{CC} = 5\text{ V}$)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
Propagation delay time to logic low (Note 2) (Fig. 13)	$(R_L = 4.7\text{ k}\Omega, I_F = 0.5\text{ mA})$ $T_A = 25^\circ\text{C}$	T_{PHL}	HCPL-0701		4	30 25	μs
	$(R_L = 270\ \Omega, I_F = 12\text{ mA})$ $T_A = 25^\circ\text{C}$		HCPL-0701		0.2	2 1	
	$(R_L = 2.2\text{ k}\Omega, I_F = 1.6\text{ mA})$ $T_A = 25^\circ\text{C}$		HCPL-0700		1.5	15 10	
	$(R_L = 4.7\text{ k}\Omega, I_F = 0.5\text{ mA})$ $(R_L = 4.7\text{ k}\Omega, I_F = 0.5\text{ mA})\ T_A = 25^\circ\text{C}$		HCPL-0701		12	90 60	
	$(R_L = 270\ \Omega, I_F = 12\text{ mA})$ $T_A = 25^\circ\text{C}$		HCPL-0701		1.3	10 7	
	$(R_L = 2.2\text{ k}\Omega, I_F = 1.6\text{ mA})$ $T_A = 25^\circ\text{C}$		HCPL-0700		7	50 35	
Common mode transient immunity at logic high	$(I_F = 0\text{ mA}, V_{CM} = 10\text{ V}_{P-P})$ $T_A = 25^\circ\text{C}, (R_L = 2.2\text{ k}\Omega)$ (Note 3) (Fig. 14)	ICM_{HI}	HCPL-0700	1,000	10,000		$\text{V}/\mu\text{s}$
			HCPL-0701				
Common mode transient immunity at logic low	$(I_F = 1.6\text{ mA}, V_{CM} = 10\text{ V}_{P-P}, R_L = 2.2\text{ k}\Omega)$ $T_A = 25^\circ\text{C}$ (Note 3) (Fig. 14)	ICM_{LI}	HCPL-0700	1,000	10,000		$\text{V}/\mu\text{s}$
			HCPL-0701				

NOTES

1. Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.
2. Pin 7 open. Use of a resistor between pins 5 and 7 will decrease gain and delay time.
3. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0\text{ V}$). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8\text{ V}$).
4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
5. 2500 VAC RMS for 1 minute duration is equivalent to 3000 VAC RMS for 1 second duration.

** All typicals at $T_A = 25^\circ\text{C}$

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ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Current Limiting Resistor Calculations

$$R_1 \text{ (Non-Invert)} = \frac{V_{DD1} - V_{DF} - V_{OL1}}{I_F}$$

$$R_1 \text{ (Invert)} = \frac{V_{DD1} - V_{OH1} - V_{DF}}{I_F}$$

$$R_2 = \frac{V_{DD2} - V_{OLX} (@ I_L - I_2)}{I_L}$$

Where:

V_{DD1} - Input Supply Voltage

V_{DD2} - Output Supply Voltage

V_{DF} - Diode Forward Voltage

V_{OL1} - Logic "0" Voltage of Driver

V_{OH1} - Logic "1" Voltage of Driver

I_F - Diode Forward Current

V_{OLX} - Saturation Voltage of
Output Transistor

I_L - Load Current Through
Resistor R2

I_2 - Input Current of Output Gate

INPUT			OUTPUT						
			CMOS @ 5 V	CMOS @ 10 V	74XX	74LXX	74SXX	74LSXX	74HXX
		R1 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)	R2 (Ω)
CMOS @ 5 V	NON-INV.	2000	1000	2200	750	1000	1000	1000	560
	INV.	510							
CMOS @ 10 V	NON-INV.	5100							
	INV.	4700							
74XX	NON-INV.	2200							
	INV.	180							
74LXX	NON-INV.	1800							
	INV.	100							
74SXX	NON-INV.	2000							
	INV.	360							
74LSXX	NON-INV.	2000							
	INV.	180							
74HXX	NON-INV.	2000							
	INV.	180							

Fig. 1 Resistor Values for Logic Interface

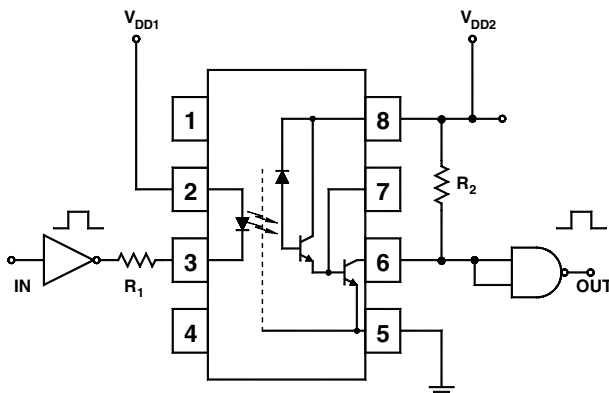


Fig. 2 Non-Inverting Logic Interface

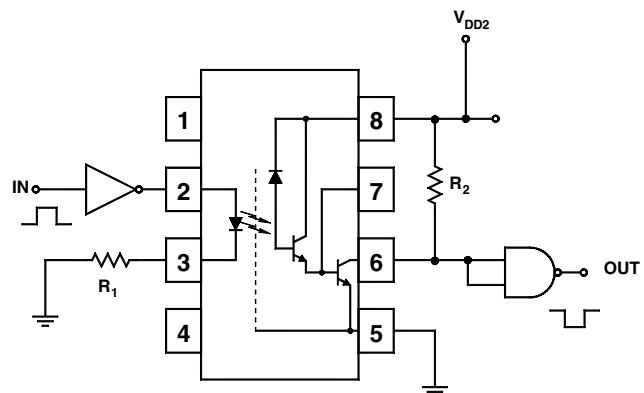


Fig. 3 Inverting Logic Interface

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Fig. 4 Propagation Delay vs. Temperature

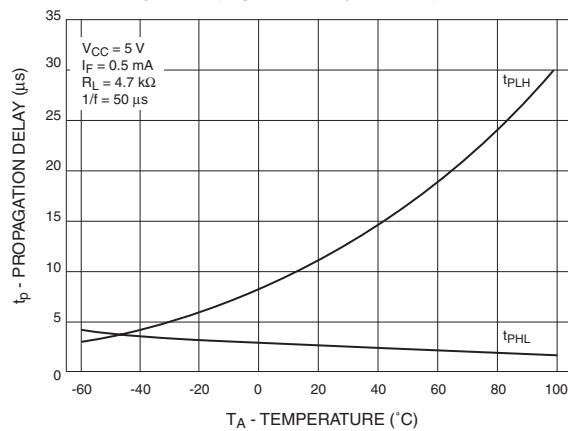


Fig. 5 Propagation Delay vs. Temperature

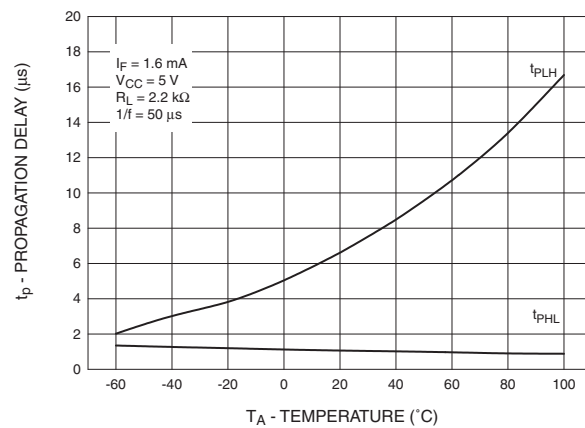


Fig. 6 Propagation Delay vs. Temperature

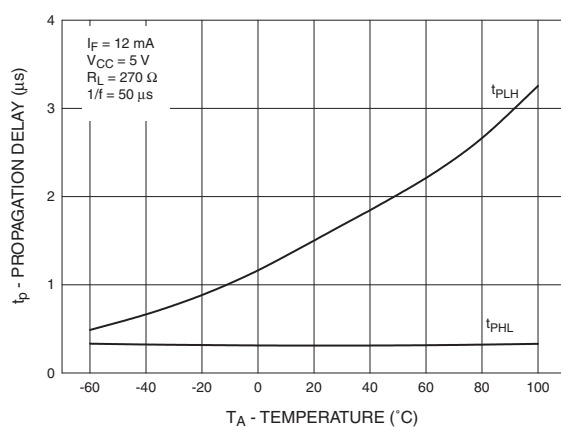
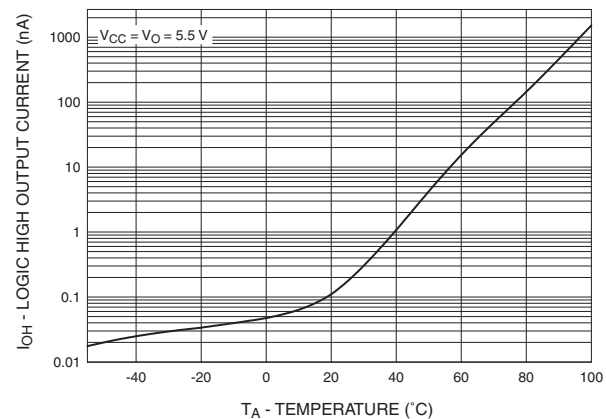


Fig. 7 Logic High Output Current vs. Temperature



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Fig. 8 Output Current vs. Input Forward Current

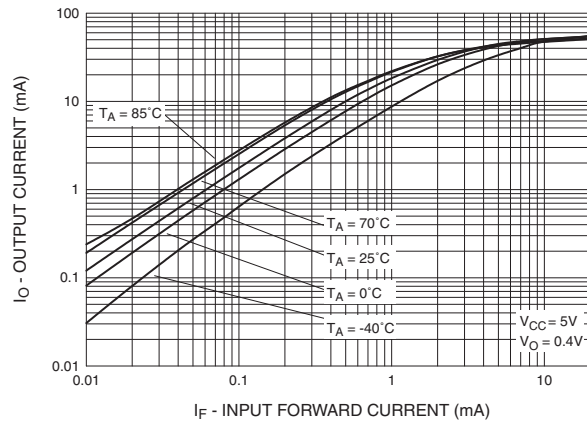


Fig. 9 Input Forward Current vs. Forward Voltage

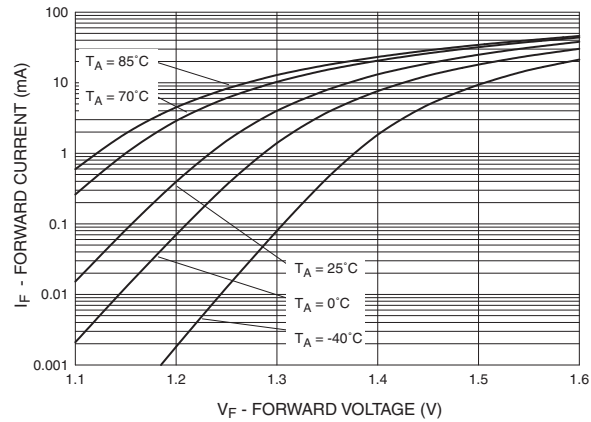


Fig. 10 Logic Low Supply Current vs. Input Forward Current

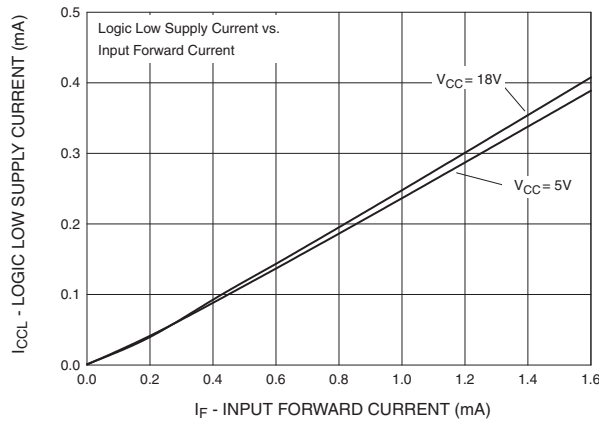


Fig. 11 DC Transfer Characteristics

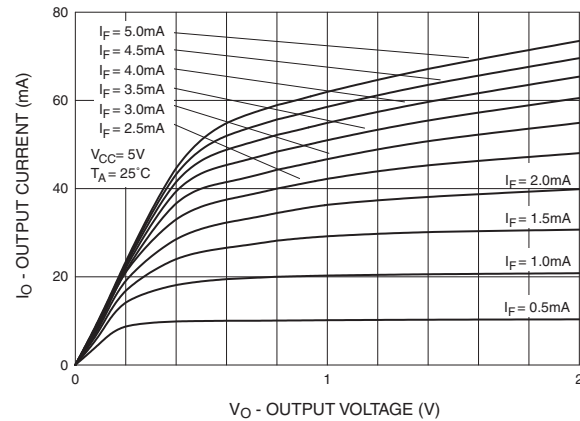
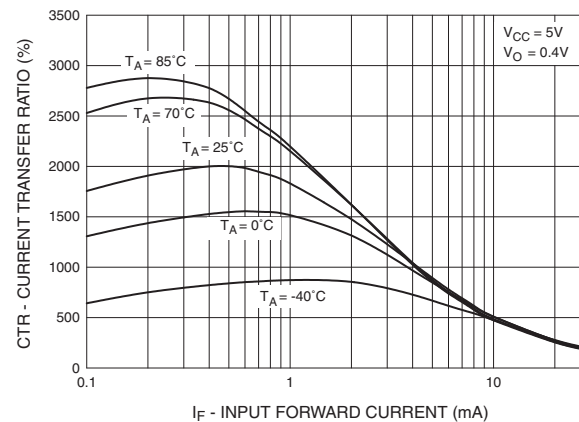
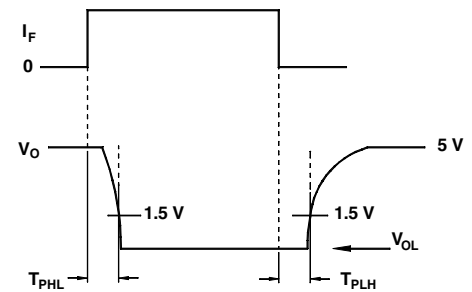
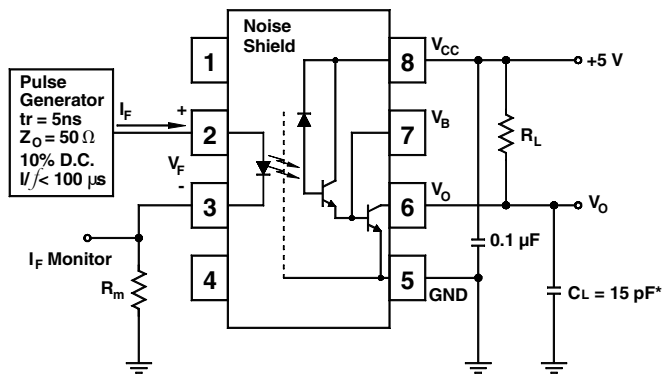


Fig. 12 Current Transfer Ratio vs. Input Forward Current



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* Includes probe and fixture capacitance

Fig. 13 Switching Time Test Circuit

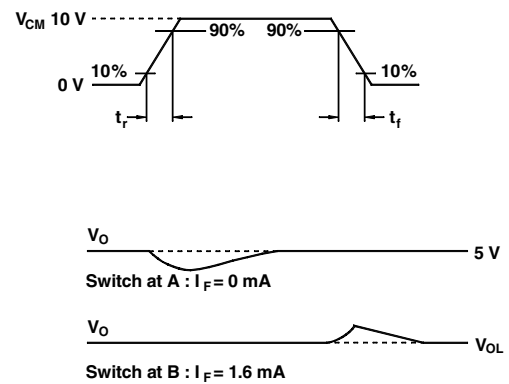
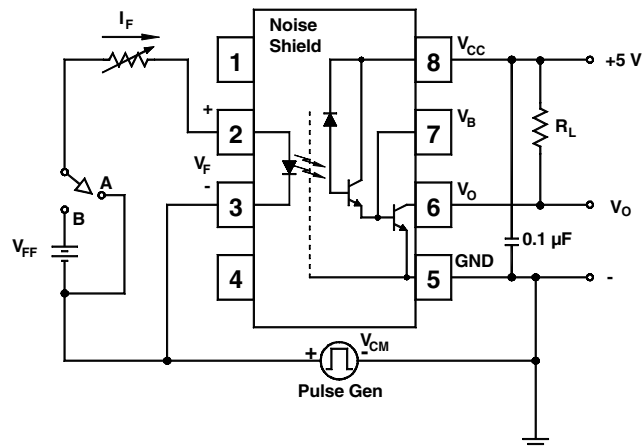


Fig. 14 Common Mode Immunity Test Circuit

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ORDERING INFORMATION

Option	Order Entry Identifier	Description
R1	.R1	Tape and Reel (500 per reel)
R2	.R2	Tape and Reel (2500 per reel)

QT Carrier Tape Specifications

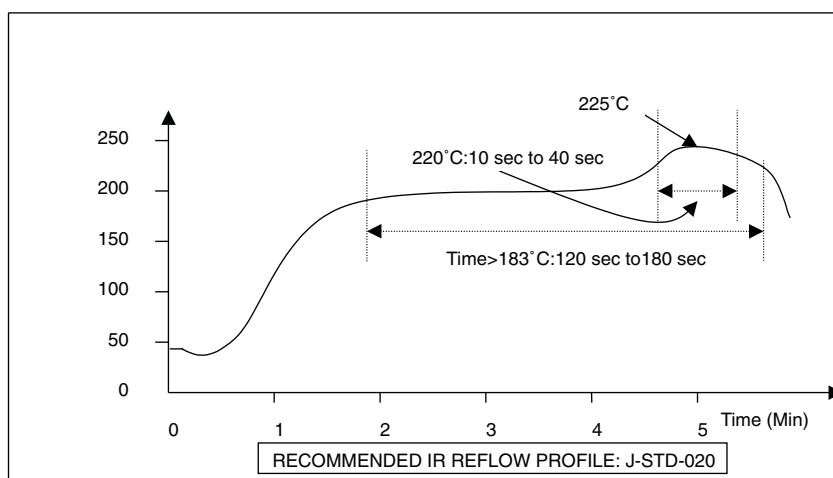
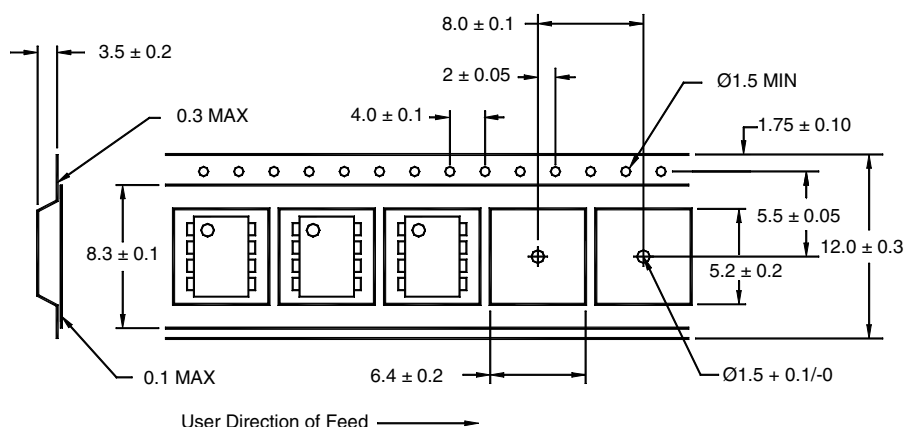


Fig. 15 JEDEC Reflow Profile

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