

HAT2068R

Silicon N Channel Power MOS FET
Power Switching

HITACHI

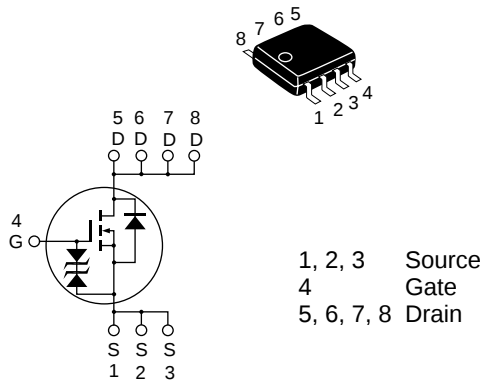
ADE-208-1225B (Z)
3rd. Edition
Jan. 2001

Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 7 \text{ m}\Omega$ typ (at $V_{GS} = 10\text{V}$)

Outline

SOP-8



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	30	V
Gate to source voltage	V _{GSS}	± 20	V
Drain current	I _D	14	A
Drain peak current	I _{D(pulse)} ^{Note1}	112	A
Body-drain diode reverse drain current	I _{DR}	14	A
Channel dissipation	Pch ^{Note2}	2.5	W
Channel to Ambient Thermal Impedance	θch-a ^{Note2}	50	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	– 55 to + 150	°C

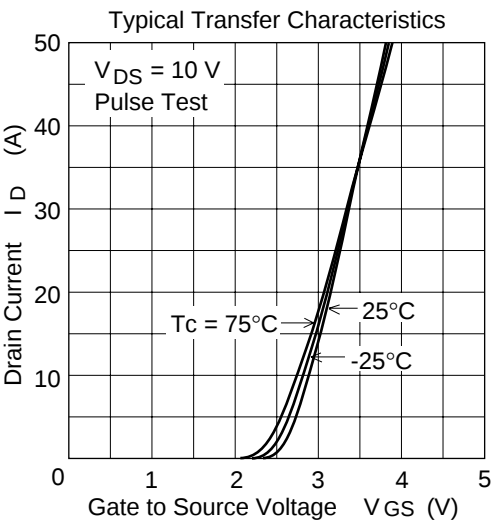
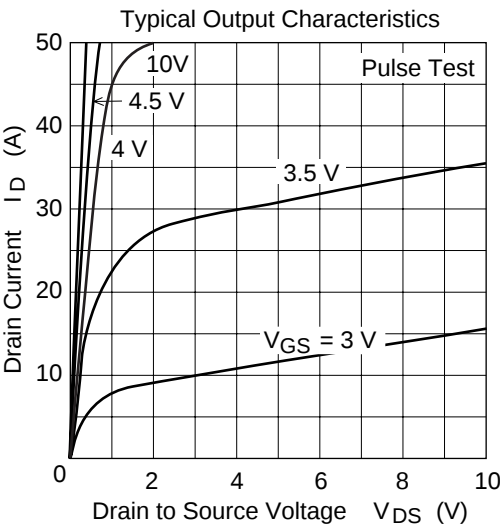
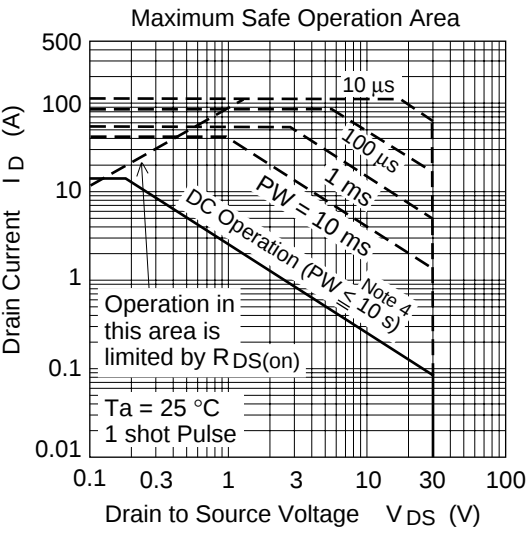
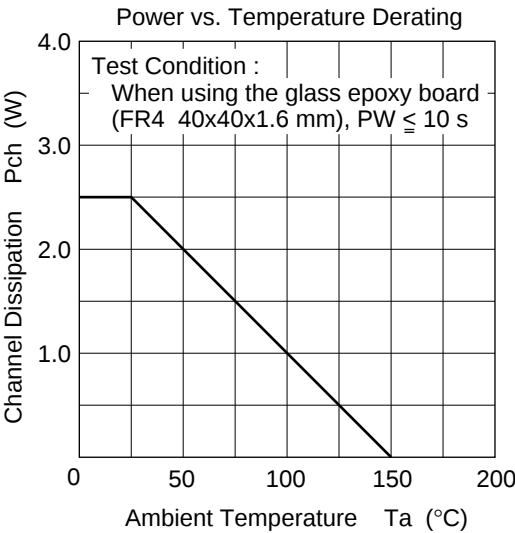
Note: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

Electrical Characteristics (Ta = 25°C)

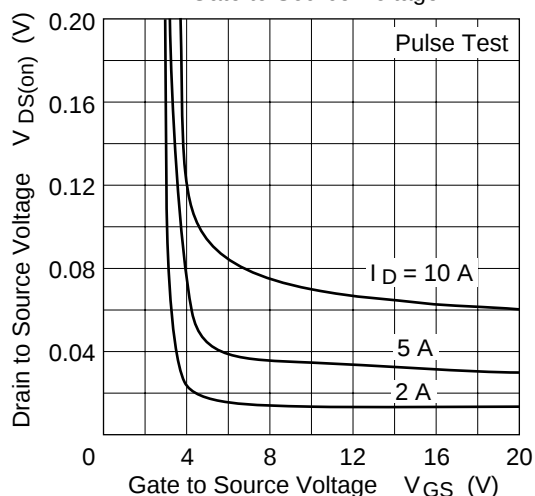
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	7	9	$\text{m}\Omega$	$I_D = 7 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	11	16	$\text{m}\Omega$	$I_D = 7 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	16	28	—	S	$I_D = 7 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	1650	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	400	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	220	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	26	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	5	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	5	—	nc	$I_D = 14 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	15	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 7 \text{ A}$
Rise time	t_r	—	30	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	50	—	ns	$R_L = 1.43 \text{ }\Omega$
Fall time	t_f	—	10	—	ns	$R_g = 4.7 \text{ }\Omega$
Body-drain diode forward voltage	V_{DF}	—	0.80	1.10	V	$I_F = 14 \text{ A}$, $V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 14 \text{ A}$, $V_{GS} = 0$ $diF/dt = 50 \text{ A}/\mu\text{s}$

Note: 3. Pulse test

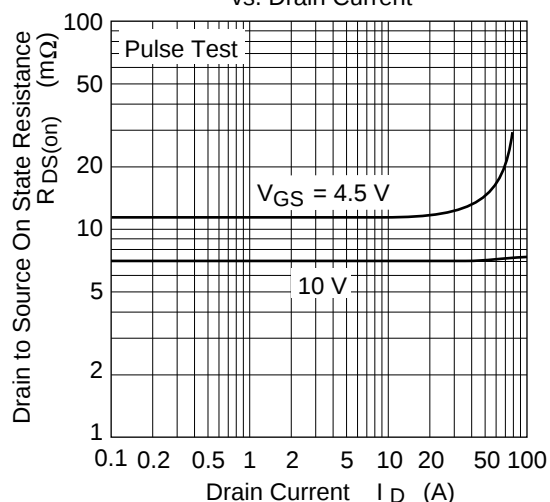
Main Characteristics



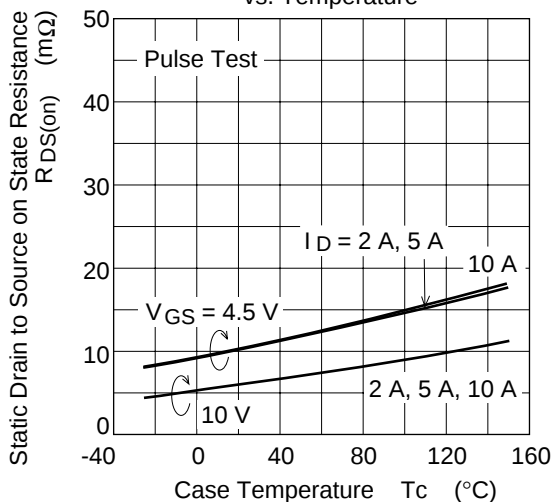
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



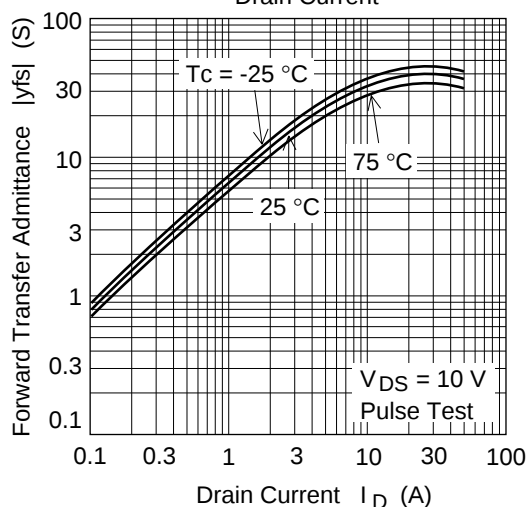
Static Drain to Source on State Resistance
vs. Drain Current

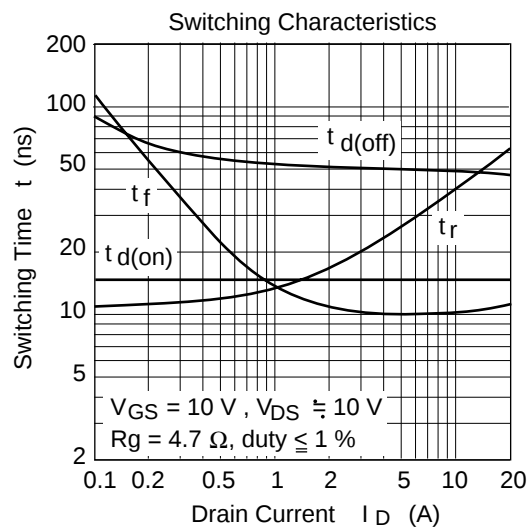
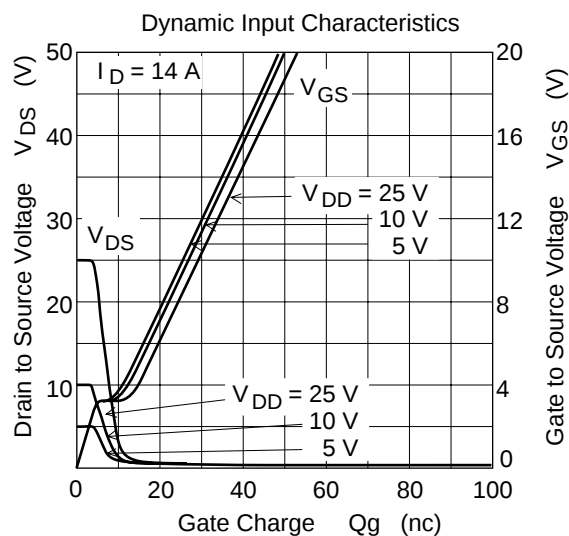
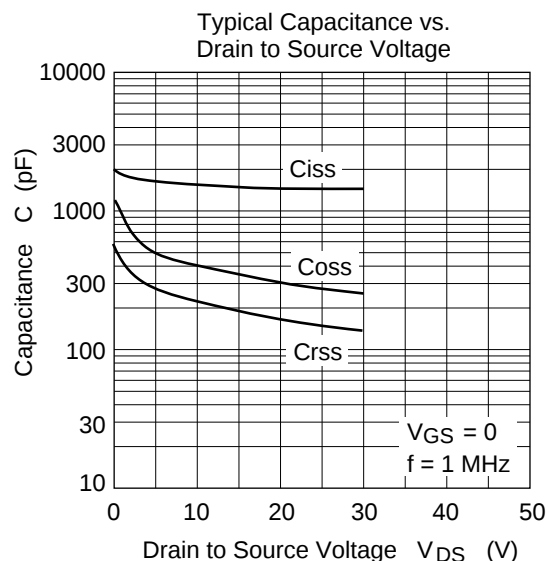
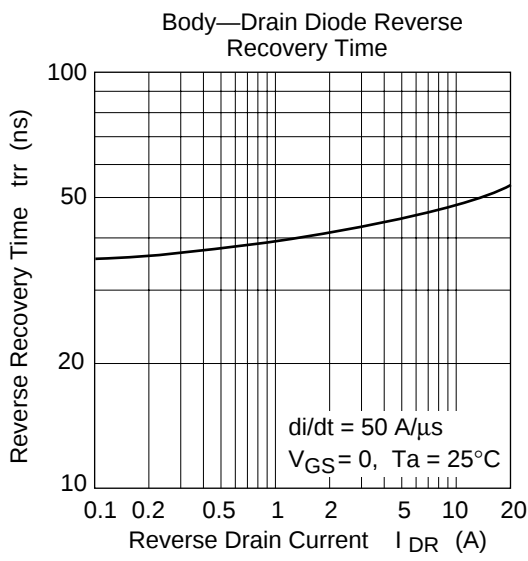


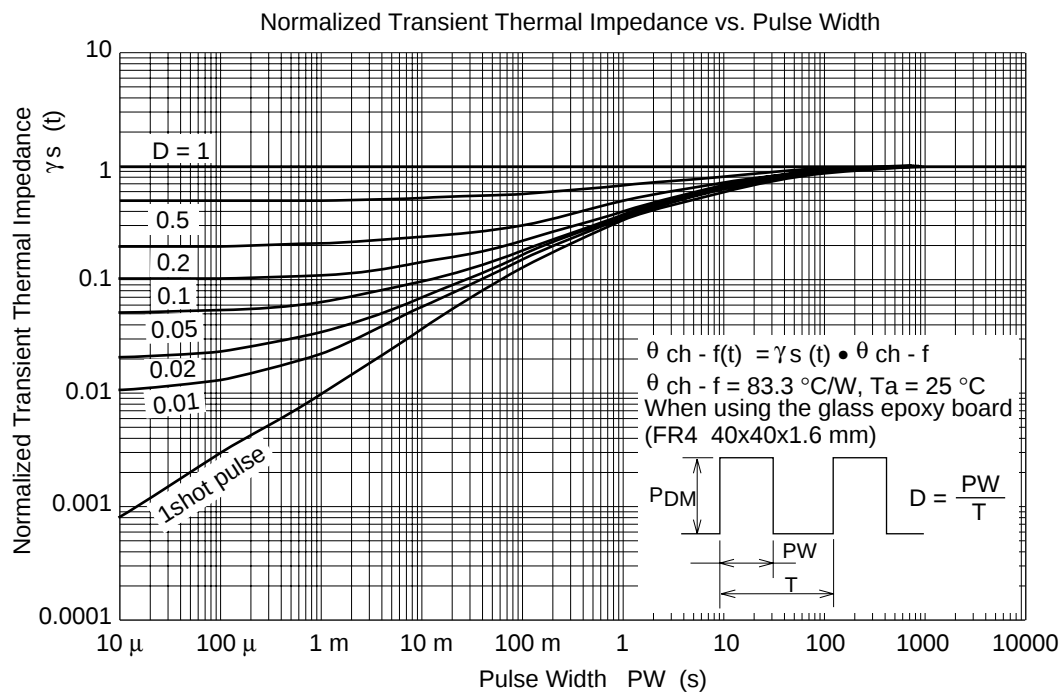
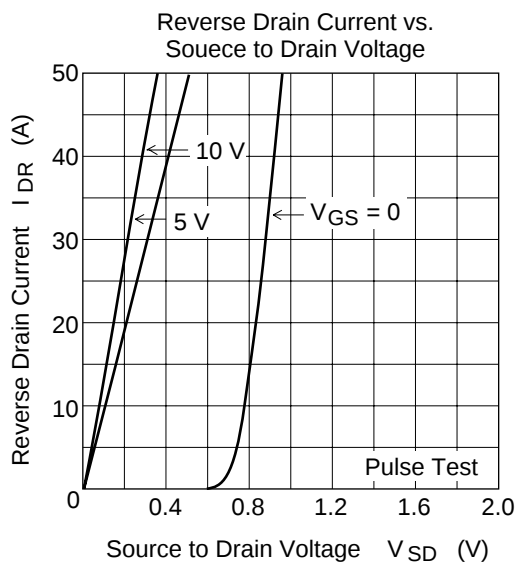
Static Drain to Source on State Resistance
vs. Temperature



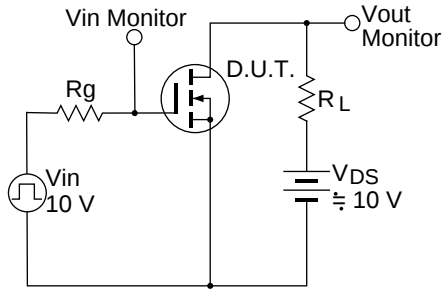
Forward Transfer Admittance vs.
Drain Current



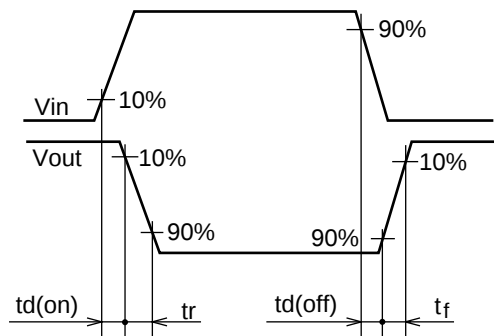




Switching Time Test Circuit

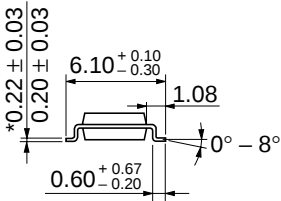
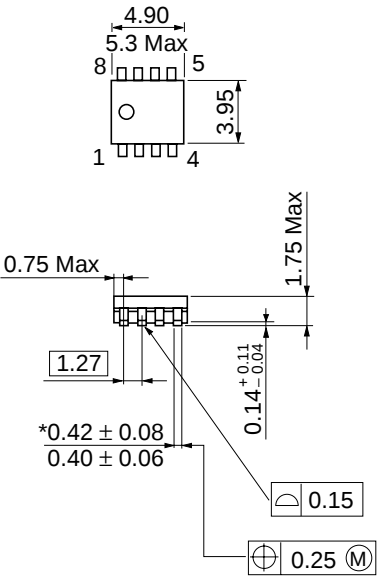


Switching Time Waveform



Package Dimensions

As of January, 2001
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

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