

H5N2004DL, H5N2004DS

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

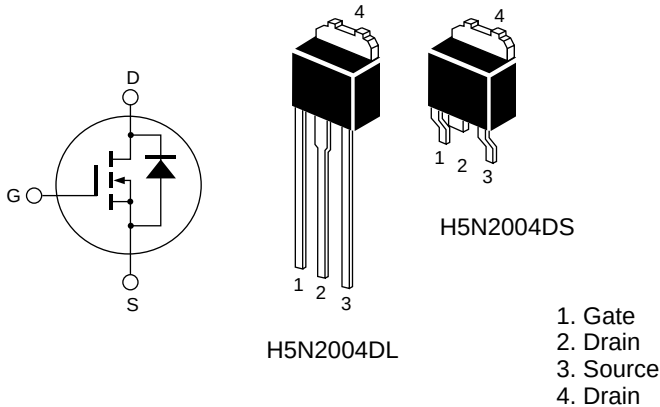
ADE-208-1372 (Z)
1st. Edition
Mar. 2001

Features

- Low on-resistance: $R_{DS(on)} = 0.38 \text{ typ.}$
- Low leakage current: $IDSS = 1 \text{ }\mu\text{A max (at } V_{DS} = 200 \text{ V)}$
- High speed switching: $t_f = 10 \text{ ns typ (at } V_{GS} = 10 \text{ V, } V_{DD} = 100 \text{ V, } I_D = 4 \text{ A)}$
- Low gate charge: $Q_g = 14 \text{ nC typ (at } V_{DD} = 160 \text{ V, } V_{GS} = 10 \text{ V, } I_D = 8 \text{ A)}$
- Avalanche ratings

Outline

DPAK-2



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	200	V
Gate to source voltage	V_{GSS}	±30	V
Drain current	I_D	8	A
Drain peak current	$I_{D (pulse)}$ ^{Note 1}	32	A
Body-drain diode reverse drain current	I_{DR}	8	A
Body-drain diode reverse drain peak current	$I_{DR (pulse)}$ ^{Note 1}	32	A
Avalanche current	I_{AP} ^{Note 3}	7	A
Channel dissipation	P_{ch} ^{Note 2}	30	W
Channel to case thermal Impedance	θ_{ch-c}	4.17	°C/W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	–55 to +150	°C

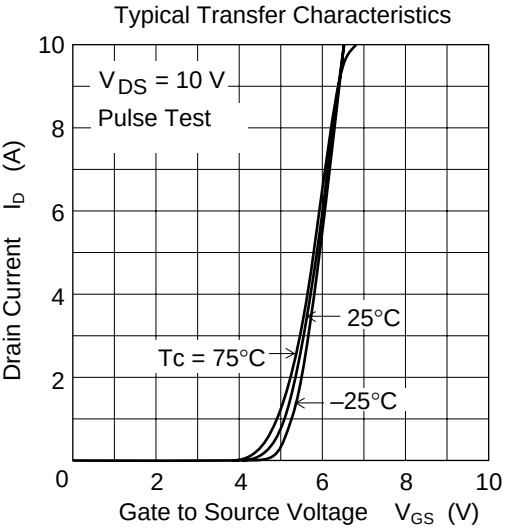
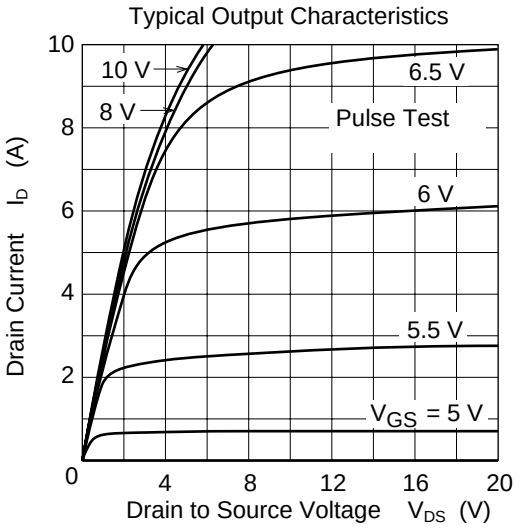
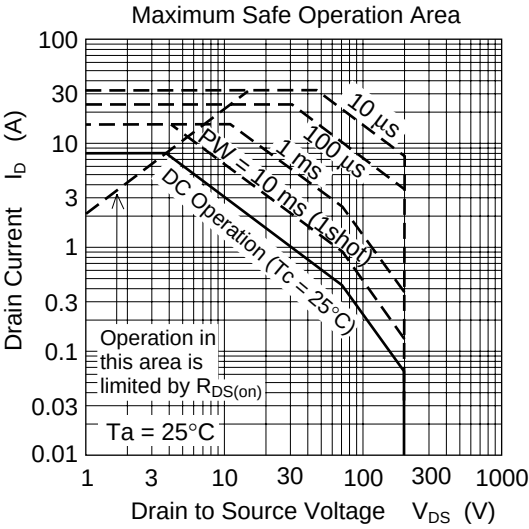
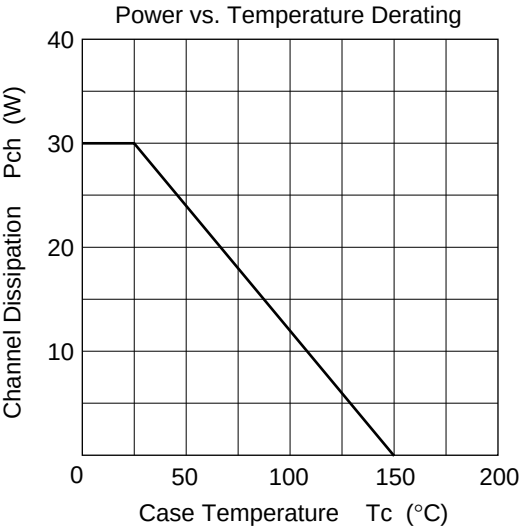
Notes: 1. $PW = 10 \mu s$, duty cycle 1%
2. Value at $T_c = 25^\circ C$
3. $T_{ch} = 150^\circ C$

Electrical Characteristics (Ta = 25°C)

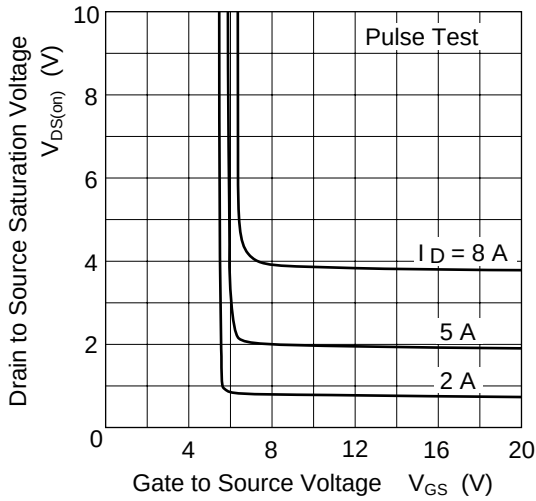
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	200	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 200 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.38	0.48		$I_D = 4 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	3.3	5.5	—	S	$I_D = 4 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	450	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	65	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	13	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_d(on)$	—	19	—	ns	$I_D = 4 \text{ A}$
Rise time	t_r	—	32	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_d(off)$	—	47	—	ns	$R_L = 25$
Fall time	t_f	—	10	—	ns	$R_g = 10$
Total gate charge	Q_g	—	14	—	nC	$V_{DD} = 160 \text{ V}$
Gate to source charge	Q_{gs}	—	2.5	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	7.5	—	nC	$I_D = 4 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.9	1.4	V	$I_F = 8 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	100	—	ns	$I_F = 8 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery charge	Q_{rr}	—	0.4	—	μC	$diF/dt = 50 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

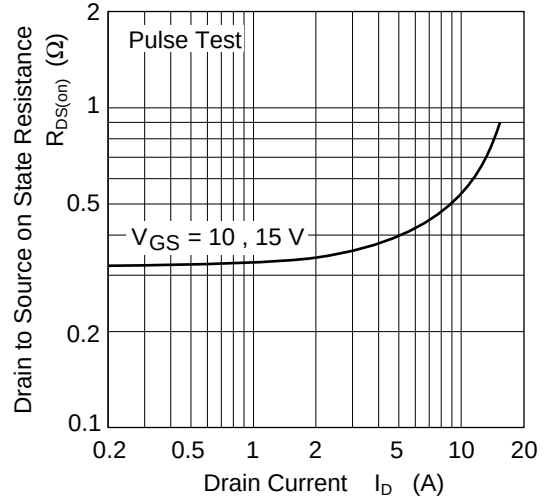
Main Characteristics



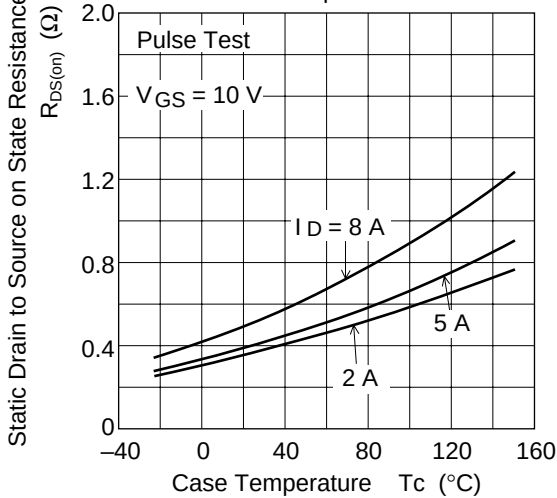
Drain to Source Saturation Voltage vs. Gate to Source Voltage



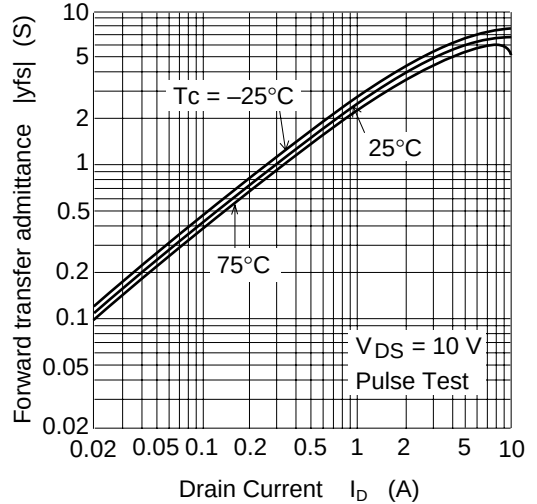
Static Drain to Source on State Resistance vs. Drain Current

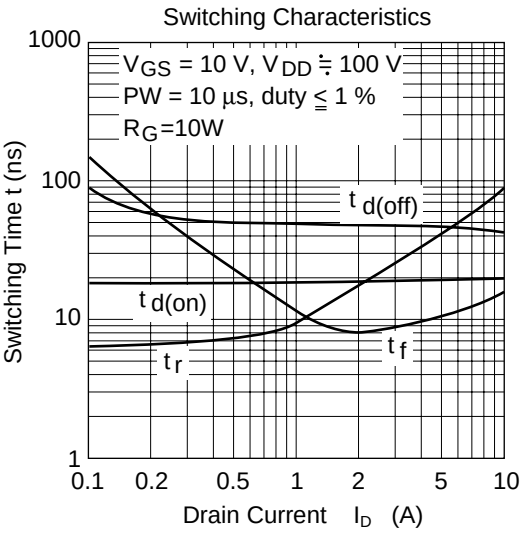
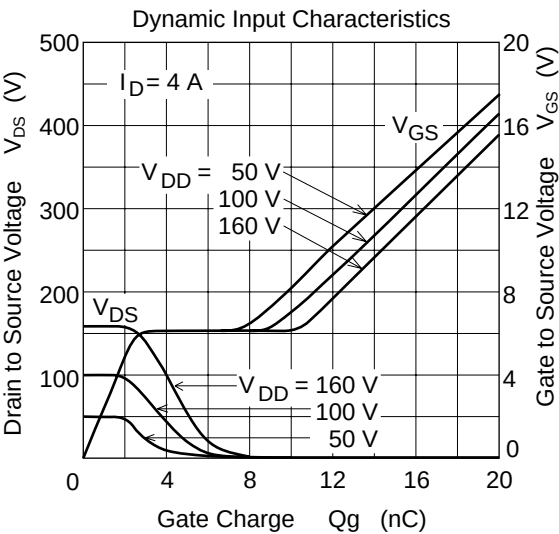
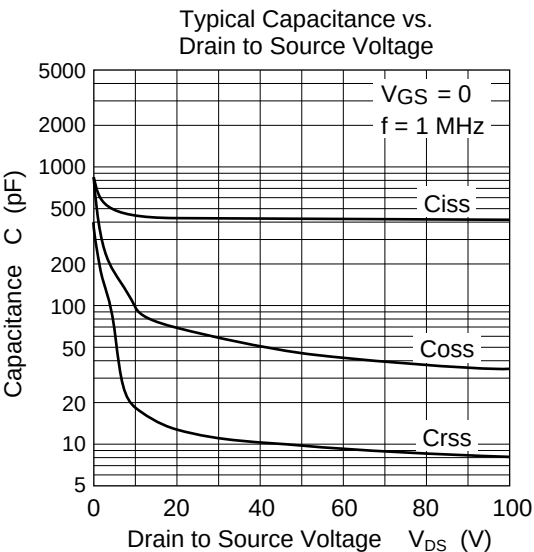
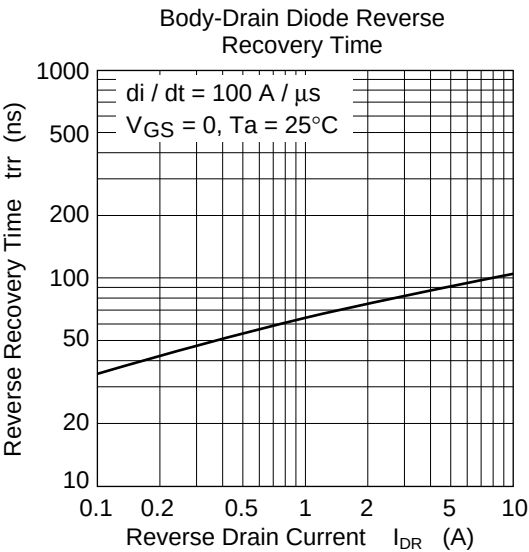


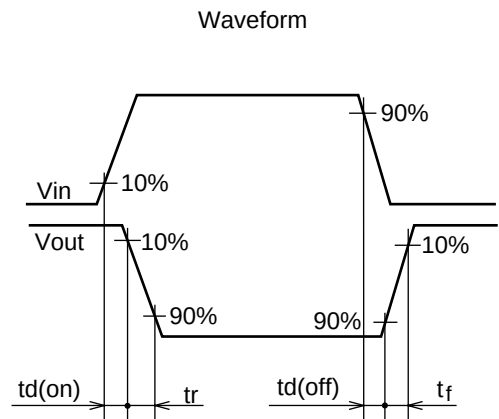
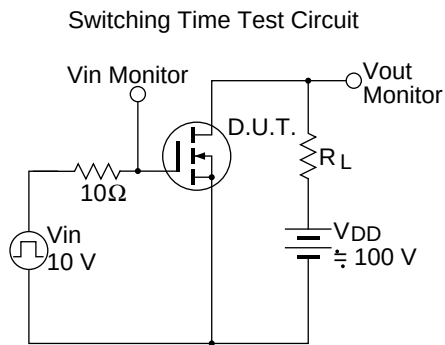
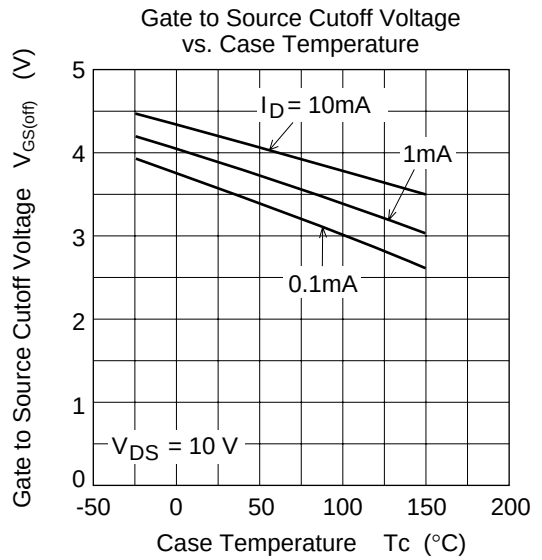
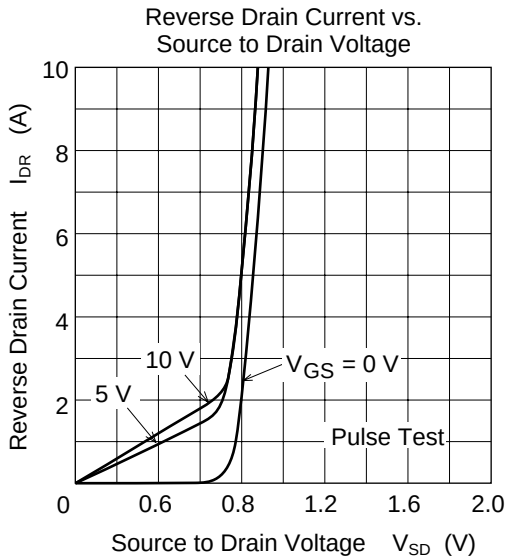
Static Drain to Source on State Resistance vs. Temperature

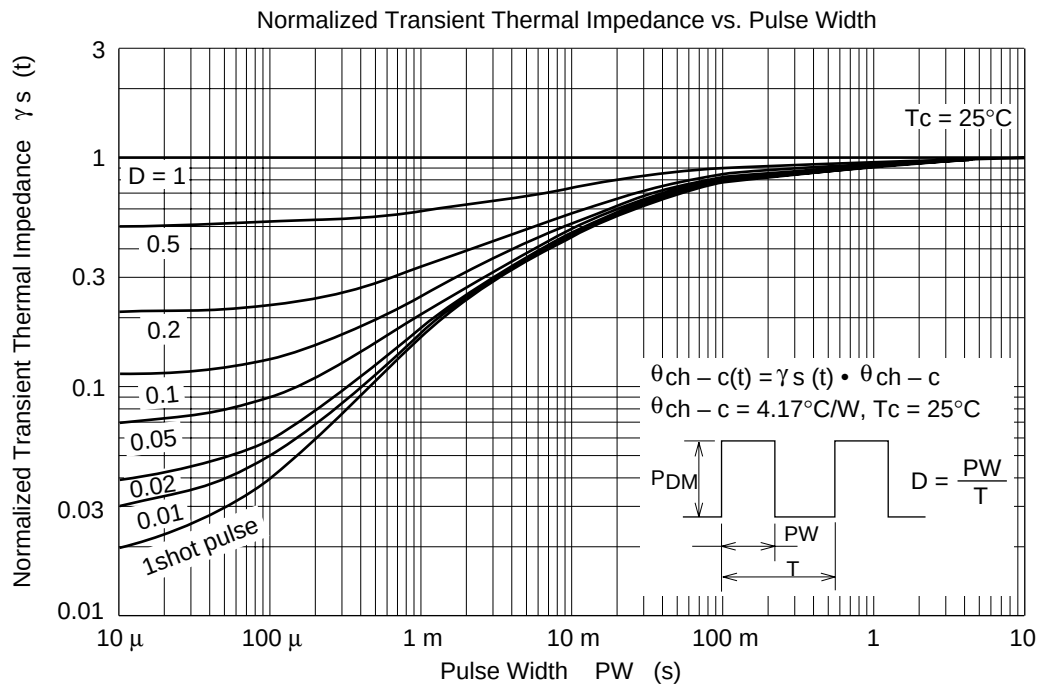


Forward Transfer Admittance vs. Drain Current





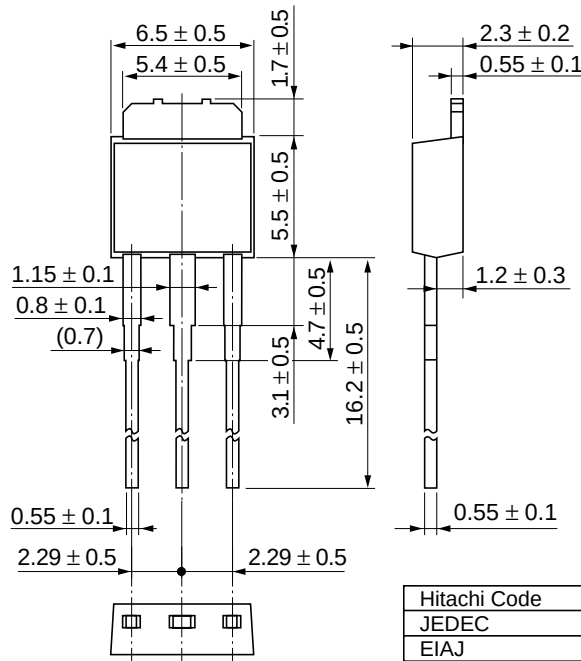




Package Dimensions

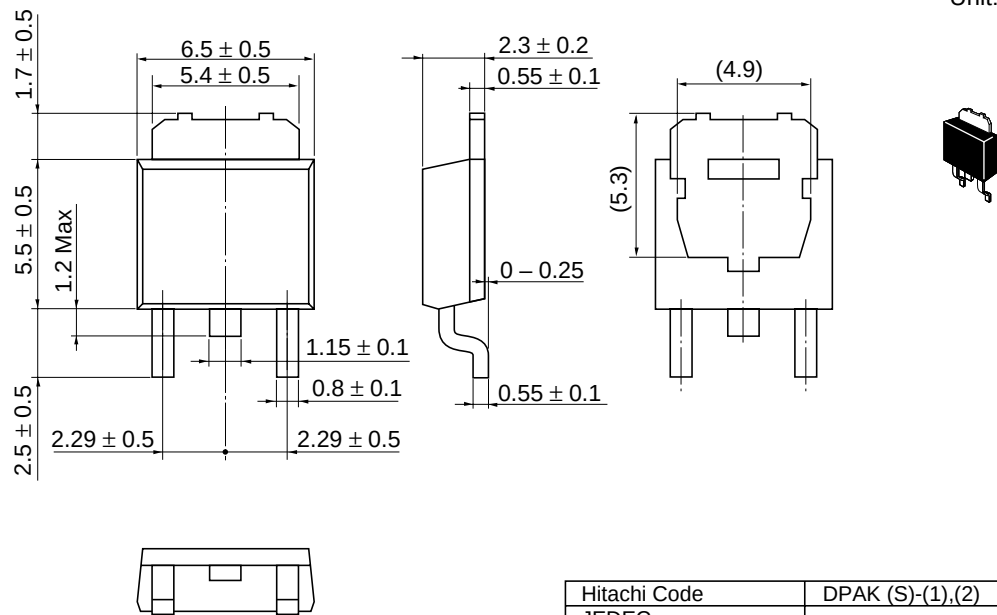
As of January, 2001

Unit: mm



Hitachi Code	DPAK (L)-(2)
JEDEC	—
EIAJ	—
Mass (reference value)	0.42 g

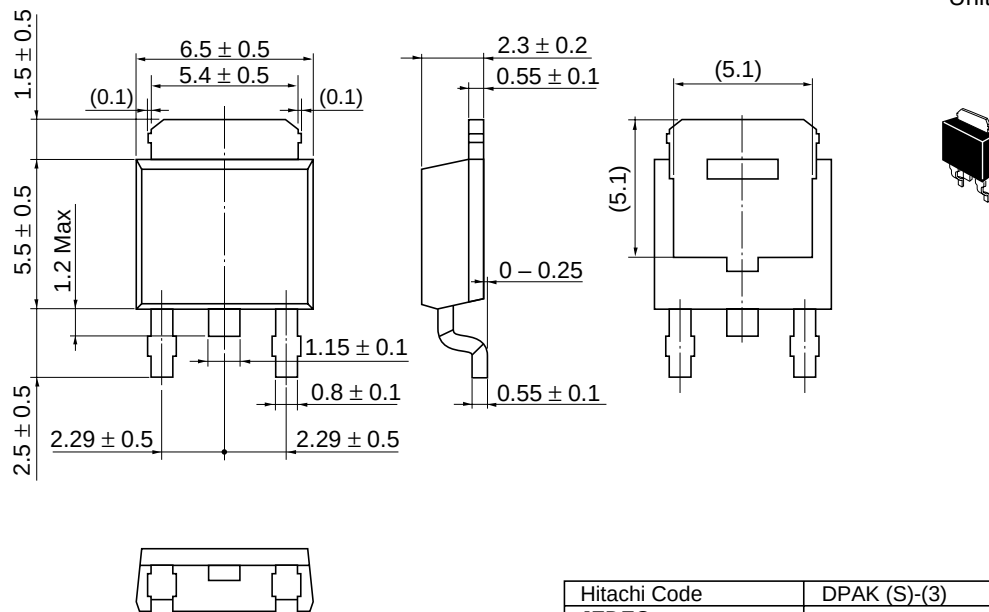
As of January, 2001
Unit: mm



Hitachi Code	DPAK (S)-(1),(2)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

As of January, 2001

Unit: mm



Hitachi Code	DPAK (S)-(3)
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.28 g

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