

HAT2049T

Silicon N Channel Power MOS FET
High Speed Power Switching

HITACHI

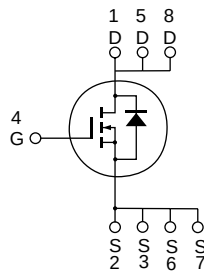
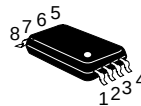
ADE-208-723A (Z)
2nd. Edition
Mar. 2001

Features

- Low on-resistance
- Capable of 2.5 V gate drive
- Low drive current
- High density mounting

Outline

TSSOP-8



1, 5, 8 Drain
2, 3, 6, 7 Source
4 Gate

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	30	V
Gate to source voltage	V _{GSS}	± 12	V
Drain current	I _D	8	A
Drain peak current	I _{D(pulse)} ^{Note1}	64	A
Body-drain diode reverse drain current	I _{DR}	8	A
Channel dissipation	Pch ^{Note2}	1.3	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	– 55 to + 150	°C

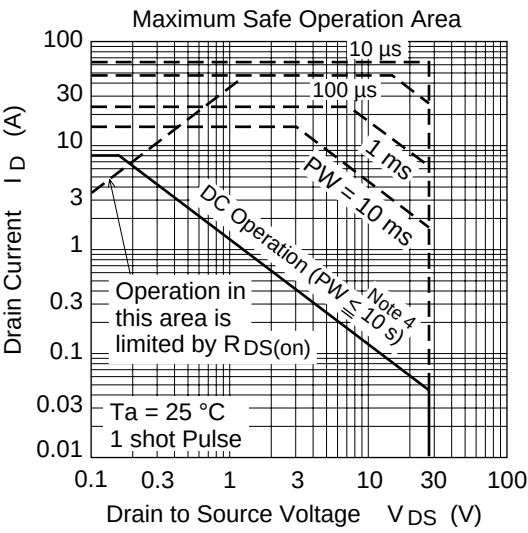
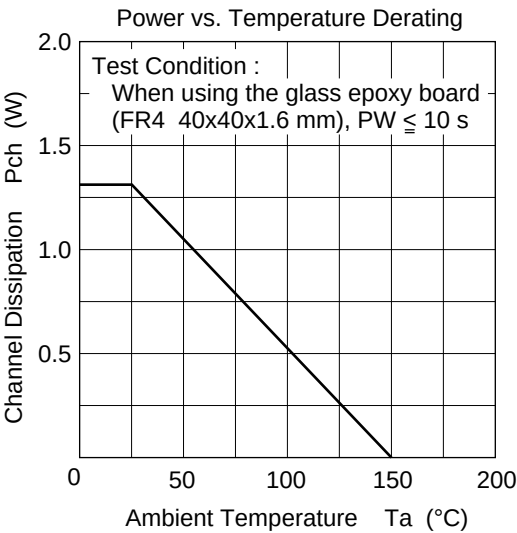
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
2. When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

Electrical Characteristics (Ta = 25°C)

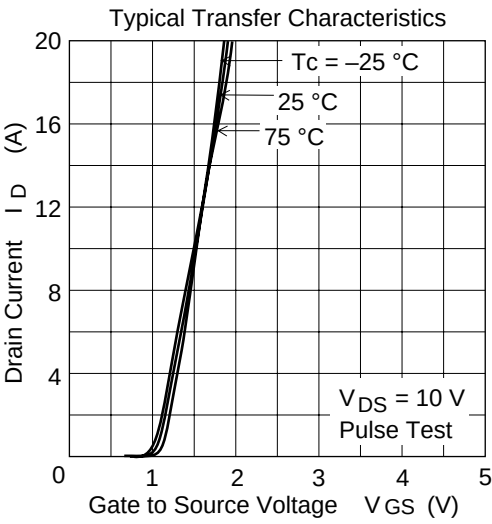
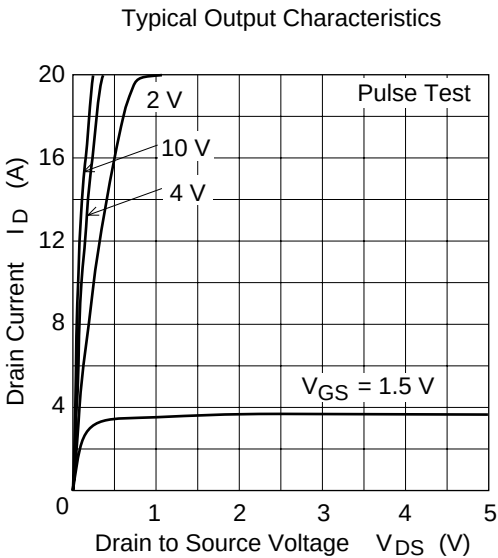
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 12 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.4	—	1.4	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.013	0.017	Ω	$I_D = 4 \text{ A}$, $V_{GS} = 4 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	0.017	0.025	Ω	$I_D = 4 \text{ A}$, $V_{GS} = 2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	13	20	—	S	$I_D = 4 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	1430	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	410	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	265	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	23	—	ns	$V_{GS} = 4 \text{ V}$, $I_D = 4 \text{ A}$
Rise time	t_r	—	165	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	215	—	ns	
Fall time	t_f	—	185	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.83	1.08	V	$I_F = 8 \text{ A}$, $V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	30	—	ns	$I_F = 8 \text{ A}$, $V_{GS} = 0$ $diF/dt = 20 \text{ A}/\mu\text{s}$

Note: 3. Pulse test

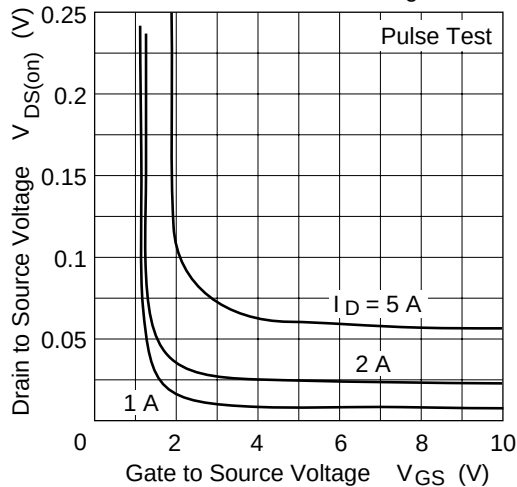
Main Characteristics



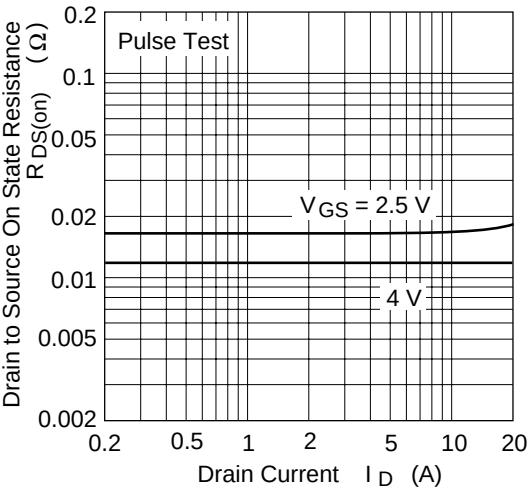
Note 4 :
When using the glass epoxy board
(FR4 40x40x1.6 mm)



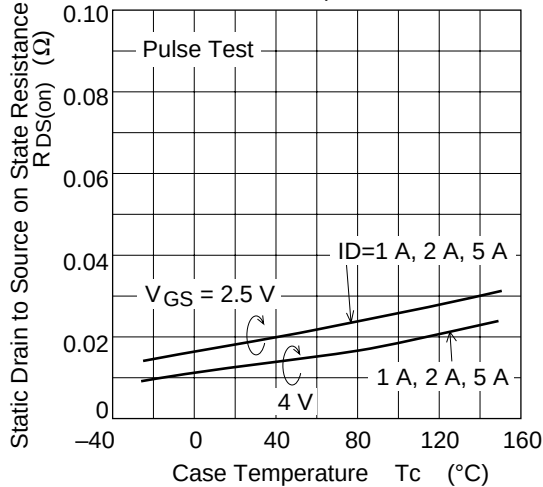
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



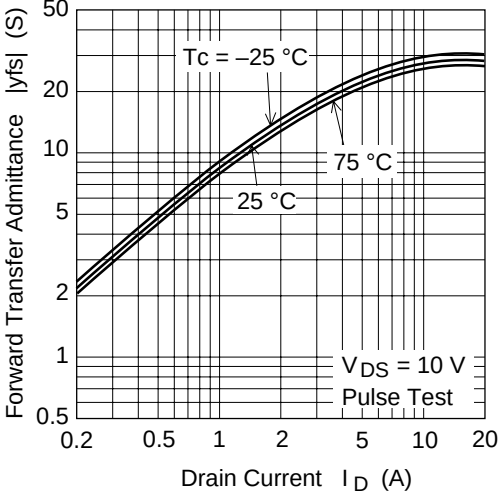
Static Drain to Source on State Resistance
vs. Drain Current



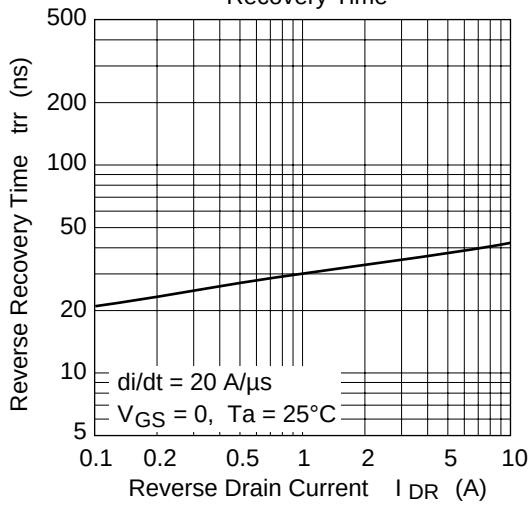
Static Drain to Source on State Resistance
vs. Temperature



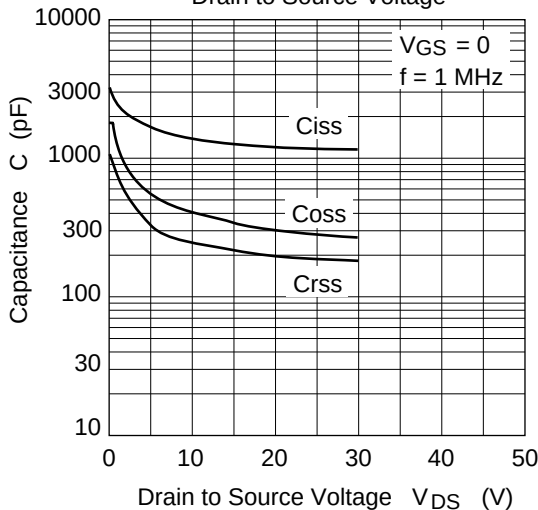
Forward Transfer Admittance vs.
Drain Current



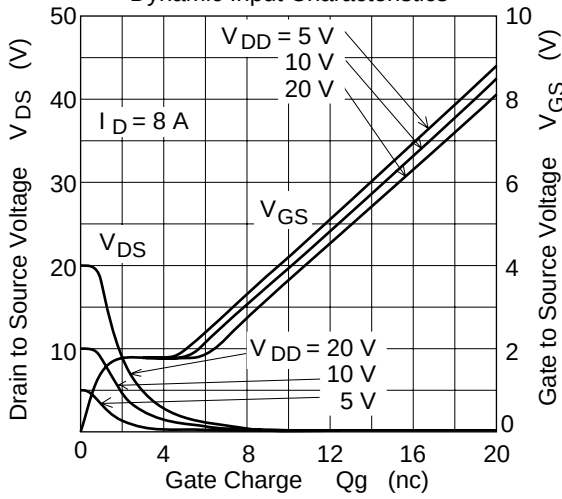
Body-Drain Diode Reverse Recovery Time



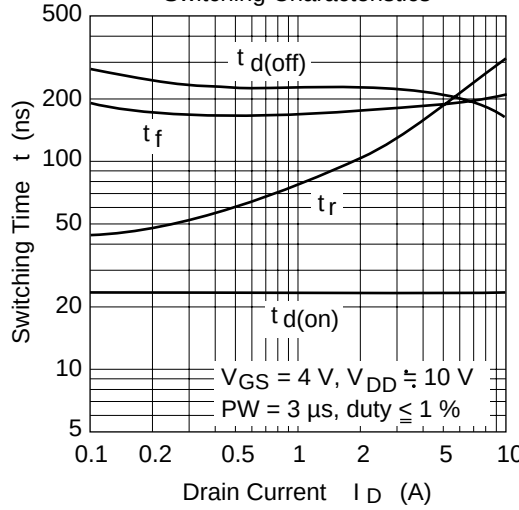
Typical Capacitance vs. Drain to Source Voltage

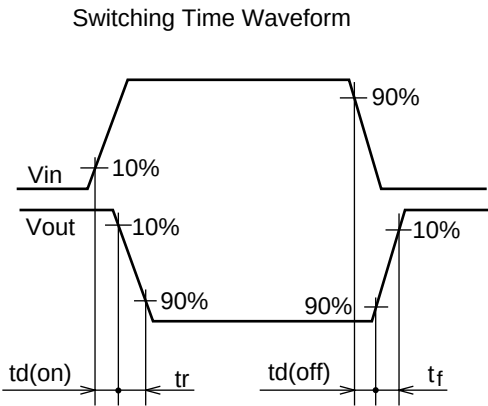
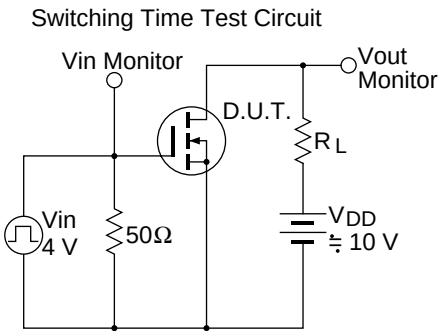
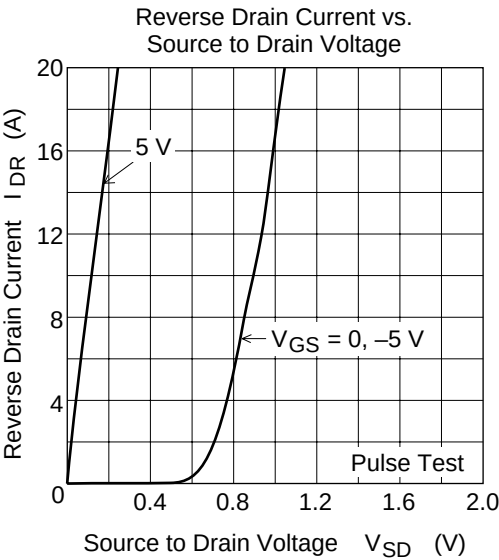


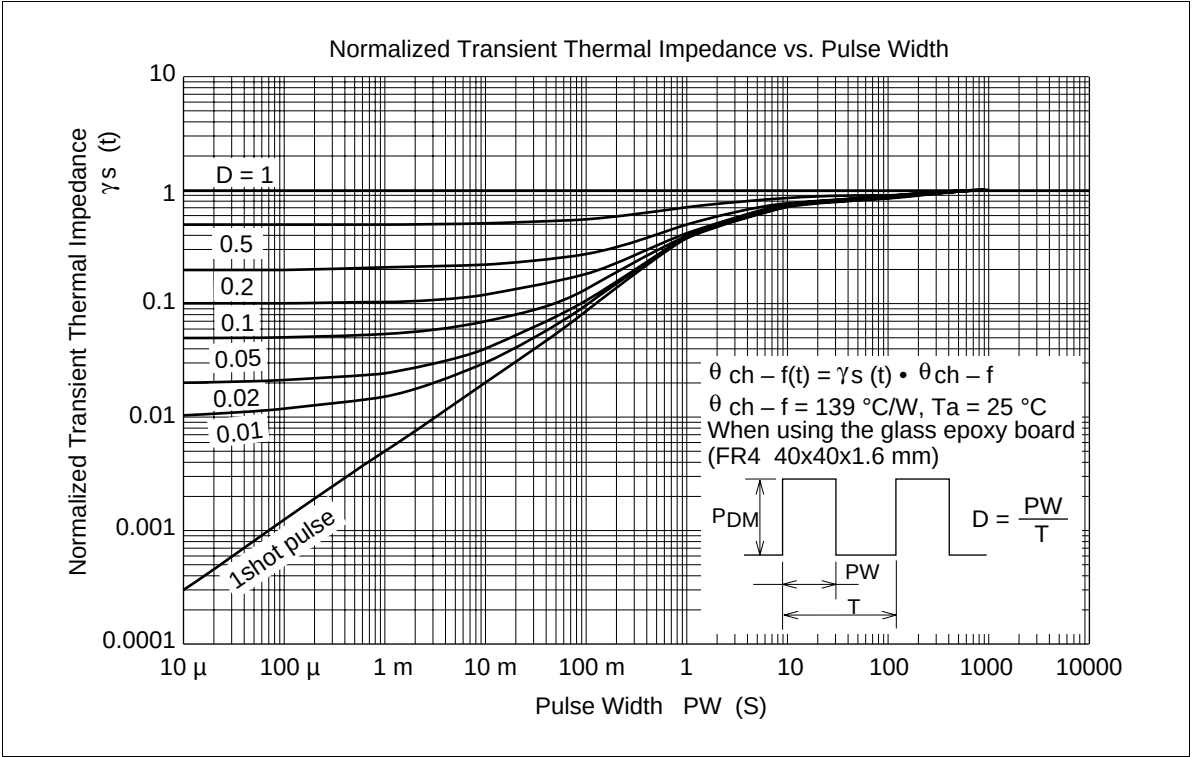
Dynamic Input Characteristics



Switching Characteristics

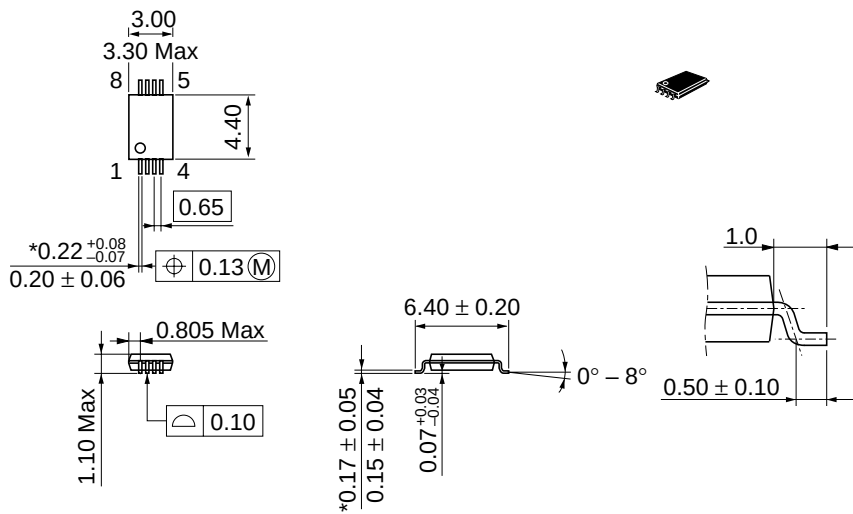






Package Dimensions

As of January, 2001
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-8D
JEDEC	—
EIAJ	—
Mass (reference value)	—

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