

HAT2059R/HAT2059RJ

Silicon N Channel Power MOS FET
High Speed Power Switching

HITACHI

ADE-208-935 (E)

1st. Edition

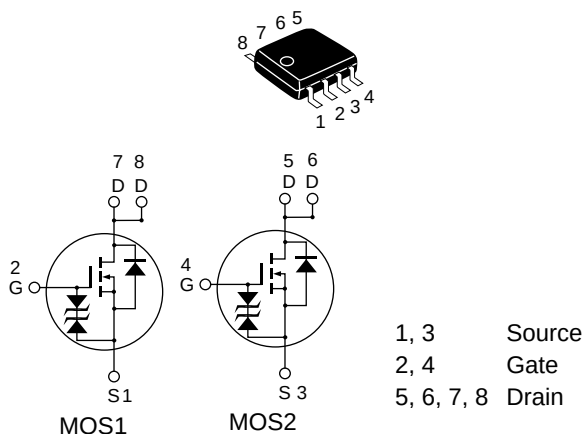
Mar. 2001

Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting
- "J" Is for automotive application
High temperature D-S leakage guarantee
Avalanche rating

Outline

SOP-8



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings		Unit
		HAT2059R	HAT2059RJ	
Drain to source voltage	V _{DSS}	150	150	V
Gate to source voltage	V _{GSS}	±20	±20	V
Drain current	I _D	2.5	2.5	A
Drain peak current	I _D (pulse) ^{Note1}	20	20	A
Body-drain diode reverse drain current	I _{DR}	2.5	2.5	A
Avalanche current	I _{AP} ^{Note4}	—	2.5	A
Avalanche energy	E _{AR} ^{Note4}	—	0.469	mJ
Channel dissipation	Pch ^{Note2}	2	2	W
	Pch ^{Note3}	3	3	W
Channel temperature	Tch	150	150	°C
Storage temperature	Tstg	−55 to +150	−55 to +150	°C

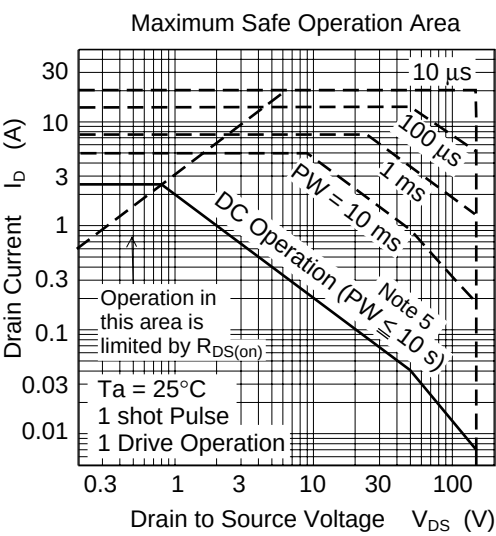
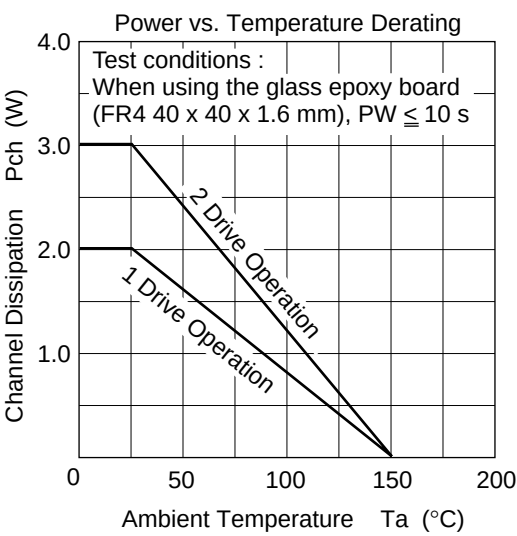
- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s
3. 2 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10 s
4. Value at Tch = 25°C, Rg ≥ 50 Ω

Electrical Characteristics (Ta = 25°C)

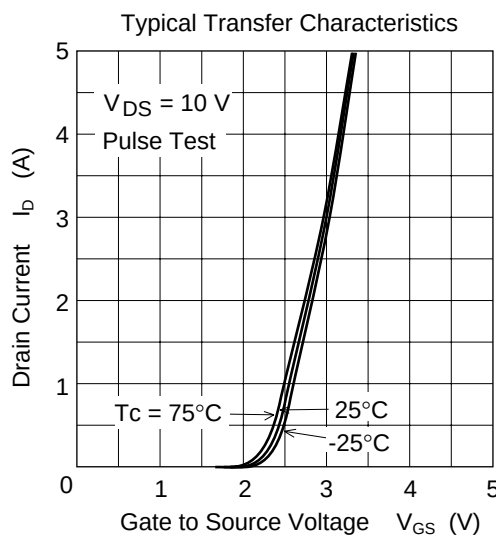
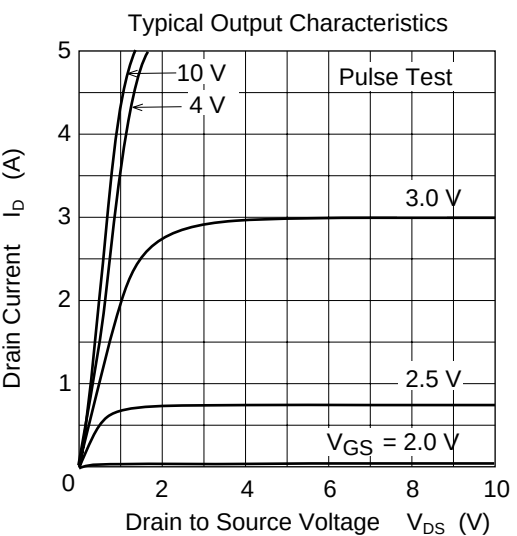
Item		Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage		$V_{(BR)DSS}$	150	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage		$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage	HAT2059R	I_{DSS}	—	—	1	μA	$V_{DS} = 150 \text{ V}$, $V_{GS} = 0$
drain current	HAT2059RJ	I_{DSS}	—	—	0.1	μA	
Zero gate voltage	HAT2059R	I_{DSS}	—	—	—	μA	$V_{DS} = 120 \text{ V}$, $V_{GS} = 0$
drain current	HAT2059RJ	I_{DSS}	—	—	10	μA	Ta = 125°C
Gate to source leak current		I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage		$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Forward transfer admittance		$ y_{fs} $	2.0	3	—	S	$I_D = 1 \text{ A}$ ^{Note1} , $V_{DS} = 10 \text{ V}$
Static drain to source on state resistance		$R_{DS(on)}$	—	260	320	m Ω	$I_D = 1 \text{ A}$ ^{Note1} , $V_{GS} = 10 \text{ V}$
		$R_{DS(on)}$	—	290	380	m Ω	$I_D = 1 \text{ A}$ ^{Note1} , $V_{GS} = 4 \text{ V}$
Input capacitance		C_{iss}	—	410	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$
Output capacitance		C_{oss}	—	145	—	pF	f = 1 MHz
Reverse transfer capacitance		C_{rss}	—	85	—	pF	
Turn-on delay time		td(on)	—	10	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 1 \text{ A}$ $V_{DD} \cong 30 \text{ V}$
Rise time		tr	—	17	—	ns	
Turn-off delay time		td(off)	—	110	—	ns	
Fall time		tf	—	50	—	ns	
Body-drain diode forward voltage		V_{DF}	—	0.85	1.1	V	$I_F = 2.5 \text{ A}$, $V_{GS} = 0^{*1}$
Body-drain reverse recovery time		trr	—	85	—	ns	$I_F = 2.5 \text{ A}$, $V_{GS} = 0$ diF/dt = 50 A/ μs

Note: 5. Pulse test

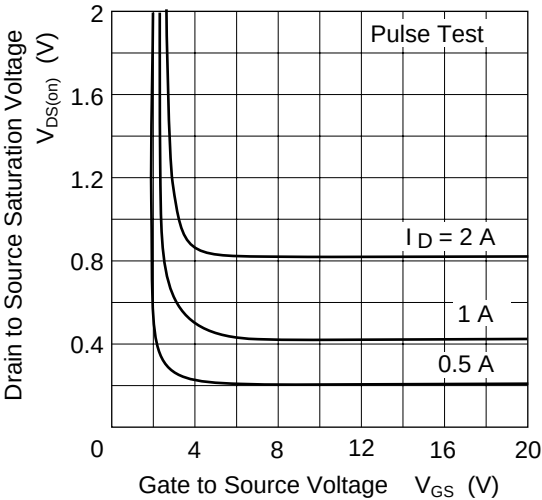
Main Characteristics



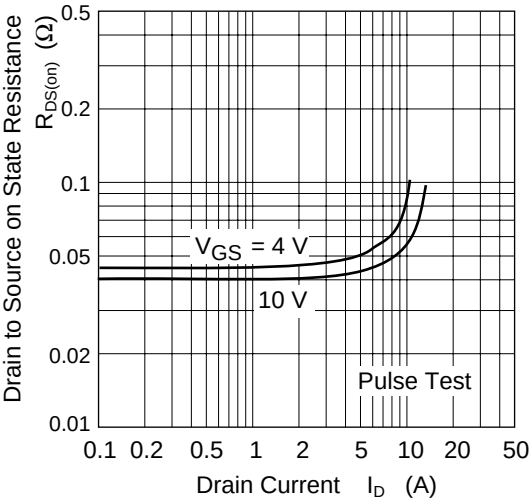
Note 6:
When using the glass epoxy board
(FR4 40 x 40 x 1.6 mm)



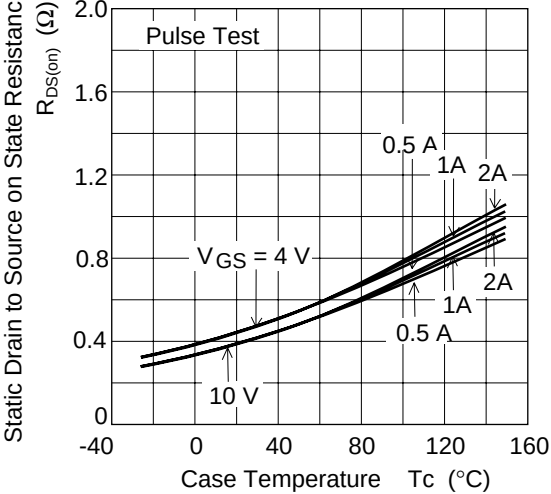
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



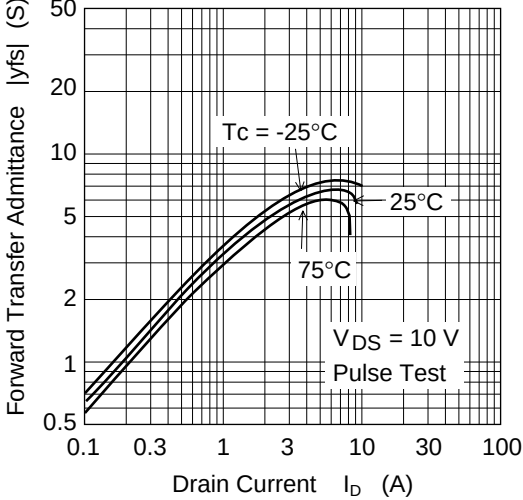
Static Drain to Source on State Resistance
vs. Drain Current

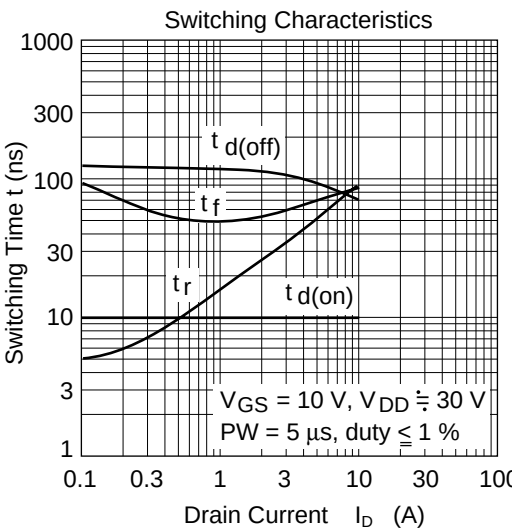
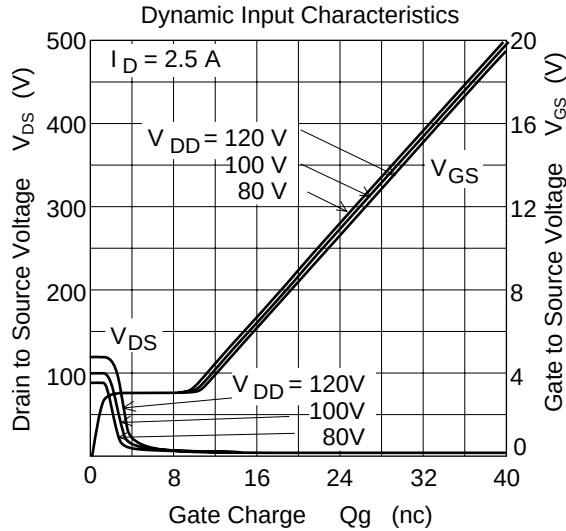
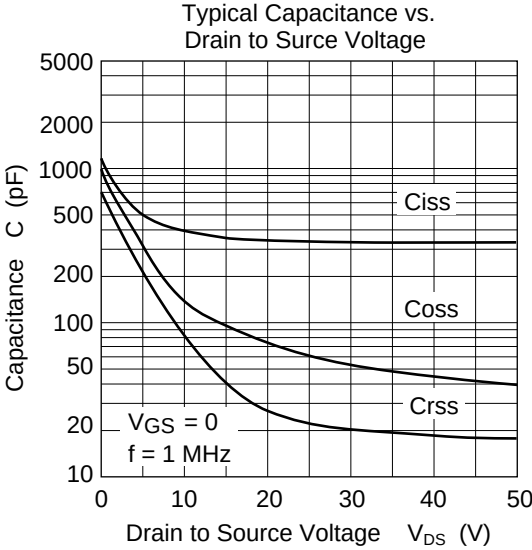
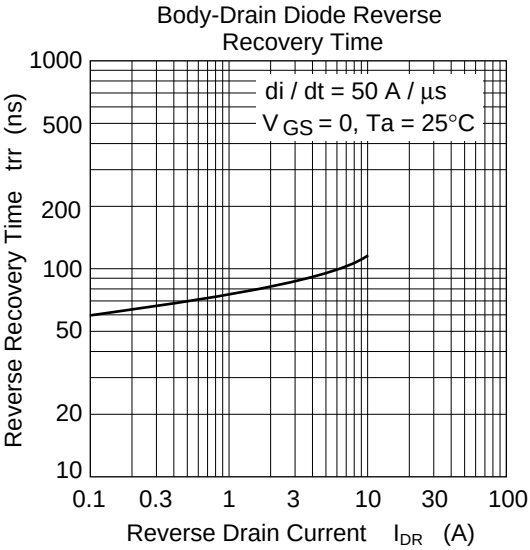


Drain to Source on State Resistance
vs. Temperature

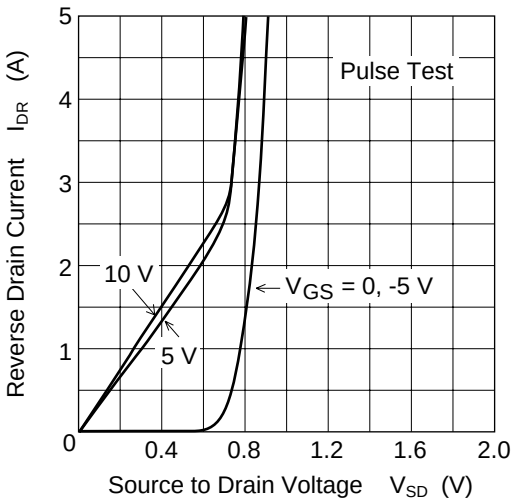


Forward Transfer Admittance vs.
Drain Current

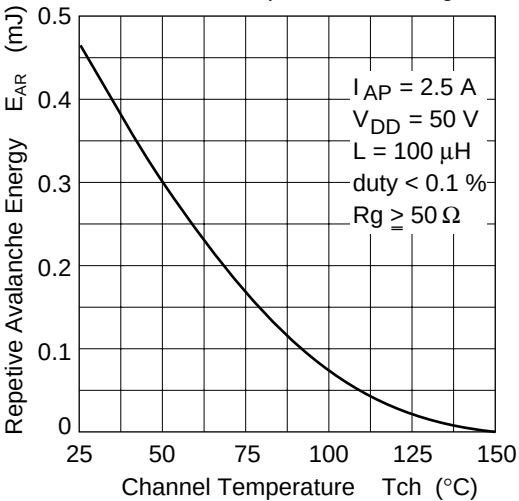




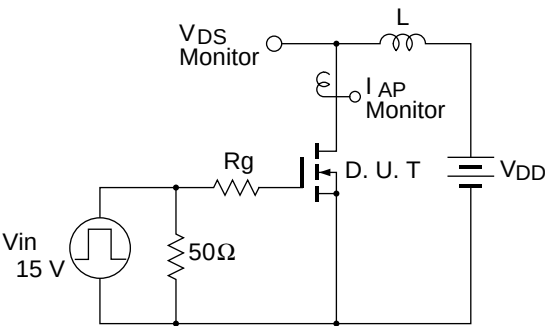
Reverse Drain Current vs.
Source to Drain Voltage



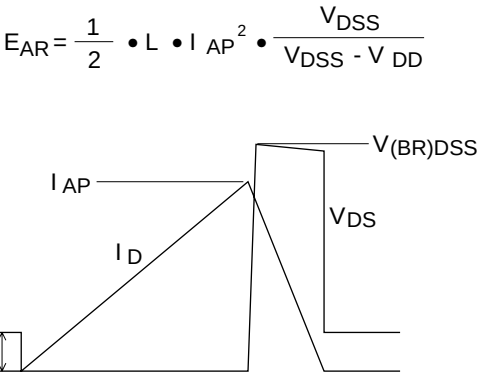
Maximum Avalanche Energy vs.
Channel Temperature Derating



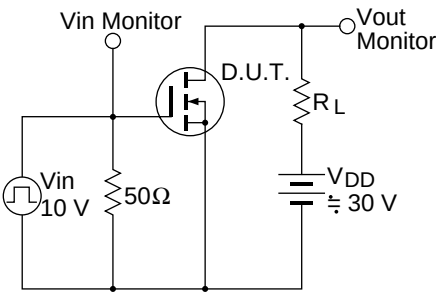
Avalanche Test Circuit



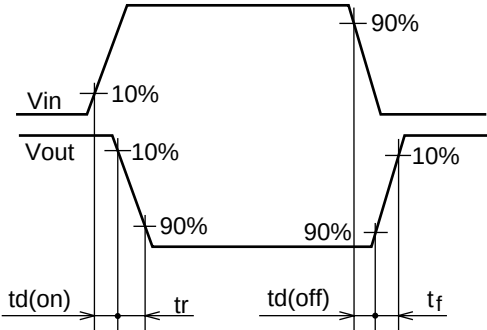
Avalanche Waveform

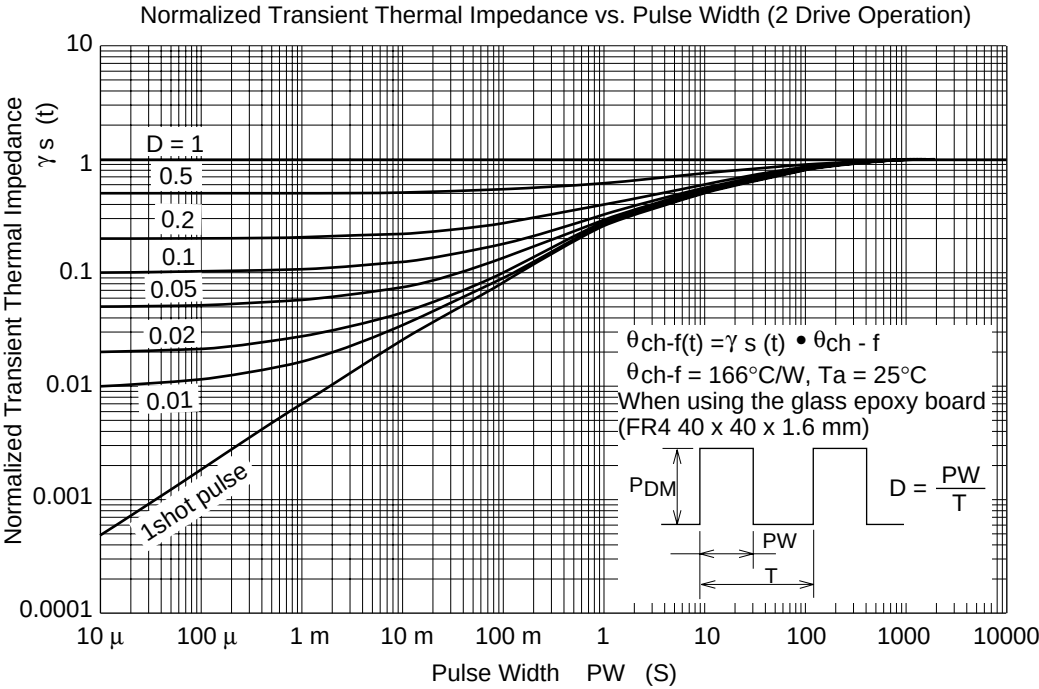
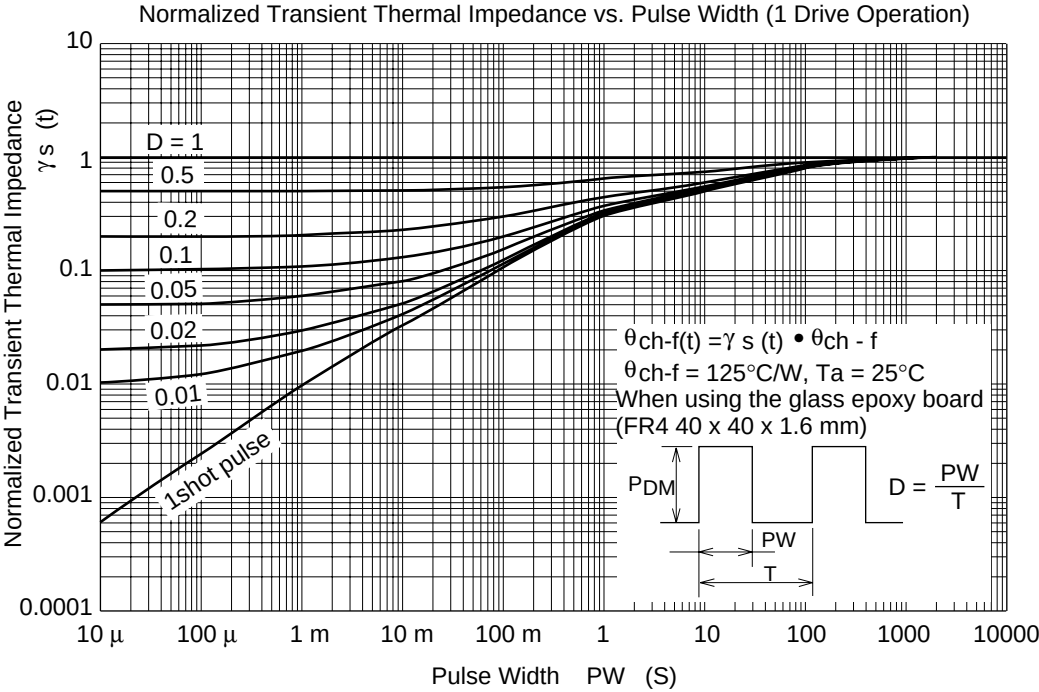


Switching Time Test Circuit



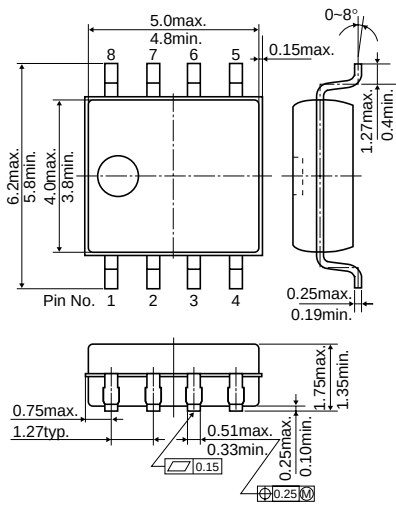
Switching Time Waveform





Package Dimensions

Unit: mm



Hitachi Code	FP-8DA
JEDEC	—
EIAJ	—

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