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# HM628128D Series

1 M SRAM (128-kword  $\times$  8-bit)

# HITACHI

ADE-203-996B (Z)

Rev. 1.0

Aug. 23, 1999

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## Description

The Hitachi HM628128D Series is 1-Mbit static RAM organized 131,072-kword  $\times$  8-bit. HM628128D Series has realized higher density, higher performance and low power consumption by employing Hi-CMOS process technology. The HM628128D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has package variations of standard 32-pin plastic DIP, standard 32-pin plastic SOP and standard 32-pin plastic TSOPI.

## Features

- Single 5 V supply: 5 V  $\pm$  10%
- Access time: 55 ns (max)
- Power dissipation
  - Active: 30 mW/MHz (typ)
  - Standby: 10  $\mu$ W (typ)
- Completely static memory.
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible all inputs
- Battery backup operation
  - 2 chip selection for battery backup

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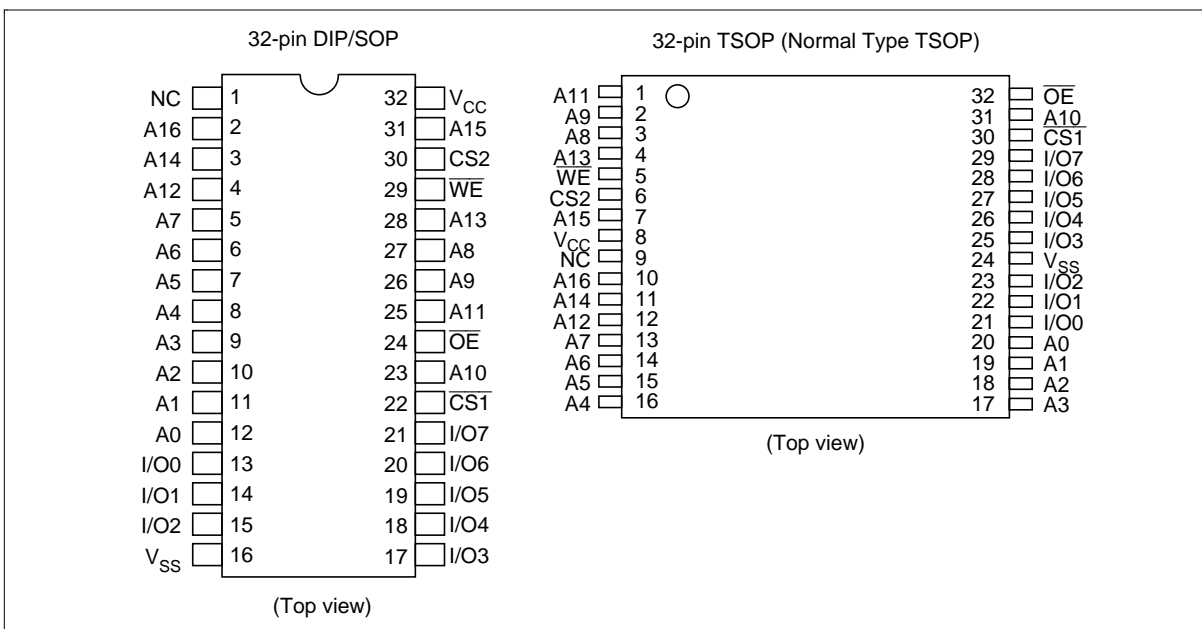
## HM628128D Series

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### Ordering Information

Type No.	Access time	Package
HM628128DLP-5SL	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628128DLFP-5SL	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628128DLT-5SL	55 ns	Normal-bend type 8 × 20 mm 32-pin plastic TSOP I (TFP-32D)

## Pin Arrangement

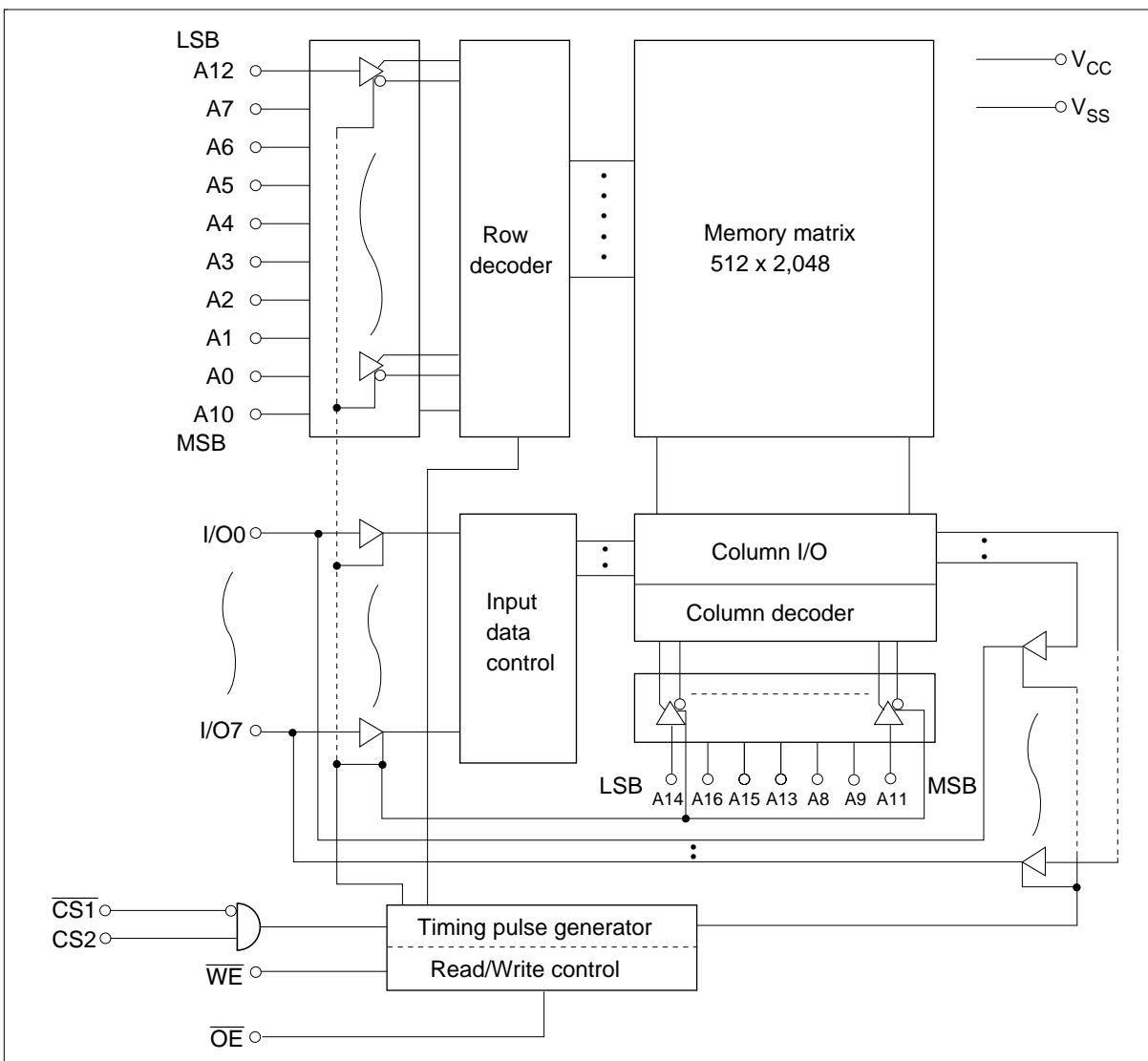


## Pin Description

Pin name	Function
A0 to A16	Address input
I/O0 to I/O7	Data input/output
CS1	Chip select 1
CS2	Chip select 2
WE	Write enable
OE	Output enable
V <sub>CC</sub>	Power supply
V <sub>SS</sub>	Ground
NC	No connection

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### Block Diagram



**Operation Table**

$\overline{\text{CS1}}$	$\text{CS2}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O	Operation
H	×	×	×	High-Z	Standby
×	L	×	×	High-Z	Standby
L	H	H	L	Dout	Read
L	H	L	H	Din	Write
L	H	L	L	Din	Write
L	H	H	H	High-Z	Output disable

Note: H:  $V_{IH}$ , L:  $V_{IL}$ , ×:  $V_{IH}$  or  $V_{IL}$

**Absolute Maximum Ratings**

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	−0.5 to +7.0	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	−0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−20 to +85	°C

Notes: 1.  $V_T$  min: −1.5 V for pulse half-width ≤ 30 ns

2. Maximum voltage is +7.0 V

**DC Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V	
	$V_{SS}$	0	0	0	V	
Input high voltage	$V_{IH}$	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	$V_{IL}$	−0.3	—	0.8	V	1
Ambient temperature range	Ta	−20	—	70	°C	

Note: 1.  $V_{IL}$  min: −1.5 V for pulse half-width ≤ 30 ns

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### DC Characteristics

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	$ I_{Li} $	—	—	1	$\mu A$	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	$ I_{Lo} $	—	—	1	$\mu A$	$\overline{CS1} = V_{IH} \text{ or } CS2 = V_{IL} \text{ or } OE = V_{IH} \text{ or } WE = V_{IL}, V_{IO} = V_{SS} \text{ to } V_{CC}$
Operating current	$I_{CC}$	—	—	15	mA	$\overline{CS1} = V_{IL}, CS2 = V_{IH}, \text{ others} = V_{IH}/V_{IL}, I_{IO} = 0 \text{ mA}$
Average operating current	$I_{CC1}$	—	—	60	mA	Min cycle, duty = 100% $I_{IO} = 0 \text{ mA}, \overline{CS1} = V_{IL}, CS2 = V_{IH}, \text{ Others} = V_{IH}/V_{IL}$
	$I_{CC2}$	—	6	20	mA	Cycle time = 1 $\mu s$ , duty = 100%, $I_{IO} = 0 \text{ mA}, \overline{CS1} \leq 0.2 \text{ V},$ $CS2 \geq V_{CC} - 0.2 \text{ V},$ $V_{IH} \geq V_{CC} - 0.2 \text{ V},$ $V_{IL} \leq 0.2 \text{ V}$
Standby current	$I_{SB}$	—	—	2	mA	(1) $\overline{CS1} = V_{IH}, CS2 = V_{IH}, \text{ or}$ (2) $CS2 = V_{IL}$
	$I_{SB1}^{*2}$	—	2	50	$\mu A$	0 V $\leq V_{in}$ (1) 0 V $\leq CS2 \leq 0.2 \text{ V}$ or (2) $\overline{CS1} \geq V_{CC} - 0.2 \text{ V},$ $CS2 \geq V_{CC} - 0.2 \text{ V}$
Output high voltage	$V_{OH}$	2.4	—	—	V	$I_{OH} = -1 \text{ mA}$
Output low voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1 \text{ mA}$

Notes: 1. Typical values are at  $V_{CC} = 5.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.  
2. This characteristics is guaranteed only for L-SL version.

### Capacitance ( $T_a = +25^\circ\text{C}$ , $f = 1 \text{ MHz}$ )

Parameter	Symbol	Typ	Max	Unit	Test conditions	Note
Input capacitance	$C_{in}$	—	8	pF	$V_{in} = 0 \text{ V}$	1
Input/output capacitance	$C_{IO}$	—	10	pF	$V_{IO} = 0 \text{ V}$	1

Note: 1. This parameter is sampled and not 100% tested.

**AC Characteristics** ( $T_a = -20$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5.0\text{ V} \pm 10\%$ , unless otherwise noted.)

**Test Conditions**

- Input pulse levels:  $V_{IL} = 0.8\text{ V}$ ,  $V_{IH} = 2.4\text{ V}$
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.5 V
- Output timing reference level: 1.5 V
- Output load: 1 TTL Gate+ CL (30pF) (Including scope and jig)

**Read Cycle**

		HM628128D			
		-5			
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time					
1 TTL Gate + CL (30pF)	t <sub>RC</sub>	55	—	ns	
1 TTL Gate + CL (100pF)	t <sub>RC</sub>	70	—	ns	
Address access time					
1 TTL Gate + CL (30pF)	t <sub>AA</sub>	—	55	ns	
1 TTL Gate + CL (100pF)	t <sub>AA</sub>	—	70	ns	
Chip select access time					
1 TTL Gate + CL (30pF)	t <sub>ACS1</sub>	—	55	ns	
1 TTL Gate + CL (100pF)	t <sub>ACS1</sub>	—	70	ns	
1 TTL Gate + CL (30pF)	t <sub>ACS2</sub>	—	55	ns	
1 TTL Gate + CL (100pF)	t <sub>ACS2</sub>	—	70	ns	
Output enable to output valid					
1 TTL Gate + CL (30pF)	t <sub>OE</sub>	—	30	ns	
1 TTL Gate + CL (100pF)	t <sub>OE</sub>	—	35	ns	
Output hold from address change	t <sub>OH</sub>	10	—	ns	
Chip selection to output in low-Z	t <sub>CLZ1</sub>	10	—	ns	2, 3
	t <sub>CLZ2</sub>	10	—	ns	2, 3
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	ns	2, 3
Chip deselection to output in high-Z	t <sub>CHZ1</sub>	0	20	ns	1, 2, 3
	t <sub>CHZ2</sub>	0	20	ns	1, 2, 3
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	ns	1, 2, 3

## HM628128D Series

### Write Cycle

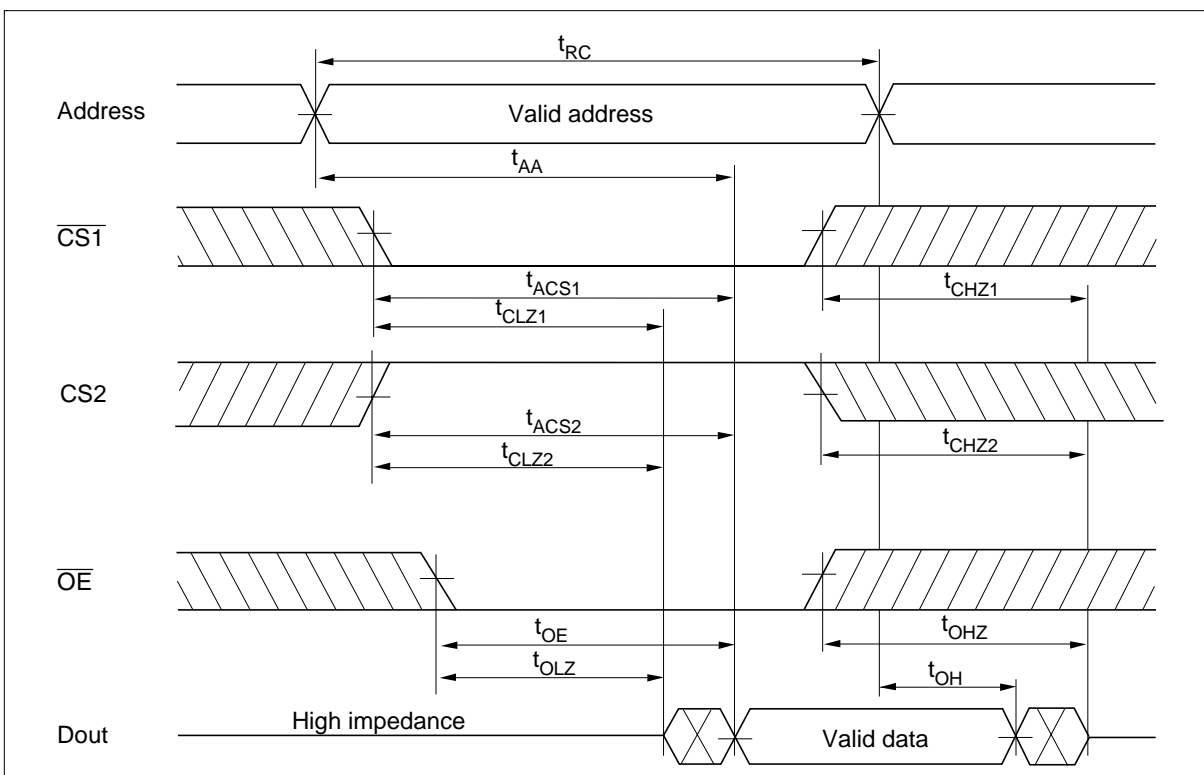
Parameter	Symbol	HM628128D		Unit	Notes
		-5			
		Min	Max		
Write cycle time	$t_{WC}$	55	—	ns	
Address valid to end of write	$t_{AW}$	50	—	ns	
Chip selection to end of write	$t_{CW}$	50	—	ns	5
Write pulse width	$t_{WP}$	40	—	ns	4, 13
Address setup time	$t_{AS}$	0	—	ns	6
Write recovery time	$t_{WR}$	0	—	ns	7
Data to write time overlap	$t_{DW}$	25	—	ns	
Data hold from write time	$t_{DH}$	0	—	ns	
Output active from output in high-Z	$t_{OW}$	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	20	ns	1, 2, 8
$\overline{WE}$ to output in high-Z	$t_{WHZ}$	0	20	ns	1, 2, 8

- Notes:
1.  $t_{CHZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
  2. This parameter is sampled and not 100% tested.
  3. At any given temperature and voltage condition,  $t_{HZ}$  max is less than  $t_{LZ}$  min both for a given device and from device to device.
  4. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS1}$ , a high CS2, and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high, and  $\overline{WE}$  going low. A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low, and  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
  5.  $t_{CW}$  is measured from  $\overline{CS1}$  going low or CS2 going high to the end of write.
  6.  $t_{AS}$  is measured from the address valid to the beginning of write.
  7.  $t_{WR}$  is measured from the earlier of  $\overline{WE}$  or  $\overline{CS1}$  going high or CS2 going low to the end of write cycle.
  8. During this period, I/O pins are in the output state; therefore, the input signals of the opposite phase to the outputs must not be applied.
  9. If the  $\overline{CS1}$  goes low or CS2 going high simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the output remain in a high impedance state.
  10. Dout is the same phase of the write data of this write cycle.
  11. Dout is the read data of next address.
  12. If  $\overline{CS1}$  is low and CS2 high during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
  13. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$



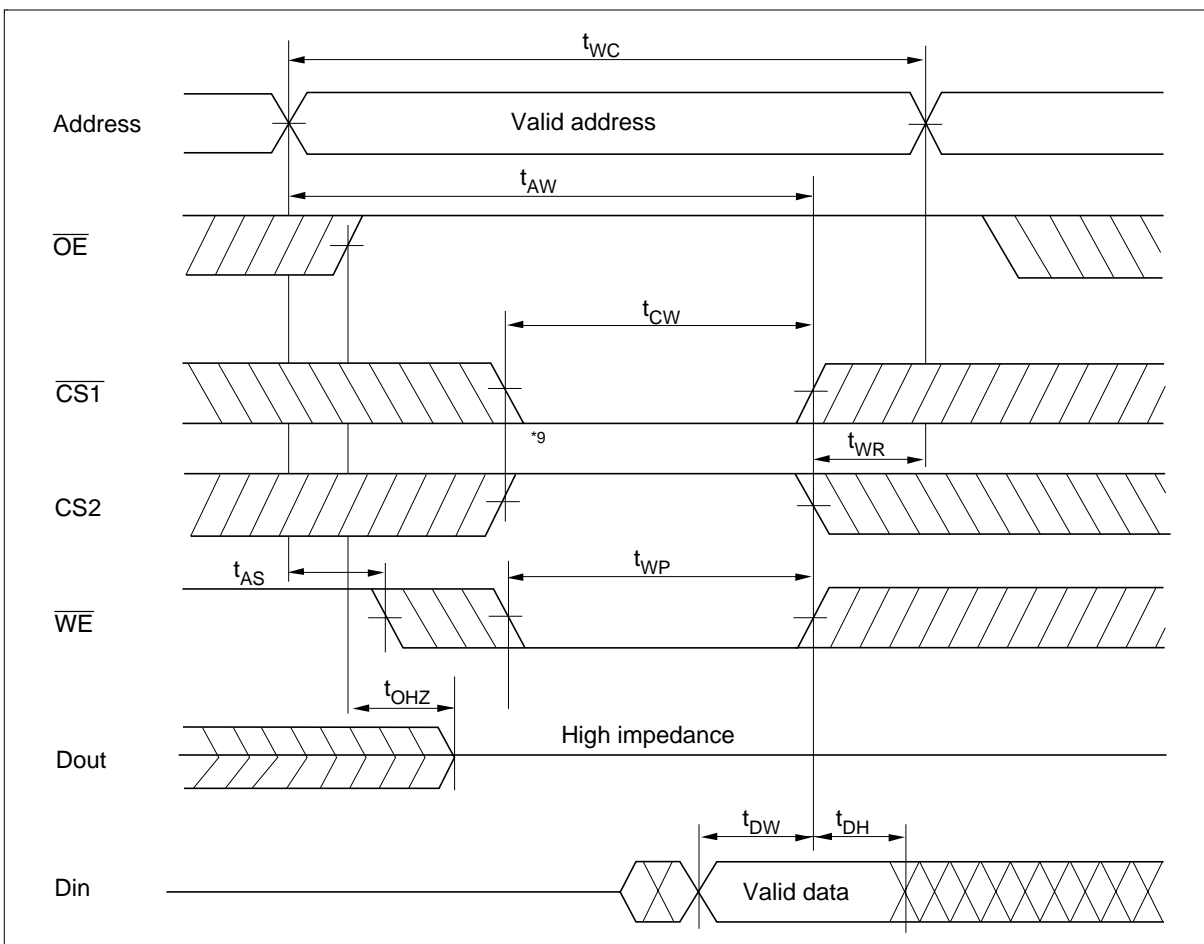
# Timing Waveforms

Read Cycle ( $\overline{WE} = V_{IH}$ )

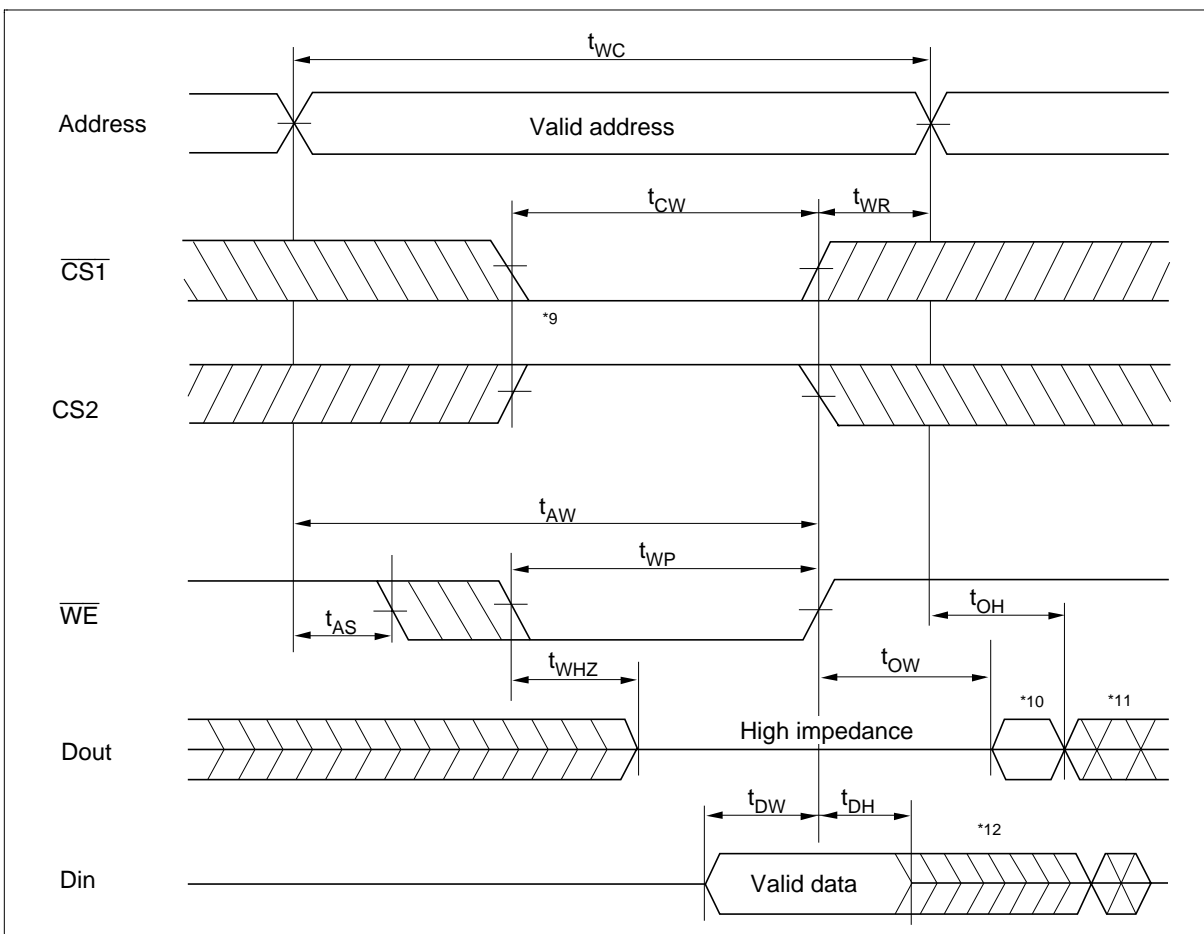


## HM628128D Series

### Write Cycle (1) ( $\overline{\text{OE}}$ Clock)



Write Cycle (2) ( $\overline{OE} = V_{IL}$ )



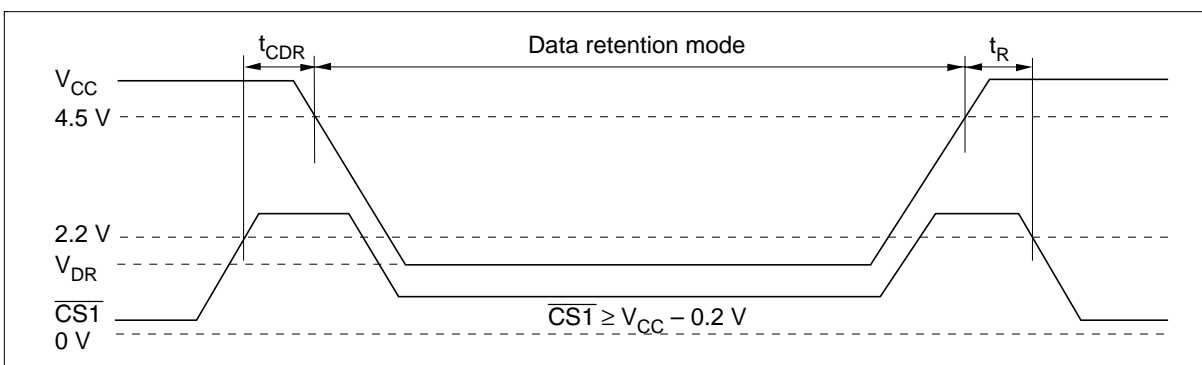
## HM628128D Series

### Low $V_{CC}$ Data Retention Characteristics ( $T_a = -20$ to $+70^\circ\text{C}$ )

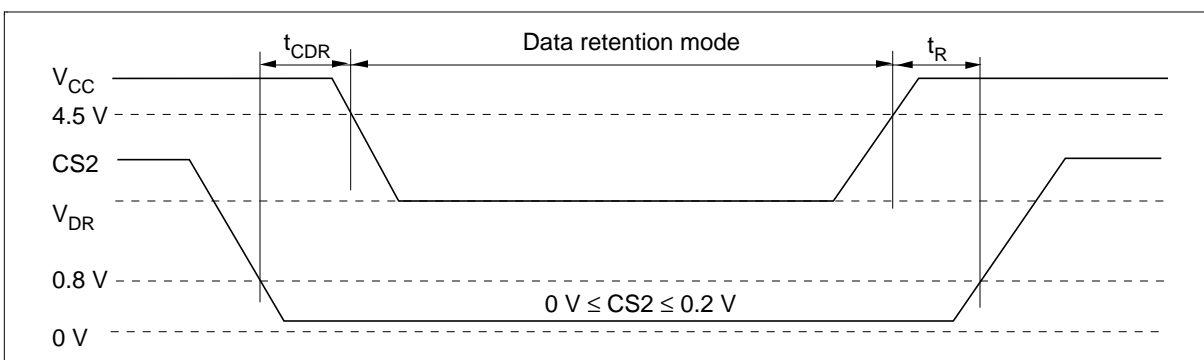
Parameter	Symbol	Min	Typ <sup>*3</sup>	Max	Unit	Test conditions <sup>*2</sup>
$V_{CC}$ for data retention	$V_{DR}$	2.0	—	—	V	$V_{in} \geq 0\text{V}$ (1) $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$ $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{V}$
Data retention current	$I_{CCDR}$ <sup>*1</sup>	—	1.0	15	$\mu\text{A}$	$V_{CC} = 3.0\text{V}$ , $V_{in} \geq 0\text{V}$ (1) $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$ , $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{V}$
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	$t_{RC}$ <sup>*4</sup>	—	—	ns	

- Notes: 1. This characteristic is guaranteed only for L-SL-version, 3  $\mu\text{A}$  max. at  $T_a = -20$  to  $+40^\circ\text{C}$ .  
2. CS2 controls address buffer,  $\overline{\text{WE}}$  buffer,  $\overline{\text{CS1}}$  buffer,  $\overline{\text{OE}}$  buffer, and Din buffer. If CS2 controls data retention mode,  $V_{in}$  levels (address,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{CS1}}$ , I/O) can be in the high impedance state. If  $\overline{\text{CS1}}$  controls data retention mode, CS2 must be  $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{V}$  or  $0\text{V} \leq \overline{\text{CS2}} \leq 0.2\text{V}$ . The other input levels (address,  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ , I/O) can be in the high impedance state.  
3. Typical values are at  $V_{CC} = 3.0\text{V}$ ,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.  
4.  $t_{RC}$  = read cycle time.

### Low $V_{CC}$ Data Retention Timing Waveform (1) ( $\overline{\text{CS1}}$ Controlled)



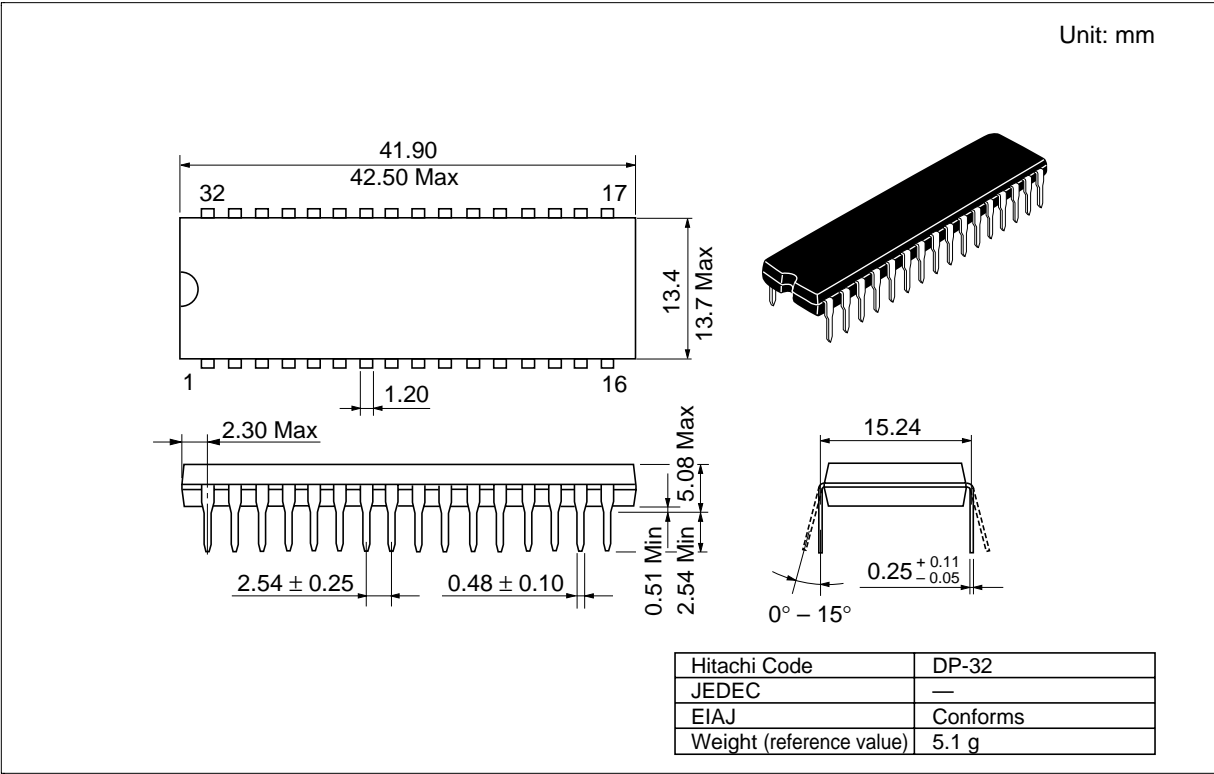
Low  $V_{CC}$  Data Retention Timing Waveform (2) (CS2 Controlled)



HM628128D Series

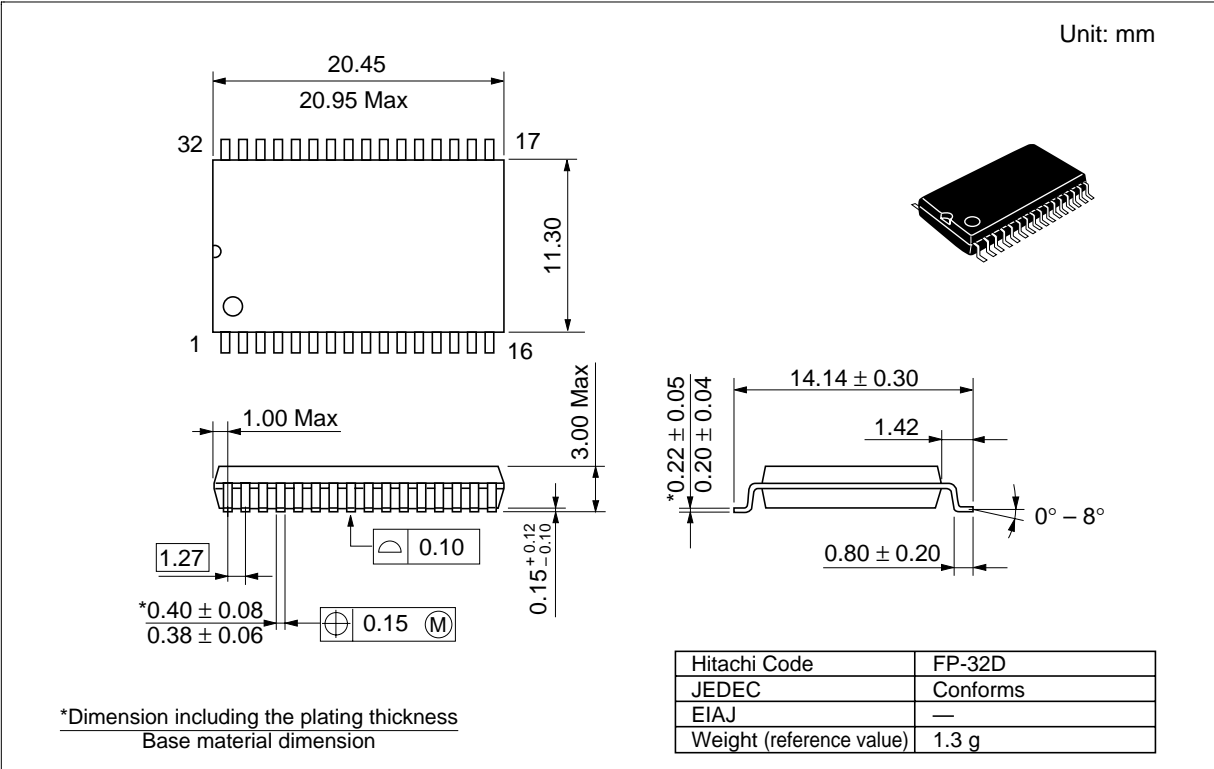
Package Dimensions

HM628128DLP Series (DP-32)



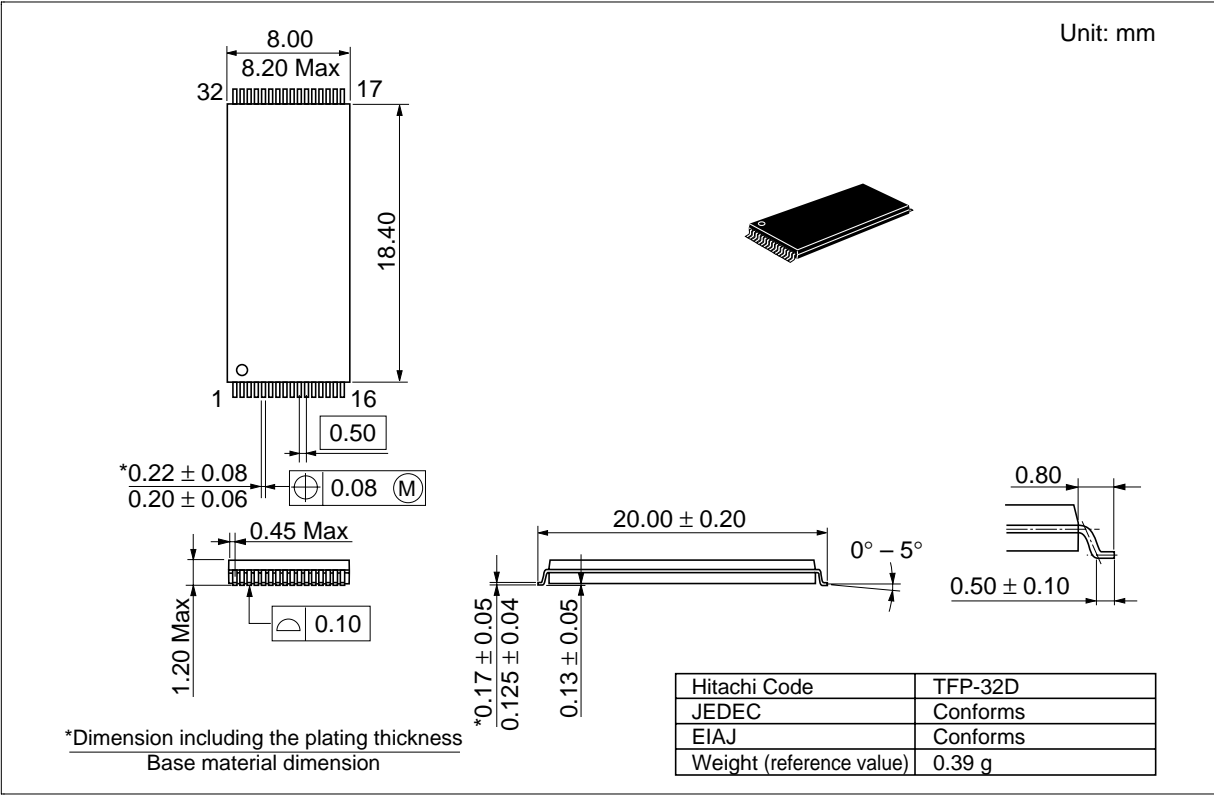
HM628128D Series

HM628128DLFP Series (FP-32D)



HM628128D Series

HM628128DLT Series (TFP-32D)





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## HM628128D Series

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### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jan. 20, 1999	Initial issue	H.Nakamura	K. Imato
0.1	Jul. 8, 1999	Deletion of HM628128D-7 Series Deletion of HM628128DLTS Series (TFP-32DC) and HM628128DLR Series (TFP-32DR) Deletion of L-version and L-UL version DC Characteristics $I_{SB1}$ max: 100 $\mu$ A to 50 $\mu$ A Deletion of Notes2 and 4 AC Characteristics Test Conditions Output load: 1TTL Gate+CL(50 pF) to 1TTL Gate+CL(30 pF) $t_{DW}$ min: 20 ns to 25 ns Correct error: Notes4 Low $V_{CC}$ Data Retention Characteristics Deletion of Notes1 and 3	H.Nakamura	K. Imato
1.0	Aug. 23, 1999	Deletion of Preliminary		