HD61604/HD61605

(Segment Type LCD Driver)

HITACHI

Description

The HD61604 and the HD61605 are liquid crystal display driver LSIs with TTL and CMOS compatible interface. Each of the LSIs can be connected to various microprocessors.

Several types of liquid crystal displays can be connected to the HD61604 according to the applications because of the software-controlled liquid crystal display drive method.

The HD61605 is a liquid crystal display driver LSI only for static drive and has 64 segment outputs that can display 8 digits per chip.

Features

- Low current consumption
  - Can drive from a battery power supply (100 µA max. on 5 V)
  - Standby input enables standby operation at lower current consumption (5 µA max. on 5 V)

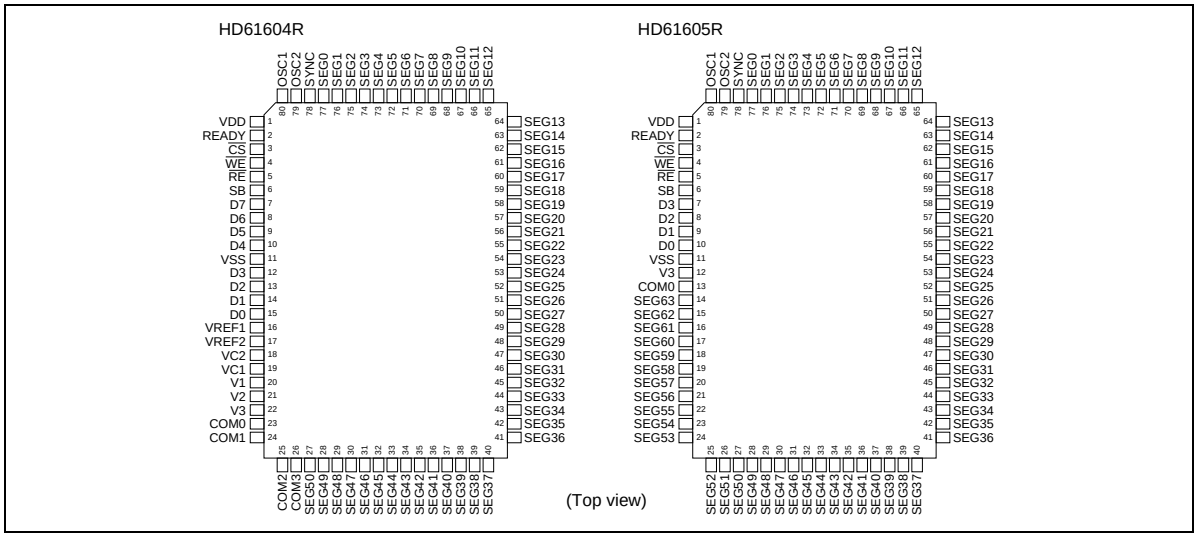
Ordering Information

Type No.	Package
HD61604R	80-pin plastic QFP (FP-80)
HD61605R	

Versatile Segment Driving Capacity

Type No.	Driving	Method	Display Segments	Example of Use	Frame Freq (Hz)at f_{osc} = 100 kHz
HD61604R	Static		51	8 segments × 6 digits + 3 marks	98
	1/2 bias	1/2 duty cycle	102	8 segments × 12 digits + 6 marks	195
	1/3 bias	1/3 duty cycle	153	9 segments × 17 digits	521
		1/4 duty cycle	204	8 segments × 25 digits + 4 marks	781
HD61605R	Static		64	8 segments × 8 digits	98

Pin Arrangement



Block Diagram

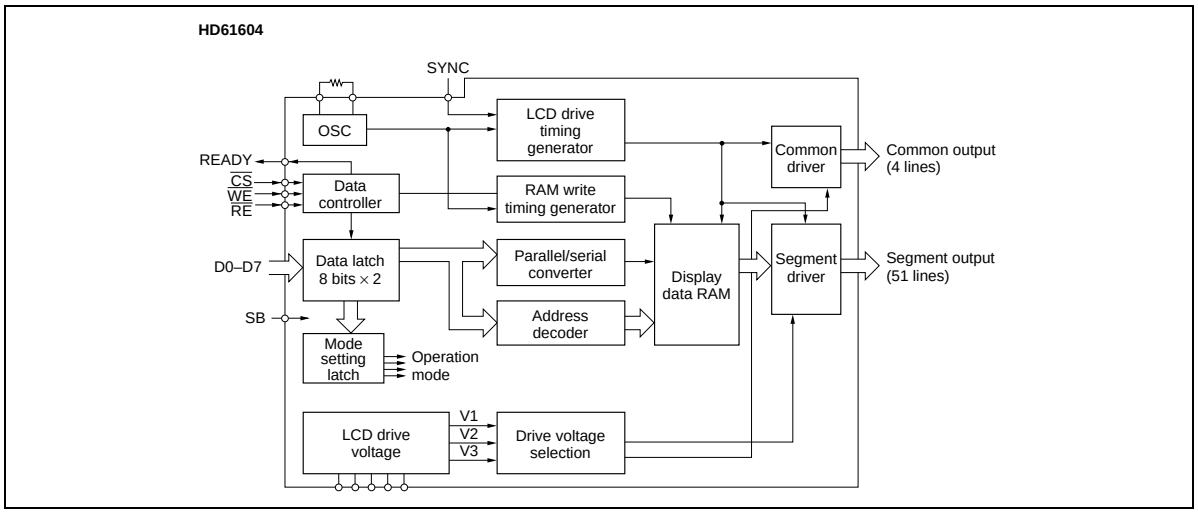


Figure 1 HD61604 Block Diagram

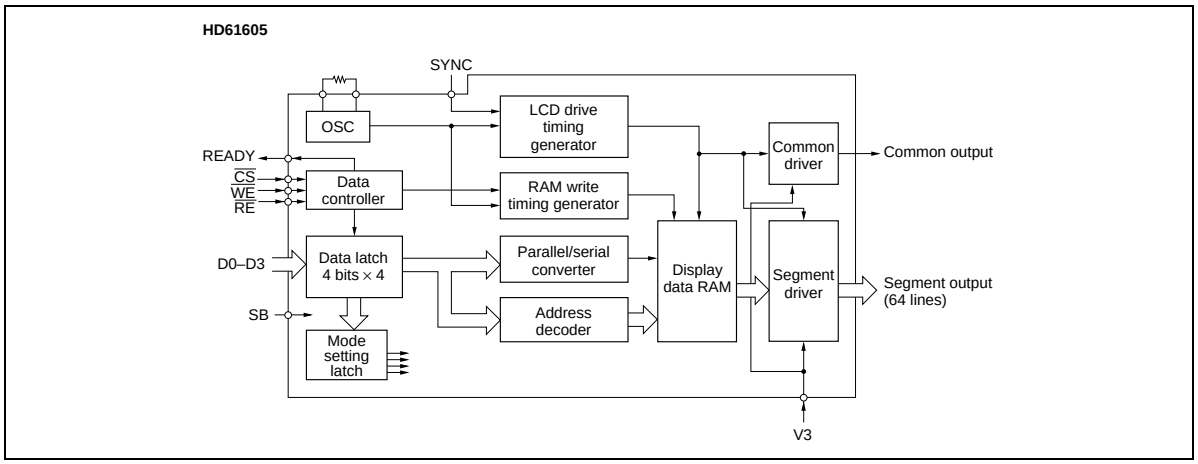


Figure 2 HD61605 Block Diagram

Pin Functions

Table 1 shows the HD61604 pin description. Table 2 shows the HD61605 pin description.

HD61604 Pin Function

READY (Ready): During data setting in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D0 to D7 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the 1st byte data.

SB (Standby): High level input stops the LSI operations.

1. Stops oscillation and clock input.
2. Stops LCD driver.
3. Stops writing data into display RAM.

D0–D7 (Data Bus): Data input pin from which 8-bit × 2-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chip applications. LCD drive timing generator is reset by high input. LCD is off.

COM0–COM3 (Common): LCD common (backplate) drive output.

SEG0–SEG50 (Segment): LCD segment drive output.

V1, V2, V3 (LCD Voltage): Power supply for LCD drive.

OSC1, OSC2 (Oscillator): Attach external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

VC1, VC2: Do not connect any wire.

VREF1: Connect this pin to V1 pin.

VREF2: Hold at VDD level.

VDD: Positive power supply.

VSS: Negative power supply.

HD61605 Pin Function

READY (Ready): During data setting in the display data RAM and mode setting latch in the LSI after data transfer, low is output to the READY pin to inhibit the next data input.

There are two modes: one in which low is output only when both of $\overline{CS}$ and $\overline{RE}$ are low, and the other in which low is output regardless of $\overline{CS}$ and $\overline{RE}$.

$\overline{CS}$ (Chip Select): Chip select input. Data can be written only when this pin is low.

$\overline{WE}$ (Write Enable): Write enable input. Input data of D0 to D3 is latched at the positive edge of $\overline{WE}$.

$\overline{RE}$ (Reset): Resets the input data byte counter. After both of $\overline{CS}$ and $\overline{RE}$ are low, the first data is recognized as the first byte data.

SB (Standby): High level input stops the LSI operation.

1. Stops oscillation and clock input.
2. Stops LCD driver.
3. Stops writing data into display RAM.

D0–D3: Data input pin from which 4-bit × 4-byte data is input.

SYNC (Synchronous): Synchronous input for 2 or more chips application. LCD drive timing generator is reset by high input. LCD is off.

COM0 (Common): LCD common (backplate) drive output**.**

SEG0–SEG63 (Segment): LCD segment drive output.

OSC1, OSC2 (Oscillator): Attach external R to these pins for oscillation. An external clock (100 kHz) can be input from OSC1.

V3 (LCD Voltage): Power supply input for LCD drive.

Voltage between VDD and V3 is used as drive voltage.

VSS: Negative power supply.

VDD: Positive power supply.

Table 1 HD61604 Pin Description

Pin Name	No. of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D0–D7	8	Input	MCU
SYNC	1	Input	MCU
COM0–COM3	4	Output	LCD
SEG0–SEG50	51	Output	LCD
V1, V2, V3	3	Power supply	External R
OSC1, OSC2	2	Input, output	External R
VC1, VC2	2	Output	
VREF1	1	Input	V1
VREF2	1	Input	VDD
VDD	1	Power supply	
VSS	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Table 2 HD61605 Pin Description

Pin Name	No. of Lines	Input/Output	Connected to
READY	1	NMOS open drain output	MCU
$\overline{CS}$	1	Input	MCU
$\overline{WE}$	1	Input	MCU
$\overline{RE}$	1	Input	MCU
SB	1	Input	MCU
D0–D3	4	Input	MCU
SYNC	1	Input	MCU
COM0	1	Output	LCD
SEG0–SEG63	64	Output	LCD
OSC1, OSC2	2	Input, output	External R
V3	1	Input	Power supply
VSS	1	Power supply	
VDD	1	Power supply	

Note: Logic polarity is positive.
1 = high = active.

Display RAM

HD61604 Display RAM

The HD61604 has an internal display RAM shown in Figure 3. Display data is stored in the RAM, or is read according to the LCD drive timing to display on the LCD. One bit of the RAM corresponds to 1 segment of LCD. Note that some bits of the RAM cannot be displayed depending on LCD drive modes.

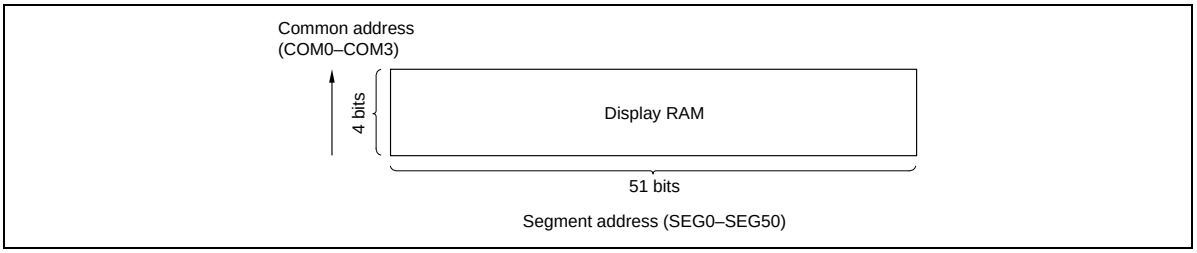


Figure 3 Display RAM (HD61604)

Reading Data from HD61604 Display RAM: A display RAM segment address corresponds to a segment output. The data at segment address SEGn is output to segment output SEGn pin.

A common address corresponds to the output timing of a common output and a segment output. The same common address data is simultaneously read. The data of display RAM is reproduced on the LCD panel.

The following shows the correspondence between the 7-segment type LCD connection and the display RAM in each mode.

1. Static drive

   In the static drive, only the column of COM0 of display RAM is output. COM1 to COM3 are not displayed (Figure 4).
2. 1/2 duty cycle drive

   In the 1/2 duty cycle drive, the columns of COM0 and COM1 of display RAM are output in time sharing. The columns of COM2 and COM3 are not displayed (Figure 5).

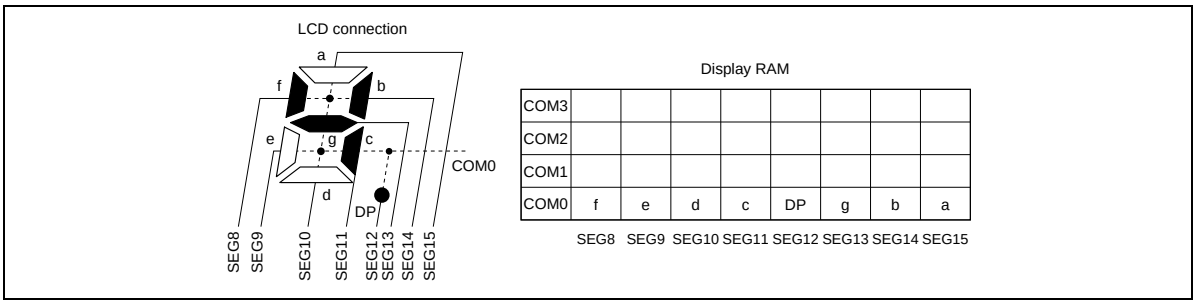


Figure 4 Example of Correspondence between LCD Connection and Display RAM (Static Drive, HD61604)

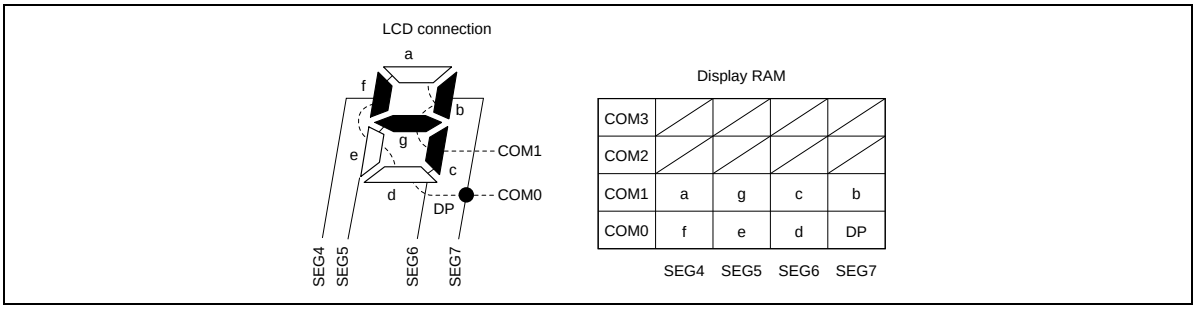


Figure 5 Example of Correspondence between LCD Connection and Display RAM (1/2 Duty Cycle, HD61604)

3. 1/3 duty cycle drive

   In the 1/3 duty cycle drive, the columns of COM0 to COM2 are output in time sharing. No column of COM3 is displayed. “y” cannot be rewritten by display data (input on an 8-segment basis). Please use bit manipulation in turning on/off the display of “y” cycle (Figure 6).

4. 1/4 duty cycle drive

   In the 1/4 duty cycle drive, all the columns of COM0 to COM3 are displayed (Figure 7).

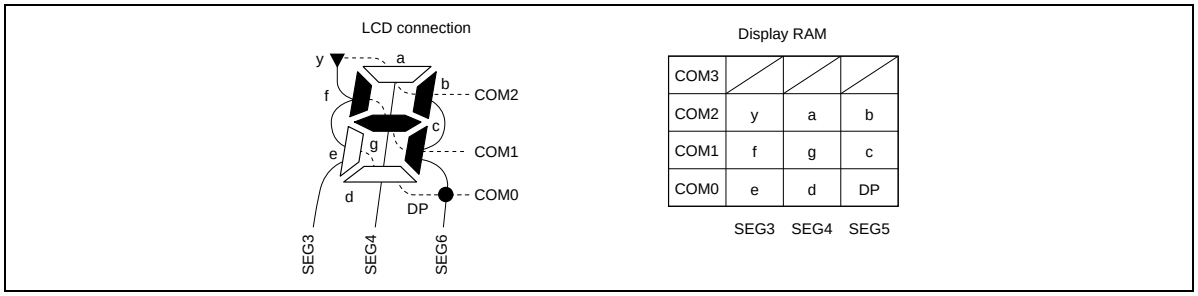


Figure 6 Example of Correspondence between LCD Connection and Display RAM (1/3 Duty Cycle, HD61604)

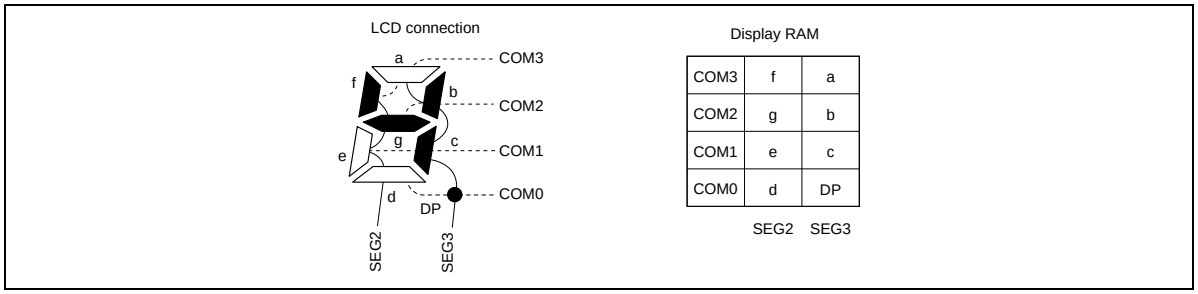


Figure 7 Example of Correspondence between LCD Connection and Display RAM (1/4 Duty Cycle, HD61604)

Writing Data into HD61604 Display RAM: Data is written into the display RAM in the following five methods:

1. Bit manipulation
   Data is written into any bit of RAM on a bit basis.
2. Static display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.
3. 1/2 duty cycle display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/2 duty cycle drive.
4. 1/3 duty cycle display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/3 duty cycle drive.
5. 1/4 duty cycle display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of 1/4 duty cycle drive.

The RAM area and the allocation of the segment data for 1-digit display depend on the drive methods as described in the section of “Reading Data from Display RAM”.

8-bit data is written on a digit basis corresponding to the above duty cycle driving methods. The digits are allocated as shown in Figure 8. As the data can be transferred on a digit basis from a microprocessor, transfer efficiency is improved by allocating the LCD pattern according to the allocation of each bit data of the digit in the data RAM.

Figure 8 shows the digit address (displayed as Adn) to specify the store address of the transferred 8-bit data on a digit basis.

Figure 9 shows the correspondence between each segment in an Adn and the 8-bit input data.

When data is transferred on a digit basis 8-bit display data and digit address should be specified as described above.

However, when the digit address is Ad6 of static, Ad12 of 1/2 duty cycle, or Ad25 for 1/4 duty cycle, display RAM does not have enough bits for the data. Thus the extra bits of the input 8-bit data are ignored.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data, a segment address (6 bits) and a common address (2 bits) should be specified.

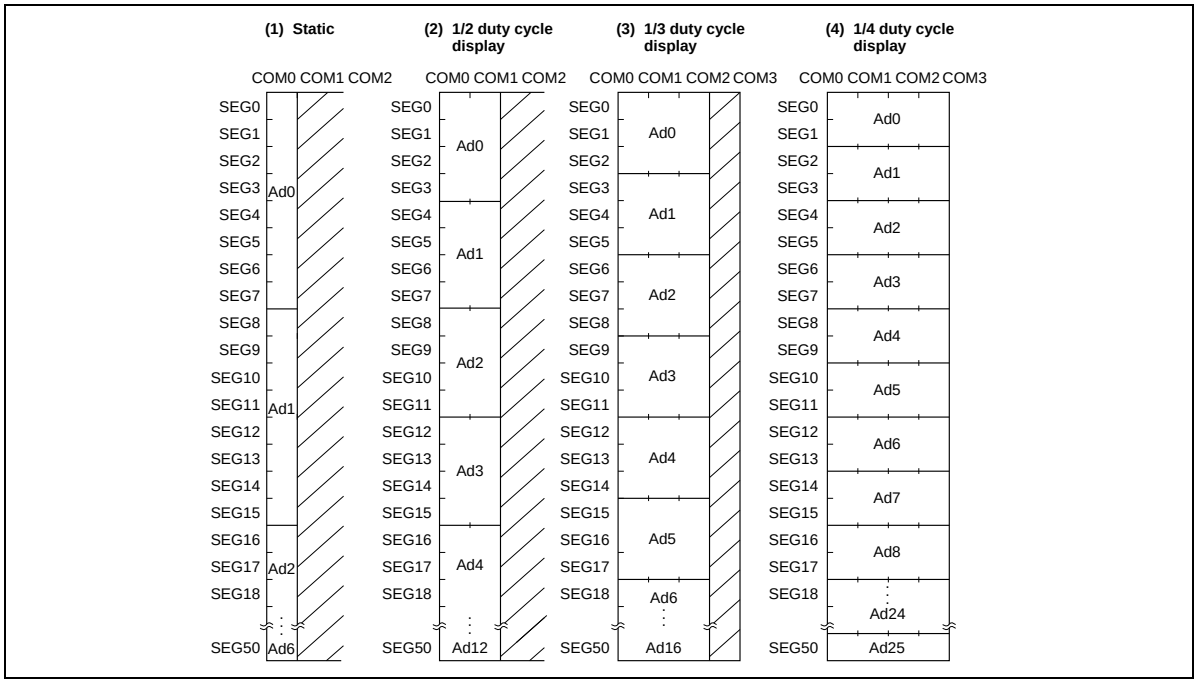


Figure 8 Allocation of Digits (HD61604)

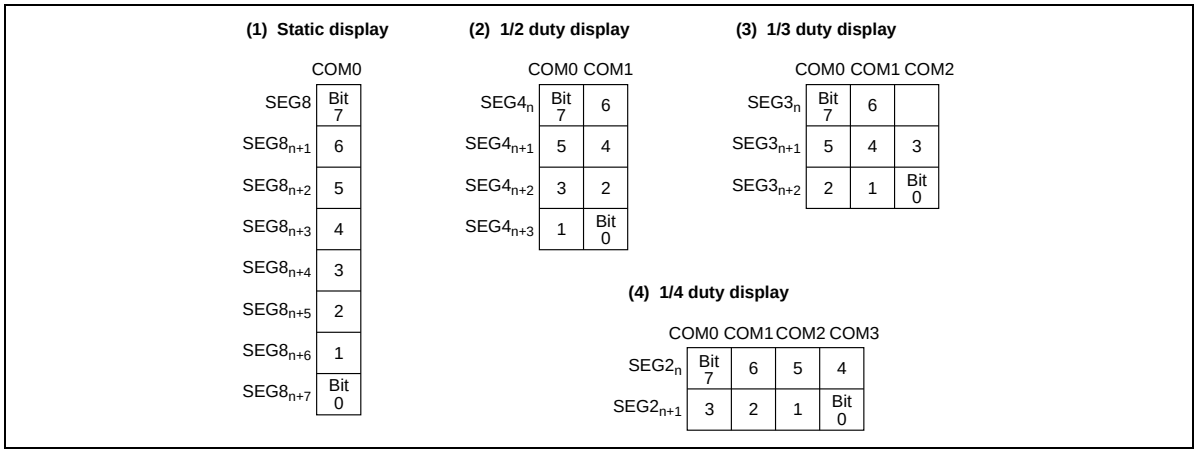


Figure 9 Bit Assignment in an Adn (HD61604)

HD61605 Display RAM

The HD61605 has an internal display RAM as shown in Figure 10. Display data is stored in the RAM and output to the segment output pin.

Reading Data from HD61605 Display RAM: Each bit of the display RAM corresponds to an LCD segment. The data at segment address SEGn is output to segment output SEGn pin. Figure 11 shows the correspondence between the 7-segment type LCD connection and the display RAM.

Writing Data into HD61605 Display RAM: Data is written into the display RAM in the following two methods:

1. Bit manipulation
   Data is written into any bit of RAM on a bit basis.
2. Static display mode
   8-bit data is written on a digit basis according to the 7-segment type LCD pattern of static drive.

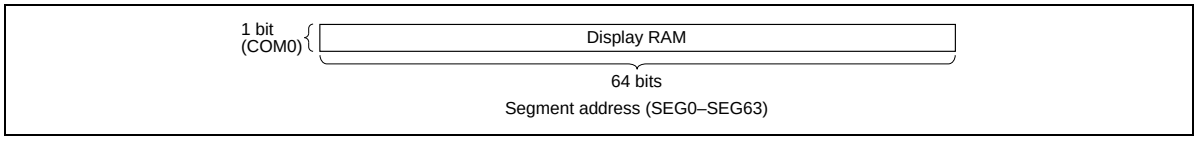


Figure 10 Display RAM (HD61605)

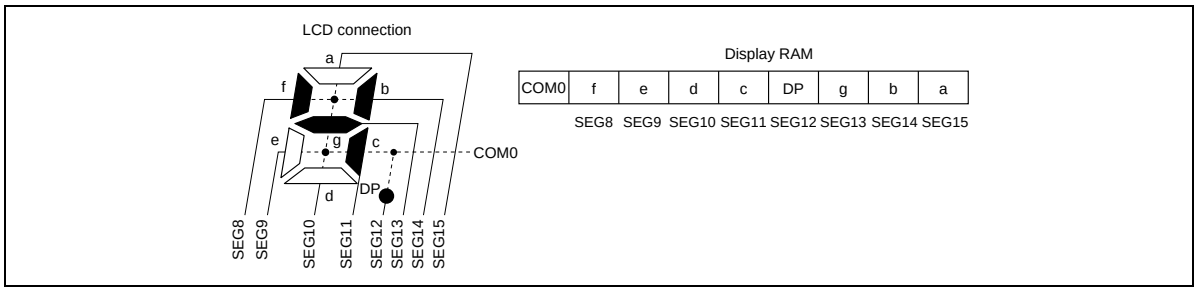


Figure 11 Example of Correspondence between LCD Connection and Display RAM (HD61605)

The 8-bit data is written on a digit basis into the digit address (displayed as Adn) shown in Figure 12. When data is transferred from a microprocessor, four 4-bit data are needed to specify the digit address and an 8-bit display data. Figure 13 shows the correspondence between each segment in an Adn and the transferred 8-bit data.

In bit manipulation, any one bit of display RAM can be written. When data is transferred on a bit basis, 1-bit display data and a segment address (6 bits) should be specified.

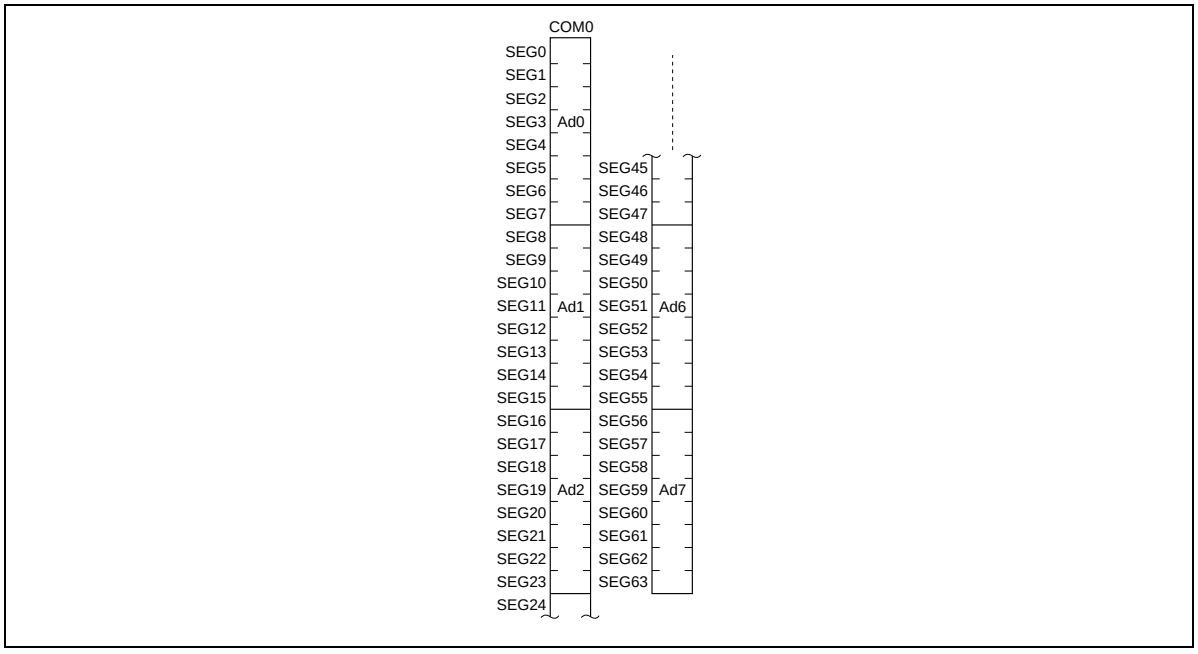


Figure 12 Allocation of Digits (HD61605)

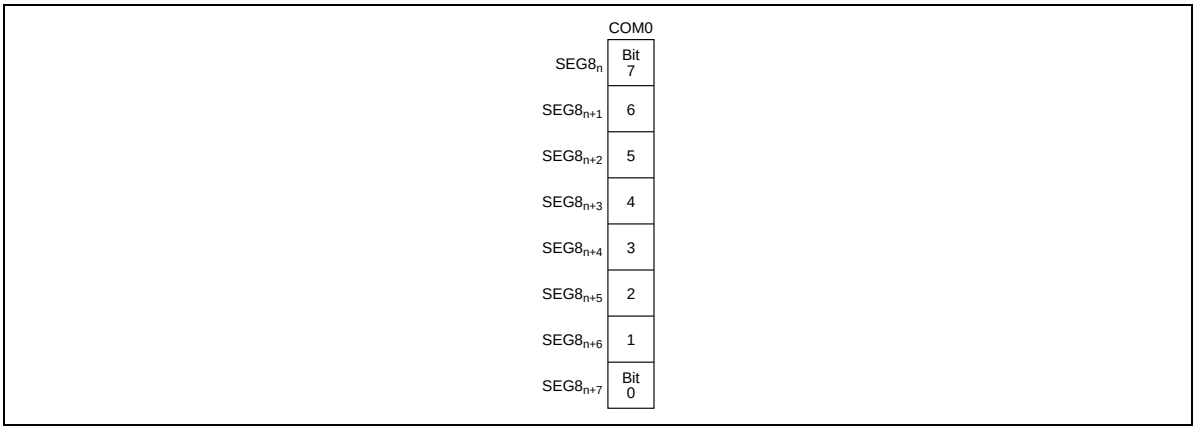


Figure 13 Bit Assignment in an Adn (HD61605)

Operating Modes

HD61604 Operating Modes

The HD61604 has the following operating modes:

1. LCD drive mode
   Determines the LCD driving method.
   a. Static drive mode
      LCD is driven statically.
   b. 1/2 duty cycle drive mode
      LCD is driven with 1/2 duty cycle and 1/2 bias.
   c. 1/3 duty cycle drive mode
      LCD is driven with 1/3 duty cycle and 1/3 bias.
   d. 1/4 duty cycle drive mode
      LCD is driven at 1/4 duty cycle and 1/4 bias.
2. Data display mode
   Determines how to write display data into the data RAM.
   a. Static display mode
      8-bit data is written into the display RAM according to the digit in static drive.
   b. 1/2 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/2 duty cycle drive.
   c. 1/3 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/3 duty cycle drive.
   d. 1/4 duty cycle display mode
      8-bit data is written into the display RAM according to the digit in 1/4 duty cycle drive.
3. READY output mode
   Determines the READY output timing.
   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:
   a. READY is always available (Figure 14).
   b. READY is made available by $\overline{CS}$ and $\overline{RE}$ (Figure 15).
4. LCD off mode
   In this mode, the HD61604 stops driving the LCD and turns it off.

The above 4 modes are specified by mode setting data. The modes are independent of each other and can be used in any combination. The bit manipulation is independent of data display mode and can be used regardless of it.

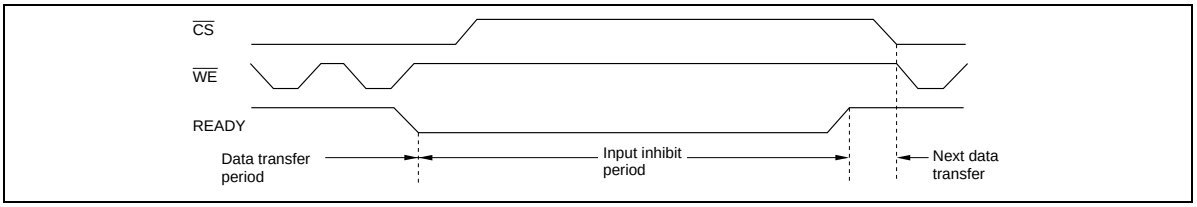


Figure 14 READY Output Timing (When It Is Always Available)

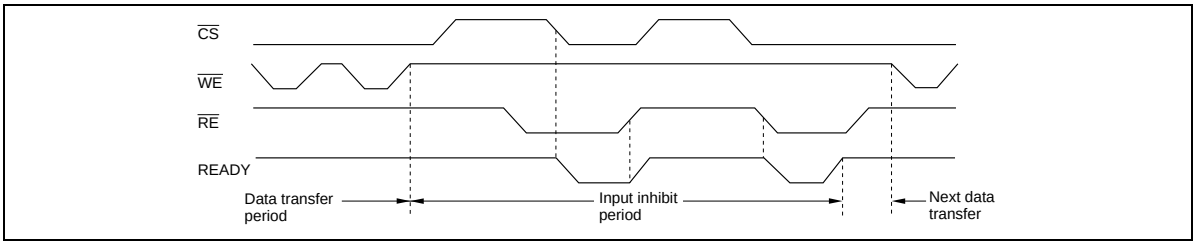


Figure 15 READY Output Timing (When It Is Made Available by $\overline{CS}$ and $\overline{RE}$)

HD61605 Operating Modes

The HD61605 has the following operating modes:

1. READY output mode
   Determines the READY output timing.
   After a data set is transferred, the data is processed internally. The next data cannot be acknowledged during the processing period. The READY output reports the period to the MPU. The timing when READY is output can be selected from the following two modes:
   a. READY is always available (Figure 16).
   b. READY is mode available by $\overline{CS}$ and $\overline{RE}$ (Figure 17).
2. LCD off mode
   In this mode, the HD61605 stops driving the LCD and turns it off.

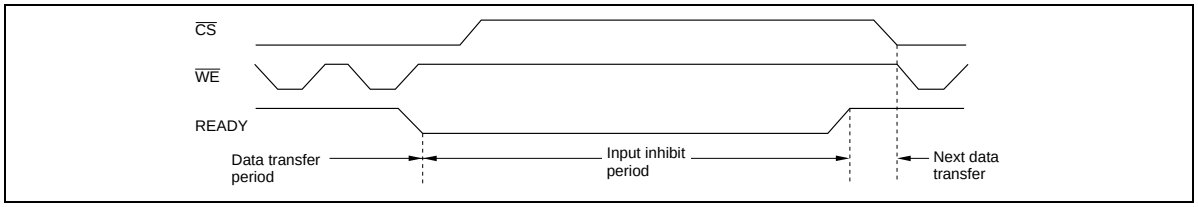


Figure 16 READY Output Timing (When It Is Always Available)

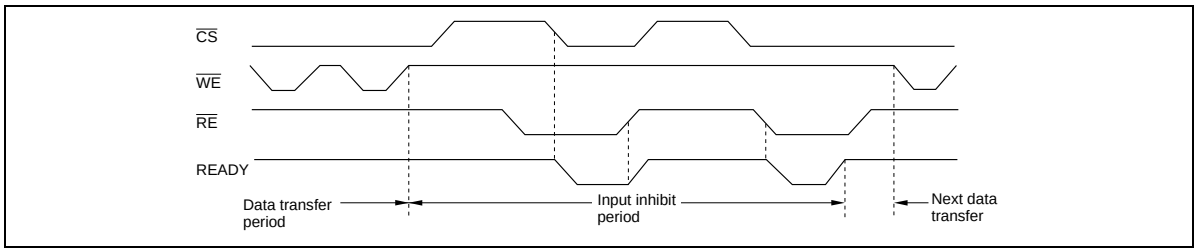


Figure 17 READY Output Timing (When It Is Made Available by $\overline{CS}$ and $\overline{RE}$)

Input Data Formats

HD61604 Input Data Formats

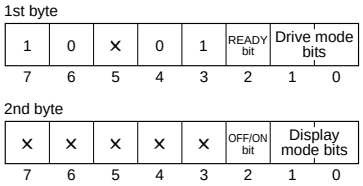
Input data is composed of 8 bits × 2 bytes. Input them as 2-byte data after READY output changes from low to high or low pulse enters into $\overline{RE}$ pin.

1. Display data
   Updates display on an 8-segment basis.

   a. Display address
      Digit address Adn in accordance with display mode
   b. Display data
      Pattern data written into the display RAM according to display mode and the address
2. Bit manipulation data
   Updates display on a segment basis.

   a. Display data
      Data written into 1 bit of the specified display RAM
   b. COM address
      Common address of display RAM
   c. SEG address
      Segment address of display RAM

3. Mode setting data



a. Display mode bits

00: Static display mode

01: 1/2 duty cycle display mode

10: 1/3 duty cycle display mode

11: 1/4 duty cycle display mode

b. OFF/ON bit

1: LCD off (set to 1 when SYNC is entered)

0: LCD on

c. Drive mode bits

00: Static drive

01: 1/2 duty cycle drive

10: 1/3 duty cycle drive

11: 1/4 duty cycle drive

d. READY bit

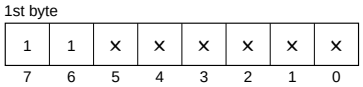
0: READY bus mode: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0 (reset to 0 when SYNC is entered)

1: READY port mode: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$

Note: Input the same data to display mode bits and drive mode bits.

4. 1-byte instruction

The first data (first byte) is ignored when the bit 6 and bit 7 in the data are 1.

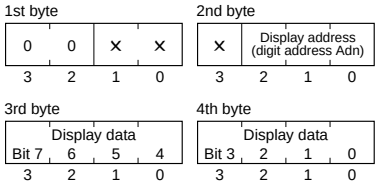


HD61605 Input Data Formats

Input data is composed of 4 bits × 4 bytes. Input them as four 4-bit data after READY output changes from low to high or low pulse is enters into $\overline{RE}$ pin.

1. Display data

   Updates display on an 8-segment basis.



   a. Display address

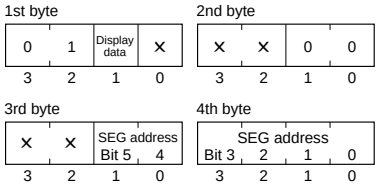
      Digit address Adn shown in Figure 12.

   b. Display data

      Pattern data written into the display RAM as shown in Figure 13.

2. Bit manipulation data

   Updates display on a segment basis.



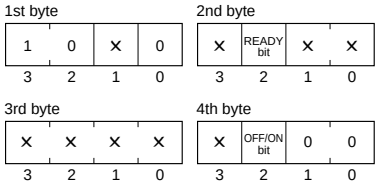
   a. Display data

      Data written into the 1 bit of the specified display RAM.

   b. SEG address

      Segment address of display RAM (segment output).

3. Mode setting data



a. OFF/ON bit

1: LCD off (set to 1 when SYNC is entered)

0: LCD on

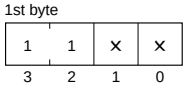
b. READY bit

0: READY bus mode: READY outputs 0 only while $\overline{CS}$ and $\overline{RE}$ are 0 (reset to 0 when SYNC is entered)

1: READY port mode: READY outputs 0 regardless of $\overline{CS}$ and $\overline{RE}$

4. 1-byte instruction

The first data (4 bits) is ignored when the bit 3 and 2 in the data are 1.



How to Input Data

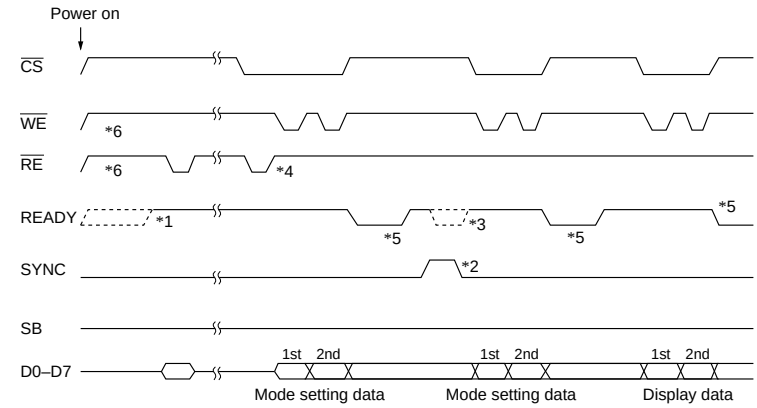
How to Input Data into HD61604

Input data is composed of 8 bits × 2 bytes. Take care that the data transfer is not interrupted, because the first 8-bit data is distinguished from the second one by the sequence only.

When data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of bytes (count of the first and second bytes):

1. Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes).
2. Input 2 or more 1-byte instruction data whose bit 7 and 6 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$, D0 to D7) is similar to that of static RAM such as HM6116. Access to the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for access, refer to the timing specifications and Figure 18.



Notes:
1. READY output is indefinite during 12 clocks after the oscillation starts at power on (clock: OSC2 clock).
2. High pulse should be applied to SYNC pin when using two or more chips simultaneously.
3. In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
4. Reset the byte counter after power on.
5. READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
6. Connect a pull-up resistor if $\overline{WE}$ or $\overline{RE}$ may be floating.
7. It is not always necessary to follow this example.

Figure 18 Example of Data Transfer Sequence

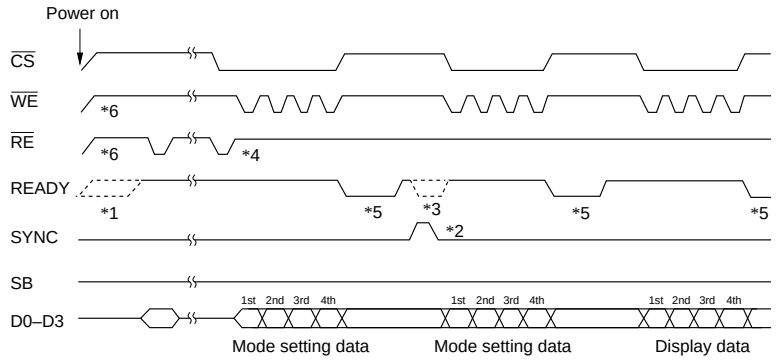
How to Input Data into HD61605

Input data is composed of 4 bits × 4 bytes. Take care that the data transfer is not interrupted because the first 4-bit data to the fourth 4-bit data are distinguished from each other by the sequence only.

When data transfer is interrupted, or at power on, the following two methods can be used to reset the count of the number of data (count of the first 4-bit data to the fourth 4-bit data):

1. Set $\overline{CS}$ and $\overline{RE}$ to low (no display data changes).
2. Input 4 or more 1-byte instruction data (4-bit data) whose bit 3 and 2 are high (display data may change).

The data input method via data input pins ($\overline{CS}$, $\overline{WE}$, D0 to D3) is similar to that of static RAM such as HM6116. Access to the LSI can be made through the same bus line as ROM and RAM. When output ports of a microprocessor are used for access, refer to the timing specifications and Figure 19.



Notes:
1. READY output is indefinite during 12 clocks after the oscillation starts at power on (clock: OSC2 clock).
2. High pulse should be applied to SYNC pin when using two or more chips simultaneously.
3. In the mode in which READY is always available, READY output is indefinite while high is being applied to SYNC.
4. Reset the 4-bit data counter after power on.
5. READY output period is within 3.5 clocks in the mode setting operation and bit manipulation or within 10.5 clocks when the display data (8 bits) is updated.
6. Connect a pull-up resistor if $\overline{WE}$ or $\overline{RE}$ is floating.
7. It is not always necessary to follow this example.

Figure 19 Example of Data Transfer Sequence

Notes on READY Output

Note that the READY output will be unsettled during 1.5 clocks (max) after inputting the first 2-byte data for setting the mode after turning the power on. This is because the READY bit data of mode setting latches and the mode of READY pin (READY bus or port mode) are unsettled until the completion of mode setting.

There are two kinds of the READY output waveforms depending of the modes.

1. READY bus mode (READY bit = 0)
2. READY port mode (READY bit = 1)

However, if you input SYNC before mode setting, waveform will be determined; when you choose READY bus mode, (1) a in Figure 20 will be output, and when you choose READY port mode, (2) a will be output. The figures can be applied both to HD61604 and HD61605.

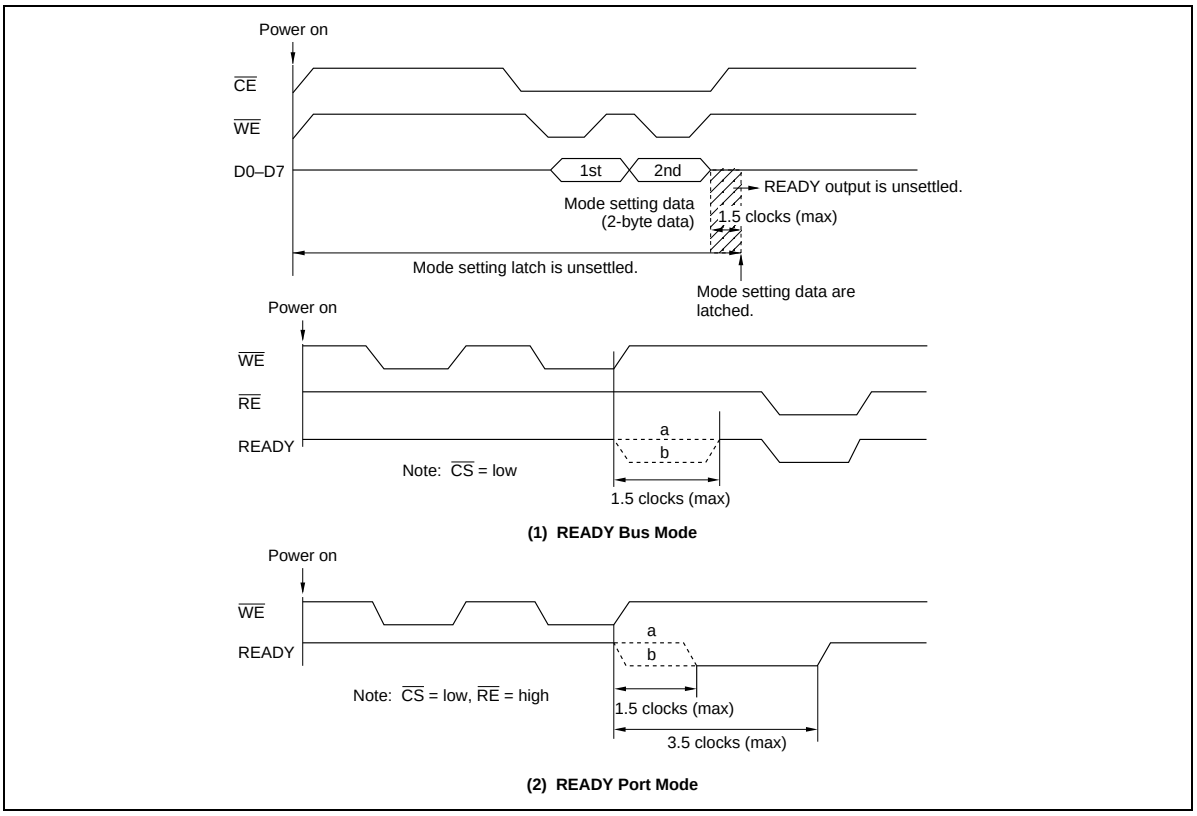


Figure 20 READY Output According to Modes

Standby Operation

Standby operation with low power consumption can be activated when pin SB is used. Normal operation of the LSI is activated when pin SB is low level, and the LSI goes into the standby state when pin SB is high level. The standby state of the LSI is as follows:

1. LCD driver is stopped (LCD is off).
2. Display data and operating mode are held.
3. The operation is suspended while display changes (while READY is outputting low). In this case, READY outputs high within 10.5 clocks or 3.5 clocks after release from the standby mode.
4. Oscillation is stopped.

When this mode is not used, connect pin SB to VSS.

Multichip Operation

When an LCD is driven with two or more chips, the driving timing of the LCD must be synchronized. In this case, the chips are synchronized with each other by using SYNC input. If SYNC input is high, the LCD driver timing circuit is reset. Apply high pulse to the SYNC input after the operating mode is set.

A high pulse to the SYNC input changes the mode setting data. (The OFF/ON bit is set and the READY bit is reset. See (3) Mode Setting Data in “Input Data Formats.”) Transfer the mode setting data into the LSI after every SYNC operation.

If a power on reset signal is applied to the SYNC pin, the LCD can be off-state when the power is turned on.

When SYNC input is not used, connect pin SYNC to VSS.

When SB input is used, after standby mode is released, high pulse must be applied to the SYNC input, and mode setting data must be set again.

Restriction on Usage

Minimize the noise by inserting a noise bypass capacitor (≥ 1 µF) between VDD and VSS pins. (Insert one as near chip as possible.)

Liquid Crystal Display Drive Voltage Circuit (HD61604)

What is LCD Voltage?

HD61604 drives liquid crystal display using four levels of voltages (Figure 21); VDD, V1, V2, and V3 (VDD is the highest and V3 is the lowest). The voltage between VDD and V3 is called VLCD and it is necessary to apply the appropriate VLCD according to the liquid crystal display. V3 always needs to be supplied regardless of the display duty ratio since it supplies the voltage to the LCD drive circuit of HD61604.

Connecting R2–R5 in series between VDD and VSS (Figure 22) generates ÆV or VLCD by using the resistance ratio to supply these voltage to pins V1, V2, V3, C2–C4 are the smoothing capacitors. Connect a trimmer potentiometer for R5 and change its resistance value to control the contrast.

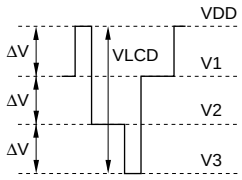
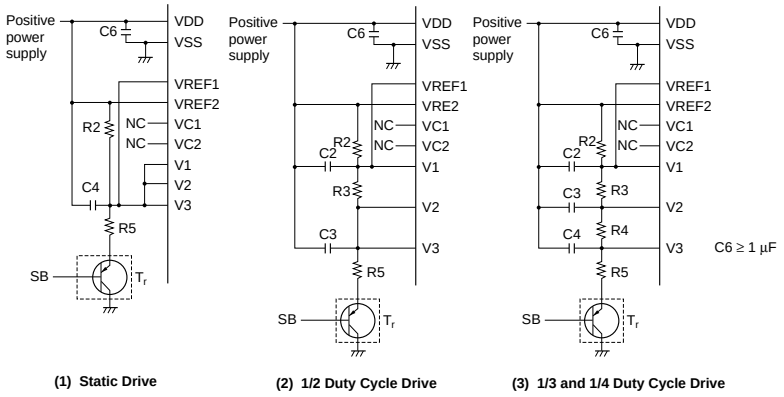


Figure 21 LCD Output Waveform and Output Levels (1/3 Duty Cycle, 1/3 Bias)



Notes: 1. When standby mode is used, a transistor is required.
2. R2–R5 should be some kΩ–some tens of kΩ, and C2–C4 should be 0.1 µF–0.3 µF.

Figure 22 Example when External Drive Voltage Is Used

Liquid Crystal Display Drive Voltage (HD61605)

As shown in Figure 23, apply LCD drive voltage from the external power supply.

Oscillation Circuit

When Internal Oscillation Circuit Is Used

When the internal oscillation circuit is used, attach an external resistor R_{OSC} as shown in Figure 24. (Insert R_{OSC} as near chip as possible, and make the OSC1 side shorter.)

When External Clock Is Used

When an external clock of 100 kHz with CMOS level is provided, pin OSC1 can be used for the input pin. In this case, open pin OSC2.

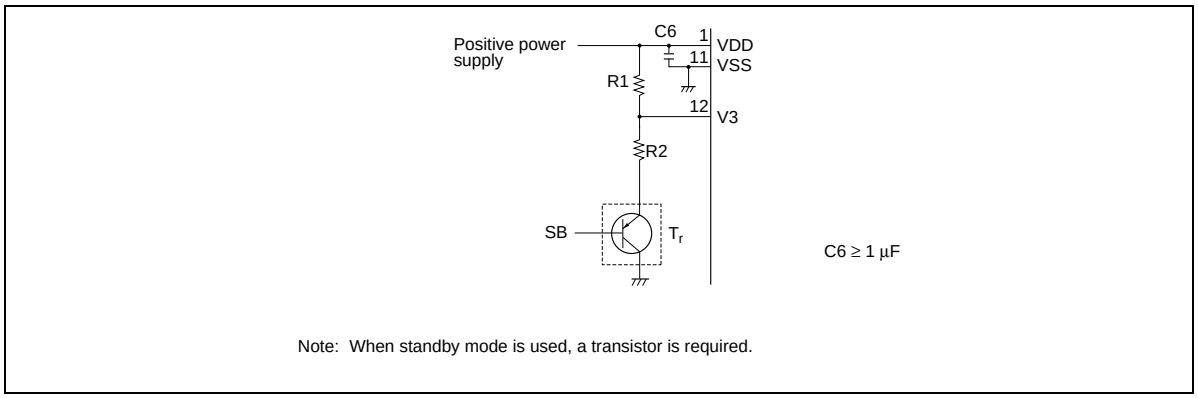


Figure 23 Example of Drive Voltage Generator

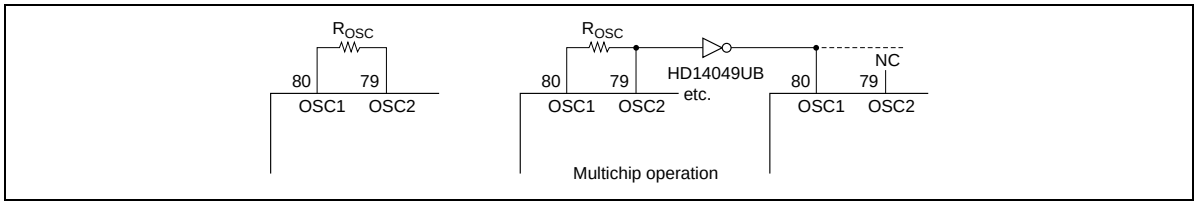


Figure 24 Example of Oscillation Circuit

Applications

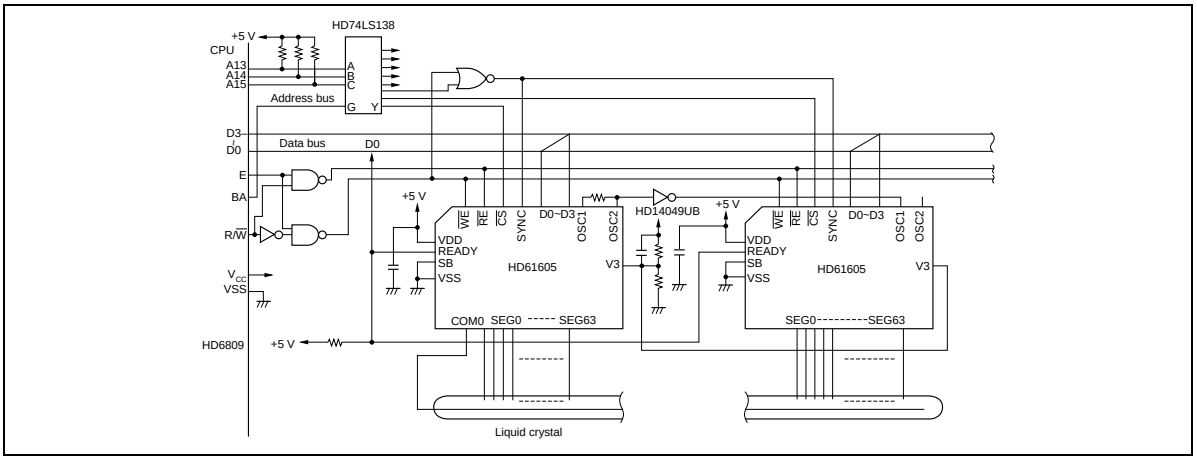


Figure 25 Example (1)

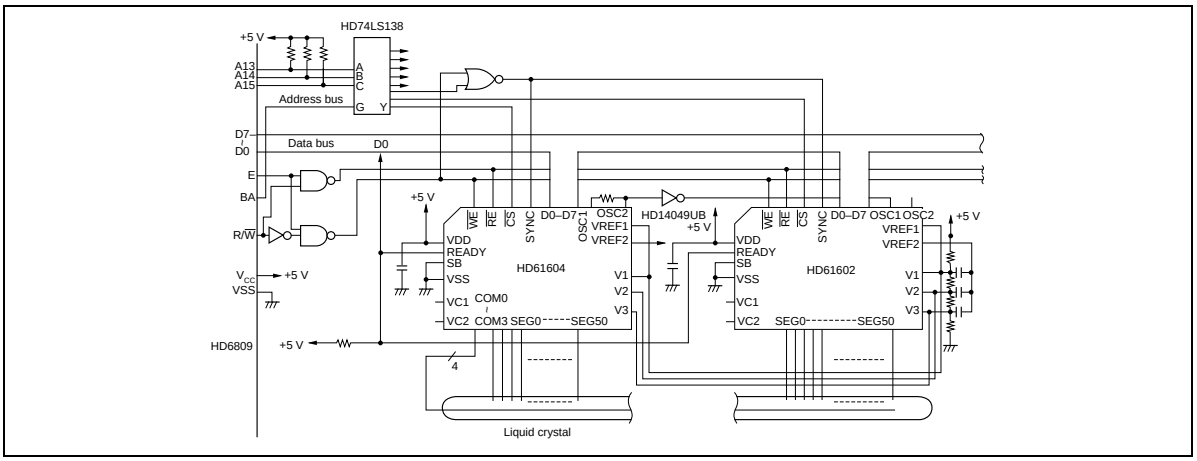


Figure 26 Example (2)

Absolute Maximum Ratings

Item	Symbol	Limit	Unit
Power supply voltage*	VDD, V1, V2, V3	–0.3 to +7.0	V
Pin voltage*	VT	–0.3 to VDD + 0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

* Value referenced to VSS = 0 V.

Note: If LSIs are used above absolute maximum ratings, they may be permanently destroyed. Using them within electrical characteristics limits is strongly recommended for normal operation. Use beyond these conditions will cause malfunction and poor reliability.

Recommended Operating Conditions

		Limit			
Item	Symbol	Min	Typ	Max	Unit
Power supply voltage*	VDD	4.5	—	5.5	V
	V1, V2, V3	0	—	VDD	V
Pin voltage*	VT	0	—	VDD	V
Operating temperature	T_{opr}	–20	—	+75	°C

* Value referenced to VSS = 0 V.

Electrical Characteristics

DC Characteristics (VSS = 0 V, VDD = 4.5 V to 5.5 V, Ta = –20°C to +75°C, unless otherwise noted)

Item		Symbol	Limit Min	Typ	Max	Unit	Test Condition
Input high voltage	OSC1	VIH1	0.8 VDD	—	VDD	V	
	Others	VIH2	2.0	—	VDD	V	
Input low voltage	OSC1	VIL1	0	—	0.2 VDD	V	
	Others	VIL2	0	—	0.8	V	
Output leakage current	READY	I_{OH}	—	—	5	µA	Pull up the pin to VDD
Output low voltage	READY	VOL	—	—	0.4	V	I_{OL} = 0.4 mA
Input leakage current*[1]	Input pin	I_{IL1}	–1.0	—	1.0	µA	VIN = 0 to VDD
	V1	I_{IL2}	–20	—	20	µA	VIN = VDD to V3
	V2, V3	I_{IL3}	–5.0	—	5.0	µA	
LCD driver voltage drop	COM0–COM3	Vd1	—	—	0.3	V	±Id = 3 µA for each COM, V3 = VDD – 3 V
	SEG0–SEG50	Vd2	—	—	0.6	V	±Id = 3 µA for each SEG, V3 = VDD – 3 V
Current consumption*[2]		I_{DD}	—	—	100	µA	During display* R_{OSC} = 360 kΩ
		I_{DD}	—	—	5	µA	At standby

* Except the transfer operation of display data and bit data.

Notes: 1. V1, V2: applied only to HD61604.

2. Do not connect any wire to the output pins and connect the input pins to VDD or VSS.

AC Characteristics (VSS = 0 V, VDD = 4.5 V to 5.5 V, Ta = –20°C to +75°C, unless otherwise noted)

Item		Symbol	Limit			Unit	Test Condition
			Min	Typ	Max		
Oscillation frequency	OSC2	f_{osc}	70	100	130	kHz	R_{osc} = 360 kΩ
External clock frequency	OSC1	f_{osc}	70	100	130	kHz	
External clock duty	OSC1	Duty	40	50	60	%	
I/O signal timing		t_S	400	—	—	ns	
		t_H	10	—	—	ns	
		t_{WH}	300	—	—	ns	
		t_{WL}	400	—	—	ns	
		t_{WR}	400	—	—	ns	
		t_{DL}	—	—	1.0	µs	Figure 31
		t_{EN}	400	—	—	ns	
		t_{OP1}	9.5	—	10.5	Clock	For display data transfer
		t_{OP2}	2.5	—	3.5	Clock	For bit and mode data transfer
Input signal rise time and fall time		t_r, t_f	—	—	25	ns	

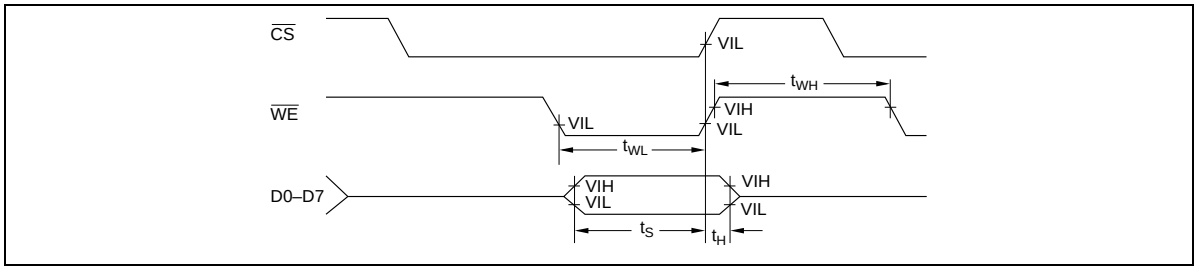


Figure 27 Write Timing ($\overline{RE}$ Is Fixed High and SYNC Low)

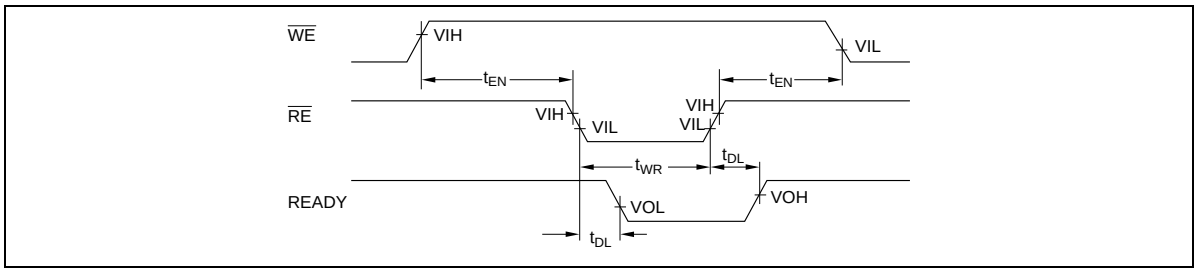


Figure 28 Reset/Read Timing ($\overline{CS}$ and SYNC Are Fixed Low)

Figure 29 READY Timing (When the READY Output Is Always Available)

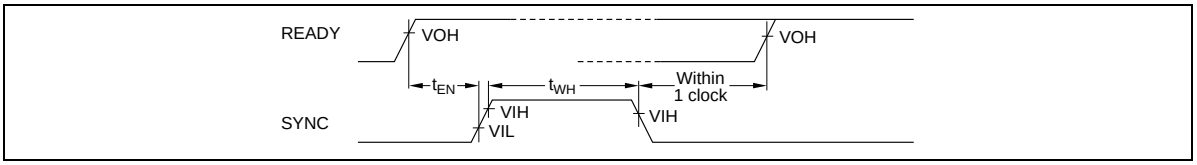


Figure 30 SYNC Timing

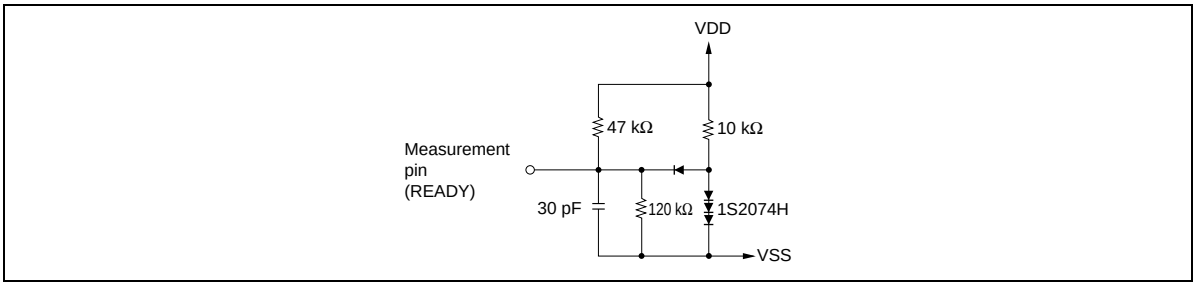


Figure 31 Bus Timing Load Circuit (LS-TTL Load)