Helium 100 Communications Processor

Virata
Product Profile

July 2001

KEY FEATURES

- **ATM switching and layer 2/3 processing device**
- **USB interfaces for external modem applications**
- **Utopia—1/2 and ADSL T1.413 interfaces**
- **Ethernet—10baseT interface**
- **Dual ARM RISC processor architecture**

Product Applications

- DSL modem
- DSL gateway
- Cable modem
- ATM line cards
- ATM access
- ATM SCU/DSU
- Bridging and routing

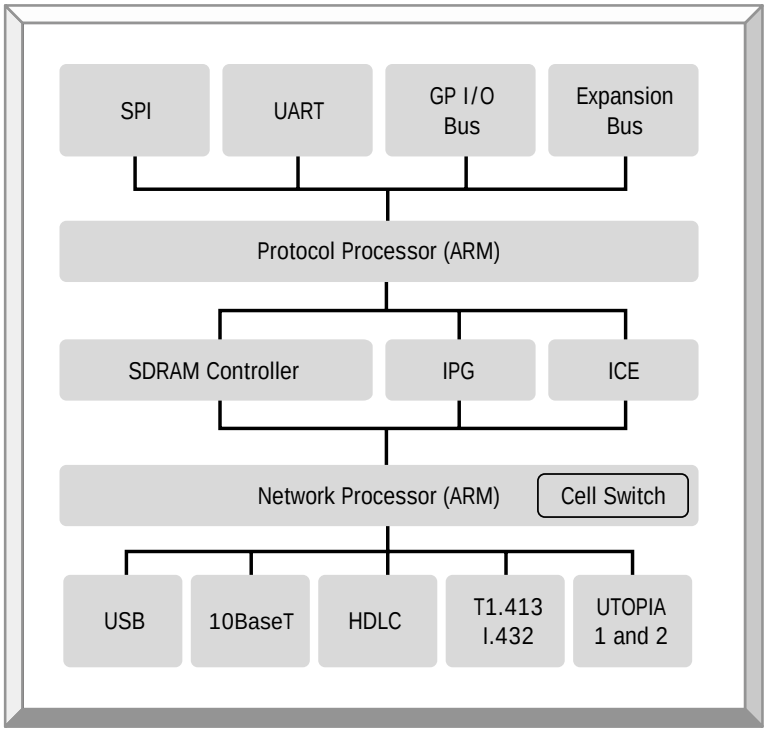
Description

Helium 100 is a single chip, highly integrated ATM switching and layer 2/3 processing device. A general purpose RISC Protocol Processor runs higher layer protocols while a high performance microcoded RISC Network Processor is used for cell and frame handling switching at up to 75 Mbps.

Integrating many common interface functions, Helium 100 is designed for flexible, low cost, high functionality, high performance products. It may be used in gateway, ATM access device, or USB modem customer premises equipment (CPE) or central office (CO).

Helium 100 contains a Network Processor that controls the direct connections to Ethernet and USB, as well as physical interfaces for Utopia 1 and 2, HDLC and I.432.

The Network Processor has 16K of microcode RAM and a high-speed interface to external SDRAM. This supports both ATM cells and packets, OAM cell handling, policing, shaping and accounting.



Helium 100 System Interfaces

The two processors communicate via the inter-processor gateway (IPG).

Helium 100 extends Virata's ATOM architecture and runs the complete suite of ATMOS™ software, including support for routing, bridging, signaling, and SNMP Management.

Software flexibility, high integration, and built-in hardware debugging (ICE) support allow rapid product development.

This combination of hardware and software, and Integrated Software on Silicon (ISOS™) provides a unique time-to-market advantage.

Reference Platform

The BD6100 is the development reference platform for Helium 100, providing a wealth of hardware and software debug tools to assist partners in rapid development and deployment of their products. Training, documentation, and support are also available.

Specifications

Processors

- Protocol Processor (PP) is a 48 MHz ARM7TDMI RISC core, which includes an 8K cache providing:
  - Modem PHY Management (depending on application)
  - Initialization code
  - Soft real-time tasks
- Network Processor (NP) is a 48 MHz ARM7TDMI RISC core with 16K of SRAM performing:
  - Data Transfer
    Framing
    Interleaving
    CRC Generation
    Switching
  - Hard real-time tasks

USB

USB 1.1 slave interface — up to 12 Mbps using Control, Interrupt, Bulk, and Isochronous endpoints and transfers.

10BaseT Ethernet

Helium 100 contains a 10baseT Ethernet MAC with a low power integrated PHY.

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Product Profile

Interfaces

- USB
- 10baseT Ethernet
- Utopia 1/2
- HDLC/T1.413
- GPIOs
- Expansion bus
- UART
- SDRAM
- Flash PROM
- EEPROM

Utopia

Utopia 1 and 2 (master/slave) interfaces with 31 ports, configuration:

- 8 ports dual-latency, or
- 2 ports dual-latency and 29 ports single latency
- 2 ports dual-latency and 12 ports single latency

ADSL

ADSL full duplex data interface to external ADSL PHY implementing all the framing requirements I.432 of T1.413.

HDLC

The HDLC interface, using the same pins as ADSL, conforms to Q.921 at a frame rate of 25MHz with a 16-bit CRC generation.

GPIO

The General Purpose I/O bus contains 13 pins. Of these pins, two are used for the UART serial interface (Tx and Rx at a speed of 38,462 baud) and three for the serial boot EEPROM (data in, data out, and clock). Five pins can also be configured as Ethernet status indicators.

SDRAM

SDRAM interface conforms to JEDEC requirements, supporting address space from 2 to 32 Mbytes with a selectable 16- or 32-bit wide data bus.

Expansion Bus

Configurable as 8- or 16-bit peripheral bus, which can support 8-bit Motorola, 16-bit Intel or 16-bit multiplexed modes. Mainly used to control external devices and boot Helium 100 from memory, ROM or Flash PROM. Up to 4 devices supported using 4 pins as programmable chip selects or more with additional decoder.

Boot Options

- USB interface
- UART
- Ethernet Network Boot
- Serial EEPROM
- Flash PROM

Software

Helium 100's Protocol Processor runs Virata's extensive networking software suite. See separate datasheet for full details:

- OS Kernel and C/C++ Library (either ATMOS or VxWorks)
- Non-zero VPI support
- OAM I.610 full implementation
- SNMP v1, v2, and v3
- Flash-FS and In Store-FS
- USB drivers for Windows® 98, ME and 2000
- QOS: UBR, CBR, nrt-VBR , rt-VBR
- ATM Forum UNI 3.0, 3.1 and 4.0 Signaling
- ILMI 4.0
- SSCOP and AAL-2 CPCS
- Bridge-mode RFC1483 PVC and SVC
- PPP over ATM PVC (RFC 2364)
- Classical IP - RFC1577, RFC1483, RFC1755
- Classical IP ARP server
- MAC-layer Bridge (Spanning Tree 802.1d)
- ATM Forum LEC
- TCP/IP Stack
- IP Router - RIP1, RIP2
- TFTP Client and Server
- PPTP and L2TP
- DHCP Client, Server, and Relay
- NAT with extensive ALG
- DNS Relay and Client
- PPPoE Client and Relay Agent
- FRF.12 Frame Relay fragmentation
- LMI for Frame Relay PVC link management

Package

225 ball PBGA

Environmental

Core Supply 1.8V,. +/- 10%
I/O Supply 3.3V, +/- 10%
Commercial temperature range of
0 to +70 degrees Centigrade

Ordering Information

VC4220-PBC, Helium 100 IC
BD6100, Helium 100 Development Board
Data book available on request
DO-008532-PS

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