General Features

- 0.8μm single poly, double metal CMOS technology
- Sea of gate architecture
- Operating voltage: 5V
- Propagation delay 0.3ns for 2-input NAND with fanout=2
- Output driving capability
  - 2mA, 4mA, 8mA, 12mA, 16mA, 20mA, 24mA, 30mA, 48mA
- 2 array bases
- Under 5K usable gates
- Maximum I/O 28, 48 (not including power pads)

HT5D Series

Part Number	Usable Gates	Maximum I/O
HT5D028	672	28
HT5D048	1285	48

Cell Libraries

- Buffers
  - Inverting, noninverting, tri-state, clock buffer
- Input buffers
  - CMOS, CMOS Schmitt
  - TTL, TTL Schmitt
- NAND/AND gates
- NOR/OR gates
- AOI/OAI gates
- XNOR/XOR gates
- D Flip-Flops
- T Flip-Flops
- Multiplexed Flip-Flops
- JK Flip-Flops
- Latches
  - with set, with clear, with set and clear, NOR-latch, NAND-latch, scannable latch
- Adders
  - 1-bit full, 2-bit full
- Adders/Subtractors
  - 1-bit, 2-bit
- Decoders
  - 2-to-4, 3-to-8
- Multiplexers
  - 2-to-1, 4-to-1, 8-to-1
- Synchronous counters
  - with clear, with clear and set
- Miscellaneous
  - DLY, CLOAD1, MAXCAP, NETWTH, RP01D1, WEIGHT

I/O Pad Libraries

- Input pads
  - Input only, with pull-up/pull-down resistor
- Clock input pads
  - Inverting/noninverting with CMOS level
  - Inverting/noninverting with Schmitt Trigger
  - Inverting/noninverting with TTL level
- Output pads
  - 2mA, 4mA, 8mA, 12mA, 16mA, 20mA, 24mA, 30mA, 48mA driving capability
  - Output only, 3-state output, with pull-up/pull-down resistor
  - CMOS level, TTL level
  - with limited slew rate control
- I/O Pads
  - 2mA, 4mA, 8mA, 12mA, 16mA, 20mA, 24mA, 30mA, 48mA driving capability
  - 3-state output, with pull-up/pull-down resistor
  - CMOS level, TTL level
  - with limited slew rate control
- Power pads
  - Core only, padding only, c ore and padding
- Crystal oscillator pads
  - Low frequency (1kHz~10MHz)
  - Intermediate frequency (10MHz~25MHz)
  - High frequency (25MHz~60MHz)

General Features

- 0.5μm single poly double/triple metal CMOS technology
- Sea of gate architecture
- Operating voltage: 5V/3V
- Propagation delay 120ps of 2-input NAND with fanout=2
- Output driving capability
  - 4mA, 8mA, 12mA, 16mA, 24mA
- Maximum 66K usable gates
- Maximum I/O: 208
- Megacells and metallized SRAM ROM blocks are available for integration
- Supports scan test ability
- 8 Array Bases

HT5F/5G Series

Part Number	Max. I/O	Usable Gates (40% DM)	Usable Gates (80% TM)
HT5F068	68	7198	—
HT5F084	84	11096	—
HT5F100	100	15444	—
HT5F128	128	25216	—
HT5F164	164	41172	—
HT5F208	208	66008	—
HT5G100	100	—	30888
HT5G128	128	—	50433

Cell Library

- Buffers
  - Inverting, noninverting, tri-state, clock buffer
- NAND/AND gates
- NOR/OR gates
- AOI/OAI gates
- XNOR/XOR gates
- Delay cells
  - 2ns, 4ns, 7ns, 10ns
- Parity generator
  - 8 bits even, 8 bits odd
- Flip-flops
  - D-type, T-type, JK-type
- Multiplexed flip-flops
- Latches
  - with set, with clear, with set and clear, Nor-Latch
  - NAND-latch, scannable latch
- Adders
  - 1-bit Half, 1-bit Full
- Decoders
  - 2-to-4, 3-to-8
- Multiplexers
  - 2-to-1, 3-to-1, 4-to-1, 5-to-1, 8-to-1
- Comparator
- Miscellaneous
  - Internal pull-up/pull-down, bus holder, RAM cell

5V I/O Pad Library

- Input pads
  - Inverting, noninverting
  - CMOS, TTL
  - Clock driver with CMOS buffer
  - Clock driver with TTL buffer
- Output pads
  - 2mA, 4mA, 8mA, 12mA, 16mA, 24mA driving capability
  - Output only, 3-state output, with pull-up/pull-down resistor
  - CMOS level, TTL level
  - with limited slew rate control
- Bidirectional pads
  - 2mA, 4mA, 8mA, 12mA, 16mA, 24mA driving capability
  - 3-state output, with pull-up/pull-down resistor
  - CMOS level, TTL level
  - with limited slew rate control

3.3V I/O Pad Library

- Input pads
  - Inverting, noninverting
  - CMOS, TTL
  - Clock driver with CMOS buffer
  - Clock driver with TTL buffer
- Output pads
  - 2mA, 4mA, 8mA, 12mA, 16mA, 24mA driving capability
  - Output only, 3-state output, with pull-up/pull-down resistor
  - CMOS level, TTL level
  - with limited slew rate control
- Bidirectional pads
  - 2mA, 4mA, 8mA, 12mA, 16mA, 24mA driving capability
  - 3-state output, with pull-up/pull-down resistor
  - CMOS level, TTL level
  - with limited slew rate control