TOMATO LSI Inc.

HT0324A

(5.0V SPECIFICATION)

65COM / 132SEG DRIVER & CONTROLLER FOR STN LCD

August. 2000

VER 0.0

TOMATO LSI Inc.

HT0324A Specification revision history		
Version	Content	Date
0.0	1. Operating voltage range : VDD = 2.4V ~ 5.5V	August. 2000

CONTENTS

1. INTRODUCTION

The HT0324A is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It contains 65 common and 132 segment driver circuits. This chip is connected directly to a microprocessor (MPU), accepts serial or 8-bit parallel display data and stores in an on-chip Display Data RAM (DDRAM) of 65 x 132 bits. It provides a high-flexible display section due to one to one correspondences between on-chip DDRAM bits and LCD panel pixels. And it performs DDRAM read / write operation with no externally operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

2. FEATURES

Driver output circuits

-. 65 common outputs / 132 segment outputs

On-chip display data RAM (DDRAM)

-. Capacity: 65 x 132=8,580 bits
-. RAM bit data “1”: a dot of display is illuminated.
-. RAM bit data “0”: a dot of display is not illuminated.

Multi-chip operation

-. Master and slave mode available

Applicable duty-ratios

Duty ratio	Applicable LCD bias	Maximum display area
1/65	1/9 or 1/7	65 x 132
1/55	1/8 or 1/6	55 x 132
1/49	1/8 or 1/6	49 x 132
1/33	1/6 or 1/5	33 x 132

Microprocessor (MPU) interface

-. High-speed 8-bit parallel bi-directional interface with 6800-series or 8080-series
-. Serial inter-face (only write operation) available

Various Function set

-. Display ON/OFF, set initial display line, set page address, set column address, read status, write / read display data, select segment driver output, reverse display ON/OFF, entire display ON/OFF, select LCD bias, set/reset modify-read, select common driver output, control display power circuit, select internal regulator resistor ratio for V0 voltage regulation, electronic volume, set static indicator state.
-. H/W and S/W reset available
-. Static drive circuit equipped internally for indicators with 4 flashing modes

Built-in analog circuits

-. On-chip Oscillator circuit for display clock(external clock can also be used)
-. High performance voltage converter
(with booster ratios of x2, x3, x4 and x5, where the step-up reference voltage can be used externally)
-. High accuracy voltage regulator(temperature coefficient: -0.05%/ or external input)
-. Electronic contrast control function (64 steps)
-. Vref = 2.1V ± 3% (V0 voltage adjustment voltage)
-. High performance voltage follower
(V1 to V4 voltage divider resistors and OP-Amp for increasing drive capacity)

Operating voltage range

-. Supply voltage (VDD): 2.4 to 5.5V
-. LCD driving voltage (VLCD = V0 -VSS): 4.5 to 15.0V

Low power consumption

-. Operating power : 40μA Typ, (VDD = 3V, x4 boosting[VCI is VDD], V0=11V, internal power supply ON, display OFF and normal mode is selected)
-. Standby power : 10μA Max. (during power save[standby] mode)

Operating Temperatures

-. Wide range of operating temperatures : -40 to 85

CMOS Process

Package type

-. Gold bumped chip and TCP available

3. BLOCK DIAGRAM

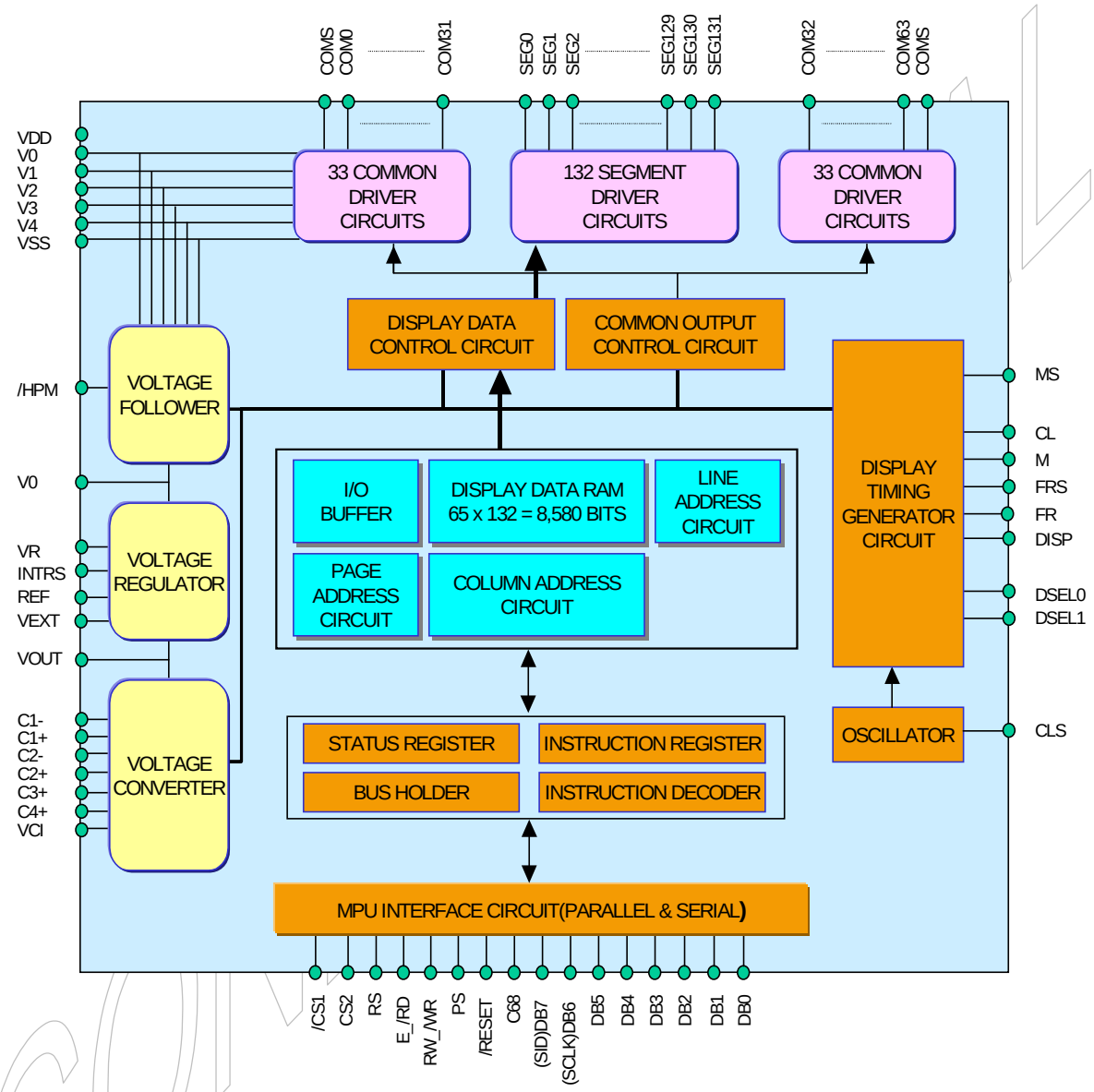

Figure 3-1. block diagra

4. PAD CONFIGURATION

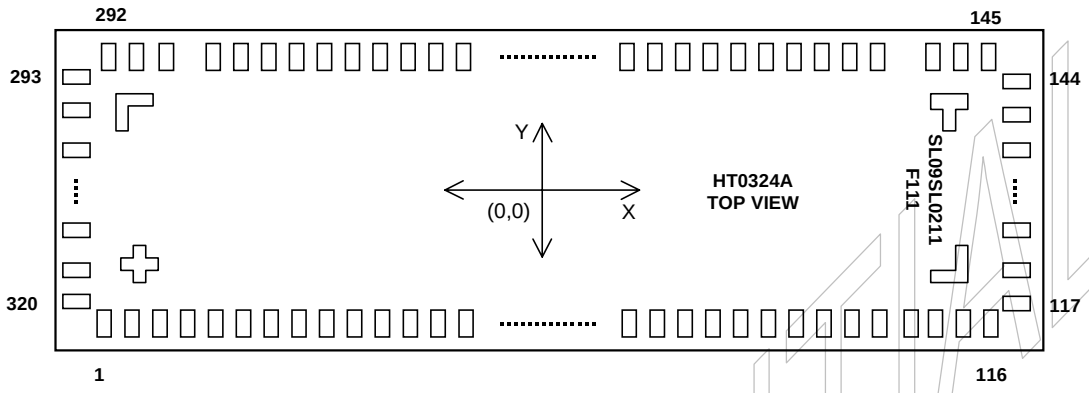

Figure 4-1. Chip configuration

Table 4-1. Pad dimensions

ITEM	Pad No.	Size		Unit
		X	Y	
Chip size (Include scribe lane)	-	9540	2310	μm
Pad pitch	2~93, 95~115	70		
	118~143, 146~291, 294~319	60		
	1~2, 93~95, 115~116, 117~118 , 143~144, 145~146, 291~292, 293~294, 319~320	80		
Bumped pad size (Bottom)	2~93, 95~115	50	102	
	118~143, 294~319	102	40	
	146~291	40	102	
	1, 94, 116, 145, 292	55	102	
	117, 144, 293, 320	102	55	
Bumped pad height	All pad	18 ±3 (Typ.)		

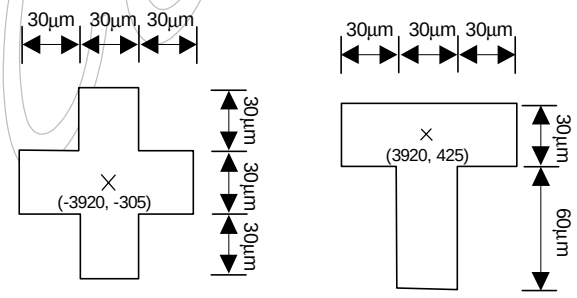

Figure 4-2. COG align key

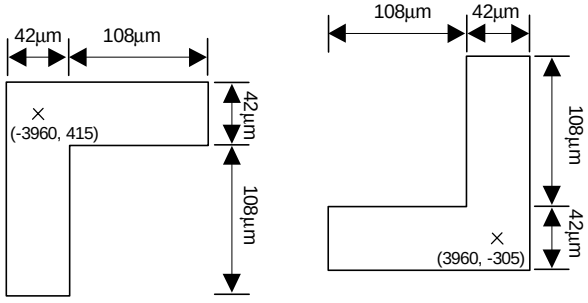

Figure 4-3. ILB align key

4-1. PAD CENTER COORDINATES

Table 4-2. Pad center coordinates [**Unit: um**]

PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y	PAD No.	PAD name	X	Y
1	DUMMY	-4045	-991	51	C4+	-535	-991	101	TEST6	2985	-991
2	FRS	-3965	-991	52	C3+	-465	-991	102	TEST7	3055	-991
3	FR	-3895	-991	53	C3+	-395	-991	103	TEST8	3125	-991
4	NC0	-3825	-991	54	C1-	-325	-991	104	TEST9	3195	-991
5	NC1	-3755	-991	55	C1-	-255	-991	105	TEST10	3265	-991
6	M	-3685	-991	56	C1+	-185	-991	106	TEST11	3335	-991
7	CL	-3615	-991	57	C1+	-115	-991	107	TEST12	3405	-991
8	DISP	-3545	-991	58	C2+	-45	-991	108	TEST13	3475	-991
9	VSS	-3475	-991	59	C2+	25	-991	109	TEST14	3545	-991
10	VSS	-3405	-991	60	C2-	95	-991	110	TEST15	3615	-991
11	/CS1	-3335	-991	61	C2-	165	-991	111	TEST16	3685	-991
12	CS2	-3265	-991	62	VDD	235	-991	112	TEST17	3755	-991
13	VDD	-3195	-991	63	VEXT	305	-991	113	TEST18	3825	-991
14	/RESET	-3125	-991	64	VEXT	375	-991	114	TEST19	3895	-991
15	RS	-3055	-991	65	REF	445	-991	115	TEST20	3965	-991
16	VSS	-2985	-991	66	VSS	515	-991	116	DUMMY	4045	-991
17	RW _/WR	-2915	-991	67	V1	585	-991	117	DUMMY	4606	-860
18	E_/RD	-2845	-991	68	V1	655	-991	118	COM31	4606	-780
19	VDD	-2775	-991	69	V2	725	-991	119	COM30	4606	-720
20	DB0	-2705	-991	70	V2	795	-991	120	COM29	4606	-660
21	DB1	-2635	-991	71	V3	865	-991	121	COM28	4606	-600
22	DB2	-2565	-991	72	V3	935	-991	122	COM27	4606	-540
23	DB3	-2495	-991	73	V4	1005	-991	123	COM26	4606	-480
24	DB4	-2425	-991	74	V4	1075	-991	124	COM25	4606	-420
25	DB5	-2355	-991	75	V0	1145	-991	125	COM24	4606	-360
26	DB6	-2285	-991	76	V0	1215	-991	126	COM23	4606	-300
27	DB7	-2215	-991	77	V0	1285	-991	127	COM22	4606	-240
28	VSS	-2145	-991	78	VR	1355	-991	128	COM21	4606	-180
29	VDD	-2075	-991	79	VR	1425	-991	129	COM20	4606	-120
30	DSEL0	-2005	-991	80	VR	1495	-991	130	COM19	4606	-60
31	DSEL1	-1935	-991	81	VSS	1565	-991	131	COM18	4606	0
32	VSS	-1865	-991	82	VSS	1635	-991	132	COM17	4606	60
33	VDD	-1795	-991	83	VDD	1705	-991	133	COM16	4606	120
34	VDD	-1725	-991	84	MS	1775	-991	134	COM15	4606	180
35	VDD	-1655	-991	85	CLS	1845	-991	135	COM14	4606	240
36	VDD	-1585	-991	86	VSS	1915	-991	136	COM13	4606	300
37	VDD	-1515	-991	87	C68	1985	-991	137	COM12	4606	360
38	VCI	-1445	-991	88	PS	2055	-991	138	COM11	4606	420
39	VCI	-1375	-991	89	VDD	2125	-991	139	COM10	4606	480
40	VCI	-1305	-991	90	/HPM	2195	-991	140	COM9	4606	540
41	VSS	-1235	-991	91	VSS	2265	-991	141	COM8	4606	600
42	VSS	-1165	-991	92	INTRS	2335	-991	142	COM7	4606	660
43	VSS	-1095	-991	93	VDD	2405	-991	143	COM6	4606	720
44	VSS	-1025	-991	94	DUMMY	2485	-991	144	DUMMY	4606	800
45	VSS	-955	-991	95	TEST0	2565	-991	145	DUMMY	4430	991
46	VOUT	-885	-991	96	TEST1	2635	-991	146	COM5	4350	991
47	VOUT	-815	-991	97	TEST2	2705	-991	147	COM4	4290	991
48	VOUT	-745	-991	98	TEST3	2775	-991	148	COM3	4230	991
49	VOUT	-675	-991	99	TEST4	2845	-991	149	COM2	4170	991
50	C4+	-605	-991	100	TEST5	2915	-991	150	COM1	4110	991

* 1. NC0, NC1: No Connection
  2. Main VSS pad (PAD No. 41,42,43,44 and 45) have to be connected

Table 4-2. Pad center coordinates (continued) [**Unit: um**]

PAD No.	Pad name	X	Y	PAD No.	Pad name	X	Y	PAD No.	PAD name	X	Y
151	COM0	4050	991	201	SEG48	1050	991	251	SEG98	-1950	991
152	COMS	3990	991	202	SEG49	990	991	252	SEG99	-2010	991
153	SEG0	3930	991	203	SEG50	930	991	253	SEG100	-2070	991
154	SEG1	3870	991	204	SEG51	870	991	254	SEG101	-2130	991
155	SEG2	3810	991	205	SEG52	810	991	255	SEG102	-2190	991
156	SEG3	3750	991	206	SEG53	750	991	256	SEG103	-2250	991
157	SEG4	3690	991	207	SEG54	690	991	257	SEG104	-2310	991
158	SEG5	3630	991	208	SEG55	630	991	258	SEG105	-2370	991
159	SEG6	3570	991	209	SEG56	570	991	259	SEG106	-2430	991
160	SEG7	3510	991	210	SEG57	510	991	260	SEG107	-2490	991
161	SEG8	3450	991	211	SEG58	450	991	261	SEG108	-2550	991
162	SEG9	3390	991	212	SEG59	390	991	262	SEG109	-2610	991
163	SEG10	3330	991	213	SEG60	330	991	263	SEG110	-2670	991
164	SEG11	3270	991	214	SEG61	270	991	264	SEG111	-2730	991
165	SEG12	3210	991	215	SEG62	210	991	265	SEG112	-2790	991
166	SEG13	3150	991	216	SEG63	150	991	266	SEG113	-2850	991
167	SEG14	3090	991	217	SEG64	90	991	267	SEG114	-2910	991
168	SEG15	3030	991	218	SEG65	30	991	268	SEG115	-2970	991
169	SEG16	2970	991	219	SEG66	-30	991	269	SEG116	-3030	991
170	SEG17	2910	991	220	SEG67	-90	991	270	SEG117	-3090	991
171	SEG18	2850	991	221	SEG68	-150	991	271	SEG118	-3150	991
172	SEG19	2790	991	222	SEG69	-210	991	272	SEG119	-3210	991
173	SEG20	2730	991	223	SEG70	-270	991	273	SEG120	-3270	991
174	SEG21	2670	991	224	SEG71	-330	991	274	SEG121	-3330	991
175	SEG22	2610	991	225	SEG72	-390	991	275	SEG122	-3390	991
176	SEG23	2550	991	226	SEG73	-450	991	276	SEG123	-3450	991
177	SEG24	2490	991	227	SEG74	-510	991	277	SEG124	-3510	991
178	SEG25	2430	991	228	SEG75	-570	991	278	SEG125	-3570	991
179	SEG26	2370	991	229	SEG76	-630	991	279	SEG126	-3630	991
180	SEG27	2310	991	230	SEG77	-690	991	280	SEG127	-3690	991
181	SEG28	2250	991	231	SEG78	-750	991	281	SEG128	-3750	991
182	SEG29	2190	991	232	SEG79	-810	991	282	SEG129	-3810	991
183	SEG30	2130	991	233	SEG80	-870	991	283	SEG130	-3870	991
184	SEG31	2070	991	234	SEG81	-930	991	284	SEG131	-3930	991
185	SEG32	2010	991	235	SEG82	-990	991	285	COM32	-3990	991
186	SEG33	1950	991	236	SEG83	-1050	991	286	COM33	-4050	991
187	SEG34	1890	991	237	SEG84	-1110	991	287	COM34	-4110	991
188	SEG35	1830	991	238	SEG85	-1170	991	288	COM35	-4170	991
189	SEG36	1770	991	239	SEG86	-1230	991	289	COM36	-4230	991
190	SEG37	1710	991	240	SEG87	-1290	991	290	COM37	-4290	991
191	SEG38	1650	991	241	SEG88	-1350	991	291	COM38	-4350	991
192	SEG39	1590	991	242	SEG89	-1410	991	292	DUMMY	-4430	991
193	SEG40	1530	991	243	SEG90	-1470	991	293	DUMMY	-4606	800
194	SEG41	1470	991	244	SEG91	-1530	991	294	COM39	-4606	720
195	SEG42	1410	991	245	SEG92	-1590	991	295	COM40	-4606	660
196	SEG43	1350	991	246	SEG93	-1650	991	296	COM41	-4606	600
197	SEG44	1290	991	247	SEG94	-1710	991	297	COM42	-4606	540
198	SEG45	1230	991	248	SEG95	-1770	991	298	COM43	-4606	480
199	SEG46	1170	991	249	SEG96	-1830	991	299	COM44	-4606	420
200	SEG47	1110	991	250	SEG97	-1890	991	300	COM45	-4606	360

Table 4-2. Pad center coordinates (continued) [**Unit: um**]

PAD No.	Pad name	X	Y	PAD No.	Pad name	X	Y	PAD No.	PAD name	X	Y
301	COM46	-4606	300								
302	COM47	-4606	240								
303	COM48	-4606	180								
304	COM49	-4606	120								
305	COM50	-4606	60								
306	COM51	-4606	0								
307	COM52	-4606	-60								
308	COM53	-4606	-120								
309	COM54	-4606	-180								
310	COM55	-4606	-240								
311	COM56	-4606	-300								
312	COM57	-4606	-360								
313	COM58	-4606	-420								
314	COM59	-4606	-480								
315	COM60	-4606	-540								
316	COM61	-4606	-600								
317	COM62	-4606	-660								
318	COM63	-4606	-720								
319	COMS	-4606	-780								
320	DUMMY	-4606	-860								

5. PIN DESCRIPTION

Table 5-1. Pin description

<table>
<tr><td colspan="3">Power supply</td></tr>
<tr><td>Name</td><td>I/O</td><td>Description</td></tr>
<tr><td>VDD</td><td rowspan="2">Power supply</td><td>Shared with the MPU power supply terminal VCC.</td></tr>
<tr><td>VSS</td><td>This is a 0V terminal connected to the system GND.
Main VSS pad (PAD No. 41,42,43,44 and 45) have to be connected</td></tr>
<tr><td>V0
V1
V2
V3
V4</td><td>I/O</td><td>The voltage is determined by the LCD pixel impedance-converted for application by an operational amplifier. Voltage have the following relationship:
V0 ≥V1≥V2≥V3≥V4≥VSS(GND)
When the on-chip power circuit is active, these voltages are generated according to the state of LCD bias, as shown in the table below.
<table>
<tr><th>LCD Bias</th><th>V1</th><th>V2</th><th>V3</th><th>V4</th></tr>
<tr><td>1/9 bias</td><td>(8/9) x V0</td><td>(7/9) x V0</td><td>(2/9) x V0</td><td>(1/9) x V0</td></tr>
<tr><td>1/8 bias</td><td>(7/8) x V0</td><td>(6/8) x V0</td><td>(2/8) x V0</td><td>(1/8) x V0</td></tr>
<tr><td>1/7 bias</td><td>(6/7) x V0</td><td>(5/7) x V0</td><td>(2/7) x V0</td><td>(1/7) x V0</td></tr>
<tr><td>1/6 bias</td><td>(5/6) x V0</td><td>(4/6) x V0</td><td>(2/6) x V0</td><td>(1/6) x V0</td></tr>
<tr><td>1/5 bias</td><td>(4/5) x V0</td><td>(3/5) x V0</td><td>(2/5) x V0</td><td>(1/5) x V0</td></tr>
</table></td></tr>
<tr><td colspan="3">LCD driver power supply</td></tr>
<tr><td>Name</td><td>I/O</td><td>Description</td></tr>
<tr><td>C1+</td><td rowspan="6">O</td><td>Capacitor1+ positive connection pin for the voltage converter</td></tr>
<tr><td>C1-</td><td>Capacitor1- negative connection pin for voltage converter</td></tr>
<tr><td>C2+</td><td>Capacitor2+ positive connect ion pin for voltage converter</td></tr>
<tr><td>C2-</td><td>Capacitor2- negative connection pin for voltage converter</td></tr>
<tr><td>C3+</td><td>Capacitor3+ positive connection pin for voltage converter</td></tr>
<tr><td>C4+</td><td>Capacitor4+ positive connection pin for voltage converter</td></tr>
<tr><td>VOUT</td><td>I/O</td><td>Voltage converter input / output pin
Connect this pin to VSS through capacitor.</td></tr>
<tr><td>VR</td><td>I</td><td>V0 voltage adjustment pin. It is valid only when using external resistors.(INTRS=”L”)</td></tr>
<tr><td>VCI</td><td>I</td><td>This is the reference voltage for the voltage converter circuit for the LCD drive.
Whether internal voltage converter use or not use, this pin should be fixed.
The voltage should have the following range: 2.4V ≤ VCI ≤ 5.5V</td></tr>
<tr><td>VEXT</td><td>I</td><td>This is the externally input reference voltage (VREF) for the internal voltage regulator.
It is valid only when external VREF is used (REF = “L”).
When using internal VREF, this pin is Open</td></tr>
<tr><td>REF</td><td>I</td><td>Select the external VREF voltage via VEXT pin
-REF = “L”: using the external VREF
-REF = “H”: using the internal VREF</td></tr>
</table>

Table 5-1. Pin description (continued)

<table>
<tr><th colspan="3">System control</th></tr>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MS</td><td>I</td><td>Master/slave mode select input. Master makes some signals for display, and slave receives them. This for display synchronization.
MS =”H”: Master mode
MS =”L”: Slave mode
<table>
<tr><th>MS</th><th>CLS</th><th>OSC Circuit</th><th>Power Supply</th><th>CL</th><th>M</th><th>FRS, FR</th><th>DISP</th></tr>
<tr><td rowspan="2">H</td><td>H</td><td>Enable</td><td>Enable</td><td>Output</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>Disable</td><td>Enable</td><td>Input</td><td>Output</td><td>Output</td><td>Output</td></tr>
<tr><td>L</td><td>-</td><td>Disable</td><td>Disable</td><td>Input</td><td>Input</td><td>Output</td><td>Input</td></tr>
</table></td></tr>
<tr><td>CLS</td><td>I</td><td>Built-in oscillator circuit enables / disable select pin.
CLS = “H”: Enable
CLS = ”L”: Disable (external display clock input to CL pin)</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input / output pin. When HT0324A is used in master/slave mode(multi-chip), the CL pin must be connected to each other.</td></tr>
<tr><td>M</td><td>I/O</td><td>LCD AC signal input / output pin.
When HT0324A is used in master/slave mode(multi-chip), the M pin must be connected to each other.
MS = “H”: Output
MS = “L”: Input</td></tr>
<tr><td>FRS</td><td>O</td><td>Static driver segment output. This pin is used together with the FR pin.</td></tr>
<tr><td>FR</td><td>O</td><td>Static driver common output. This pin is used together with the FRS pin.</td></tr>
<tr><td>DISP</td><td>I/O</td><td>LCD display blanking control input/output. When HT0324A is used in master/slave mode (multi-chip), the DISP pin must be connected to each other.
MS = “H”: Output
MS = “L”: Input</td></tr>
<tr><td>INTRS</td><td>I</td><td>Internal resistor selects pin.
This pin selects the resistor for adjusting V0 voltage level and is available only in master mode.
INTRS = “H”: using built-in resistors.
INTRS = “L”: not using built-in resistors.
V0 voltage is controlled by VR pin with external resistive divider.</td></tr>
<tr><td>/HPM</td><td>I</td><td>Power control pin of the power supply circuits for LCD driver
- /HPM = “H”: normal mode
- /HPM = “L”: high power mode
This pin is valid only in master operation.</td></tr>
<tr><td>DSEL1
DSEL0</td><td>I</td><td>The LCD driver duty ratio depends on the following table.
<table>
<tr><th>DSEL1</th><th>DSEL0</th><th>DUTY RATIO</th></tr>
<tr><td>L</td><td>L</td><td>1/33</td></tr>
<tr><td>L</td><td>H</td><td>1/49</td></tr>
<tr><td>H</td><td>L</td><td>1/55</td></tr>
<tr><td>H</td><td>H</td><td>1/65</td></tr>
</table></td></tr>
</table>

Table 5-1. Pin description (continued)

<table>
<tr><td colspan="3">MPU interface</td></tr>
<tr><td>Name</td><td>I/O</td><td>Description</td></tr>
<tr><td>/RESET</td><td>I</td><td>Hardware reset input pin.
When /RESET is “L”, initialization is executed.</td></tr>
<tr><td>PS</td><td>I</td><td>Parallel/Serial select input pin.
<table>
<tr><th>PS</th><th>Operating mode</th><th>Chip select</th><th>Data/ Instruction</th><th>Data I/O</th><th>Read/ Write</th><th>Serial</th></tr>
<tr><td>H</td><td>Parallel</td><td>/CS1, CS2</td><td>RS</td><td>DB7 to DB0</td><td>E_/RD, RW_/WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>/CS1, CS2</td><td>RS</td><td>DB7 (SID)</td><td>Write only</td><td>DB6 (SCLK)</td></tr>
</table>
When PS= “L”, DB5 to DB0 are high impedance.
E_/RD and RW_/WR are fixed to either “H” or “L”.
With serial data input, RAM display data reading is not supported.</td></tr>
<tr><td>C68</td><td>I</td><td>This pin is the MPU interface switch terminal.
C68 = “H”: 6800 series MPU interface
C68 = “L”: 8080 series MPU interface</td></tr>
<tr><td>/CS1
CS2</td><td>I</td><td>Chip select input pin.
Data input/output is enables only when /CS1 is low and CS2 is high.
When chip select is non-active, DB7 to DB0 will be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin.
RS = “H”: The data on DB7 to DB0 is used the display data.
RS = “L”: The data on DB7 to DB0 is used the control data.</td></tr>
<tr><td>RW_/WR</td><td>I</td><td>When interfacing to a 6800-series MPU, read/write is enabled at;
RW_/WR = “H”: read
RW_/WR = “L”: write
When interfacing to an 8080-series MPU, RW_/WR is enabled at low.
The signals on the data bus are latched at the rising edge of the RW_/WR signal.</td></tr>
<tr><td>E_/RD</td><td>I</td><td>When interfacing to a 6800-series MPU: Active High.
This pin is used as an enable clock input pin of the 6800-series MPU.
When interfacing to a 8080-series MPU: Active Low.
This pin is connected to the RD signal of the 8080-series MPU. While this signal is Low, HT0324A data bus output is enabled.</td></tr>
<tr><td>DB7
to
DB0</td><td>I/O</td><td>8-bit bi-directional data bus.
It is connected to the standard 8-bit microprocessor data bus.
In case of serial interface,(PS = ”L”)
DB7: Serial input data(SID)
DB6: Serial input clock(SCLK)
DB5 to DB0 : High impedance
When chip select is not active, DB7 to DB0 will be high impedance.</td></tr>
<tr><td>NC1
NC0</td><td>I/O</td><td>These are set to Open.</td></tr>
<tr><td>TEST20
to
TEST0</td><td>I/O</td><td>These are pins for IC chip testing.
These are set to Open.</td></tr>
</table>

Table 5-1. Pin description (continued)

<table>
<tr><th colspan="3">LCD driver output</th></tr>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEG0
to
SEG131</td><td>O</td><td>LCD driver output for segment. The display data and the FR signal control the output voltage of segment driver.
<table>
<tr><th rowspan="2">Display data</th><th rowspan="2">FR</th><th colspan="2">Segment output voltage</th></tr>
<tr><th>Normal display</th><th>Reverse display</th></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>VSS</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>VSS</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">VSS</td></tr>
</table></td></tr>
<tr><td>COM0
to
COM63</td><td>O</td><td>LCD driver output for common. The internal scanning data and M signal control the output voltage of common driver.
<table>
<tr><th>Scan data</th><th>FR</th><th>Common output voltage</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
<tr><td colspan="2">Power save mode</td><td>VSS</td></tr>
</table></td></tr>
<tr><td>COMS</td><td>O</td><td>Common signal output for the icons. The output signals of two pins are the same. When this signal is not used, should be left open. In multi-chip(master/slave) mode, all COMS pin on both master and slave units are the same signal.</td></tr>
</table>

Note:
-. DUMMY, TEST0 ~ TEST20, NC0, NC1: The pins should be opened(floated).

6. FUNCTIONAL DESCRIPTION

6-1. MICROPROCESSOR INTERFACE

a. Chip select input

There are /CS1 and CS2 pins for chip selection. The HT0324A can interface with an MPU only when /CS1 is “L” and CS2 is “H”. When these pins are set to any other combination, RS, E_/RD, and RW_/WR inputs are disabled and DB7 to DB0 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

b. Interface

HT0324A has three types of interface with an MPU, which are one serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in table 6-1.

Table 6-1. Parallel / Serial interface mode

PS	Type	/CS1	CS2	C68	Interface mode
H	Parallel	/CS1	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	/CS1	CS2	X*	Serial MPU mode

* X : Don't care

c. Parallel interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in table 6-2. The type of data transfer is determined by signals at RS, E_/RD, and RW_/WR as shown in table 6-3.

Table 6-2. Microprocessor selection for parallel interface

C68	/CS1	CS2	RS	E_/RD	RW_/WR	DB7 to DB0	MPU
H	/CS1	CS2	RS	E	RW	DB7 to DB0	6800-series
L	/CS1	CS2	RS	/RD	/WR	DB7 to DB0	8080-series

Table 6-3. Parallel data transfer

Common	6800-series		8080-series		Description
RS	E_/RD (E)	RW_/WR (RW)	E_/RD (/RD)	RW_/WR (/WR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Register status read
L	H	L	H	L	Writes to internal register(instruction)

d. Serial interface (PS = "L")

When the HT0324A is active and serial interface has been selected, the serial data (DB7) and the serial clock (DB6) inputs are enabled. And HT0324A is not active, the internal 8-bit shift register and the 3-bit counter are reset. The serial data can be read on the rising edge of the serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. The serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

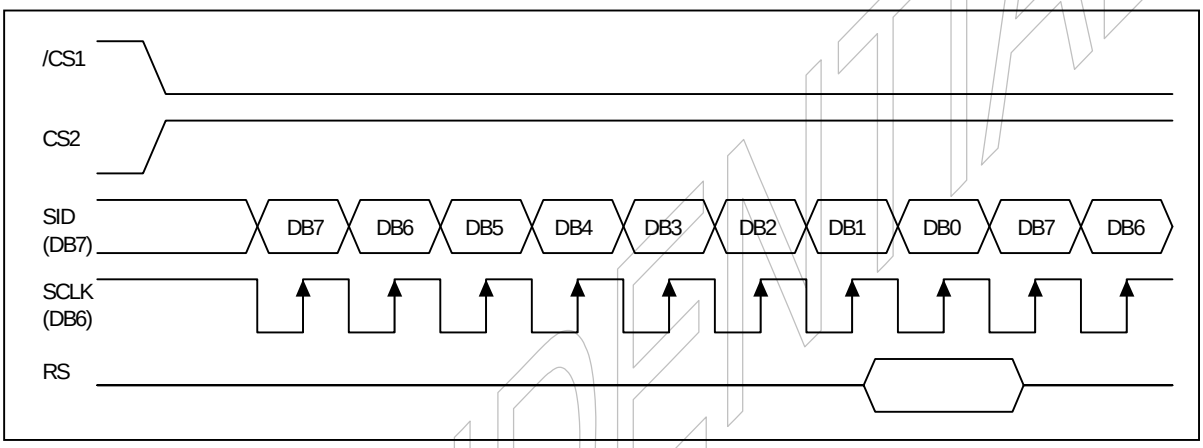

Figure 6-1. Serial interface timing

e. Busy flag

The busy flag indicates whether the HT0324A is operating or not. When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the MPU needs not to check this flag before each instruction, which improves the MPU performance.

f. Data accessing

The HT0324A uses bus holder and internal data bus for data read and data write with the MPU.
When writing data from the MPU to on-chip RAM, the data is automatically transferred from the bus holder to the on-chip RAM as shown in figure 6-2. When the MPU reads data from on-chip RAM, the first data read cycle stores the data in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 6-3. This means the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data. Therefore, a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed.

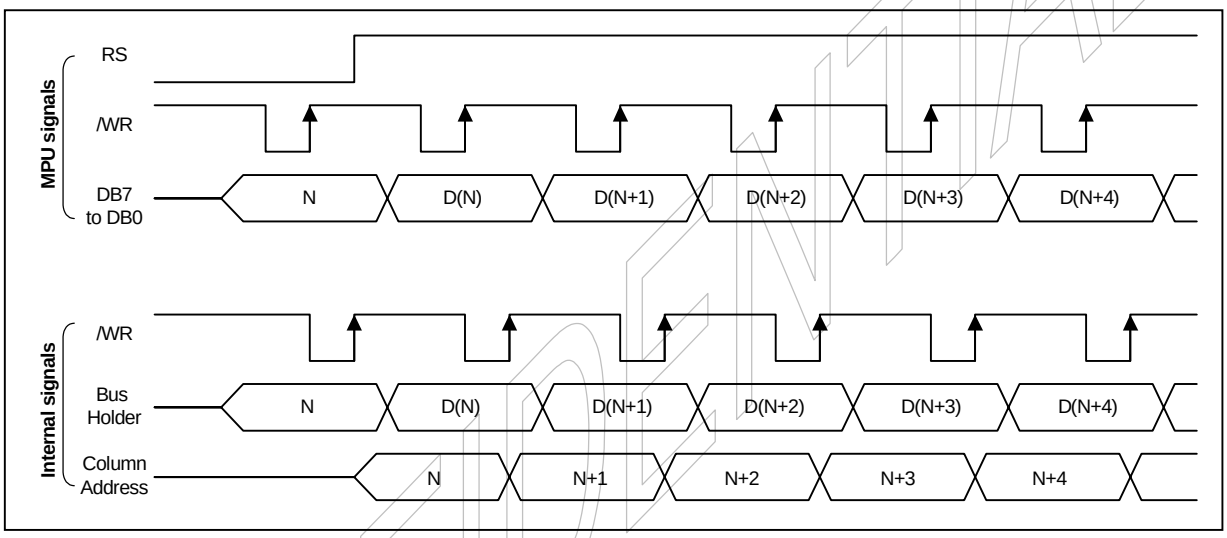

Figure 6-2. Write timing

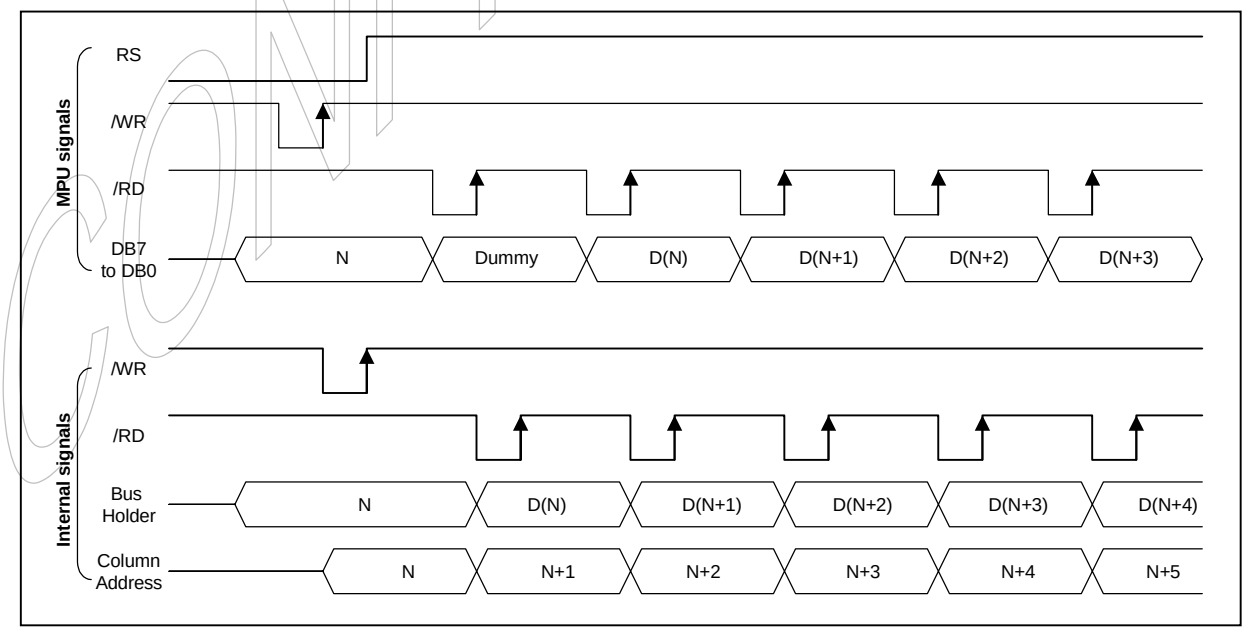

Figure 6-3. Read timing

6-2. DISPLAY DATA RAM (DDRAM)

a. DDRAM

The DDRAM stores pixel data for the LCD. It has 65-row (8 page x 8 bit + 1) by 132-column addressable array. Each pixel can be selected by specifying the page and the column address. The 65 rows are divided into 8 pages of 8 lines and the 9th page with a single line (DB0 only). Data is read from or written to the 8 lines of each page directly through DB7 to DB0. The display data of DB0 to DB7 from the MPU correspond to the LCD common direction as shown in Figure 6-4.
The MPU can read from and write to DDRAM through the I/O buffer, which is independent operation from signal reading for the LCD driver. This independent operation makes it possible that the MPU writes the data into the DDRAM at the same time as data is being displayed without causing the LCD flicker.

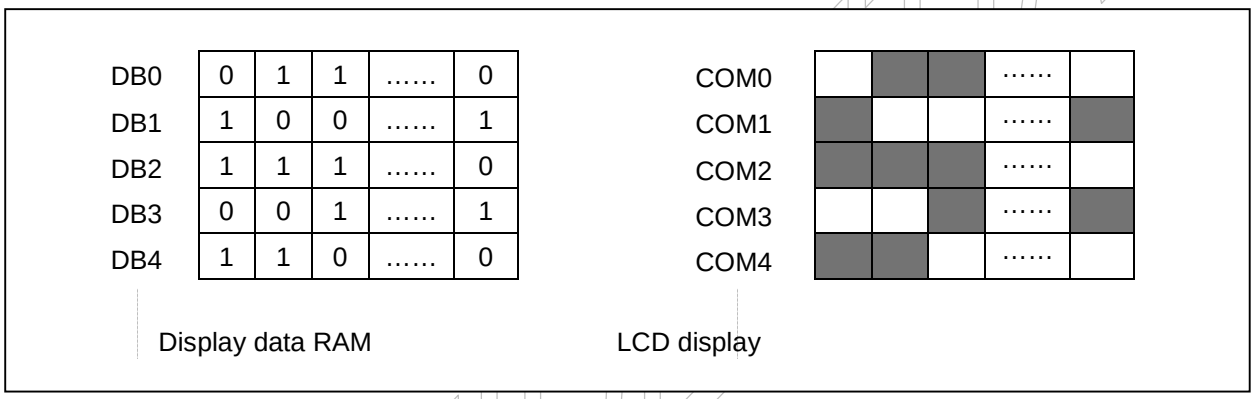

Figure 6-4. RAM-to-LCD data transfer

b. Page address circuit

This circuit is for providing a page address to DDRAM shown in figure 6-6. The 4-bit page address register changed by only the “Set page” instruction. Page address 8 (DB3, DB2, DB1, DB0 = 1, 0, 0, 0) is a special RAM area for the icons and display data DB0 is only valid.
When Page Address is above 8, it is impossible to access to on-chip RAM.

c. Column address circuit

Column address circuit has a 8-bit preset counter that provides column address to the DDRAM as shown in figure 6-6. When the “Set column address MSB / LSB” instruction is issued, 8-bit [Y7:Y0] is updated. And this address is increased by +1 each display data Read/Write instruction. This allows that the MPU display data can be accessed continuously. The increment of the column address stops with 83H. And the counter is not increased and locked if the address is specified over 84H. It is unlocked if a column address is set again by “Set column address MSB / LSB” instruction. The column address counter is independent of the page address register.
The ADC select instruction makes it possible to convert the relationship between the column address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing the ADC select instruction. Refer to the figure 6-5.

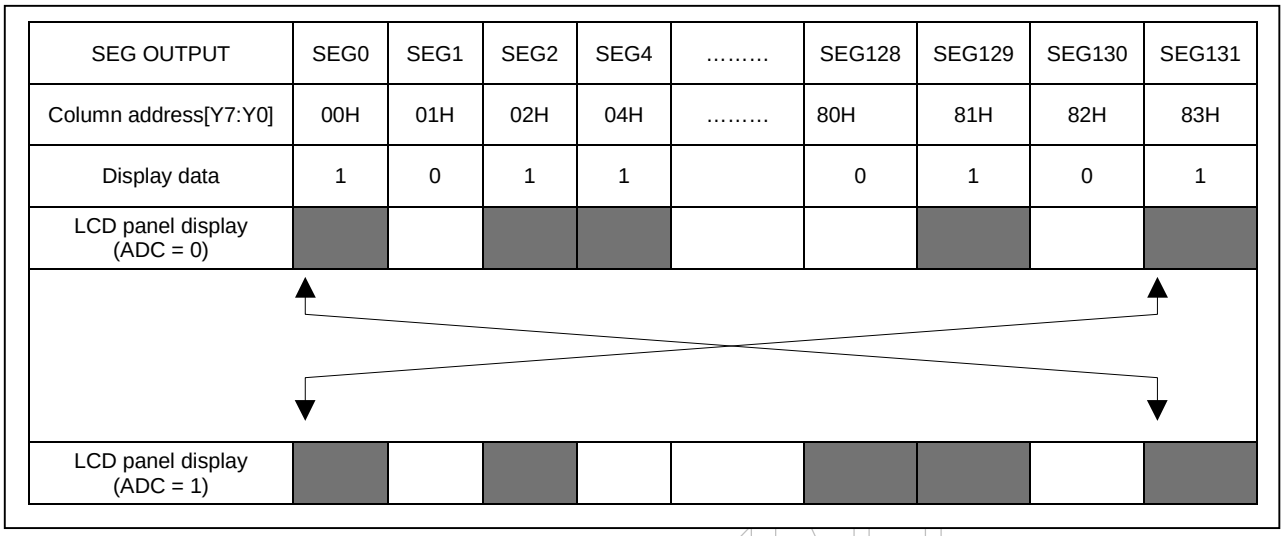

Figure 6-5. The relationship between the column address and the segment outputs

d. Line address circuit

This circuit assigns DDRAM a line address corresponding to the first line (COM0) of the display. Using the display start line address set command, what is normally the top line of the display can be specified.
By setting the line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of DDRAM as shown in figure 6-6.
At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by +1 and the line address is generated for transferring the 132-bit RAM data to the display data latch circuit. However, the display data of icons is not scrolled because the MPU can not access the line address of icons.

e. Segment control circuit

This circuit controls the display data by the Display ON / OFF, reverse display ON / OFF and entire display ON /OFF instructions without changing the data in the DDRAM.

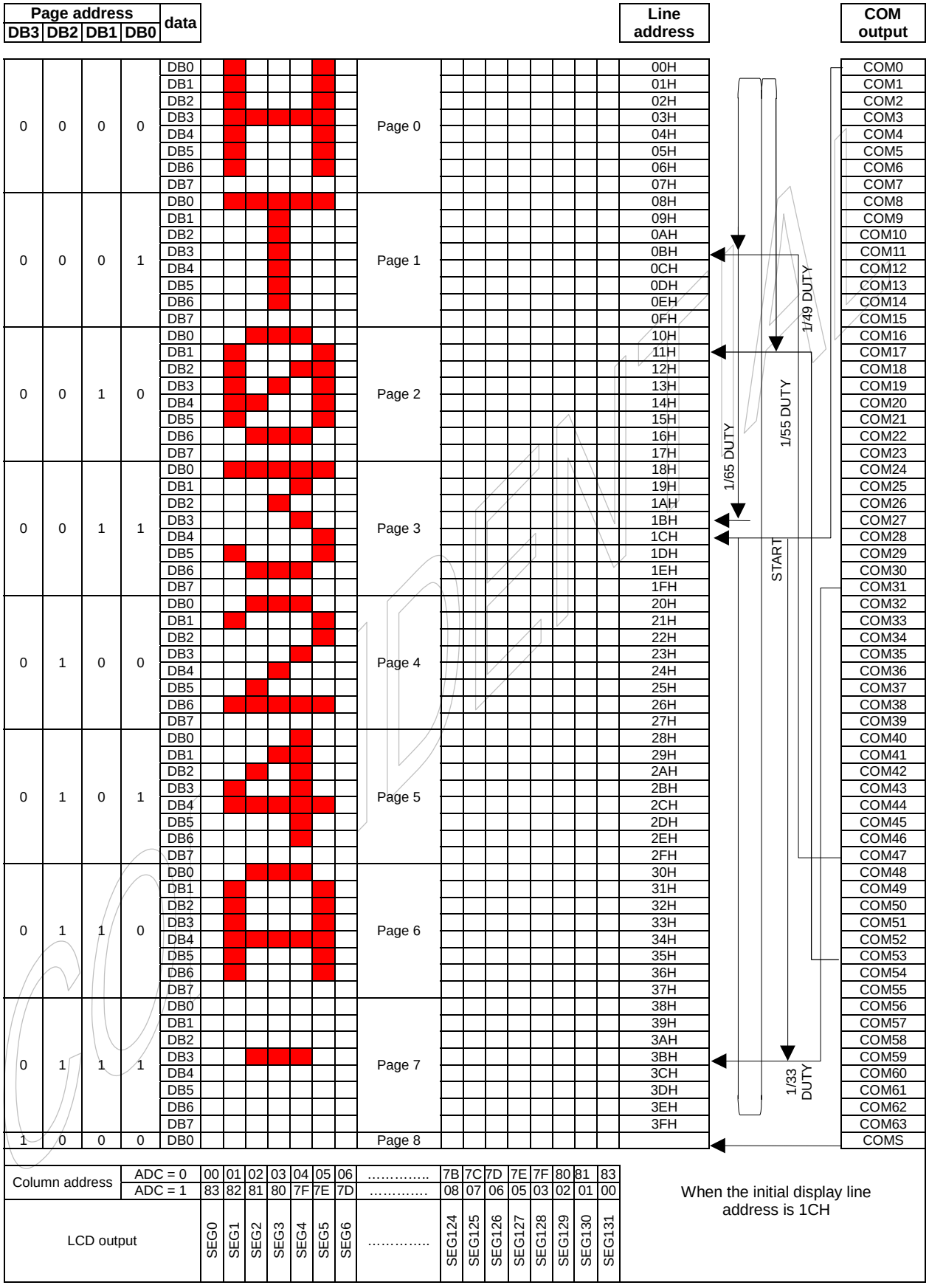

Figure 6-6. Display data RAM map

6-3. LCD DISPLAY CIRCUITS

a. Oscillator

HT0324A implement complete on-chip oscillator and its frequency is nearly independent of V_{DD}.
This oscillator signal is used in the voltage converter and display timing generation circuit.
The oscillator circuit is enabled when MS="H" and CLS="H". When the external clock is used, set CLS="L" and imply clock signal to CL pin.

b. Display timing generator circuit

This circuit generates timing signals to be used for displaying LCD. The display clock (CL) is generated by oscillation clock and CL generates the clock for the line counter and the signal for the display data latch. The line address of DDRAM is generated in synchronization with CL. The 132-bit display data is latched in the display data latch circuit synchronized with CL. Reading to the display data liquid crystal driver circuit is completely independent of access to the DDRAM by the MPU. The display timing generator circuit generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving 2-frame AC driver waveform and internal timing signal are shown in figure 6-7.
When HT0324A is used multiple-chip configuration, the slave chip requires the M, CL and DISP signals from the master. Table 6-4 shows the M, CL, and DISP status.

Table 6-4. Master and slave timing signal status

Operation mode	Clock	MS	CLS	M	CL	FRS, FR	DISP
Master mode	Internal	H	H	Output	Output	Output	Output
	External	H	L	Output	Input	Output	Output
Slave mode	Internal	L	H	Input	Input	Output	Input
	External	L	L	Input	Input	Output	Input

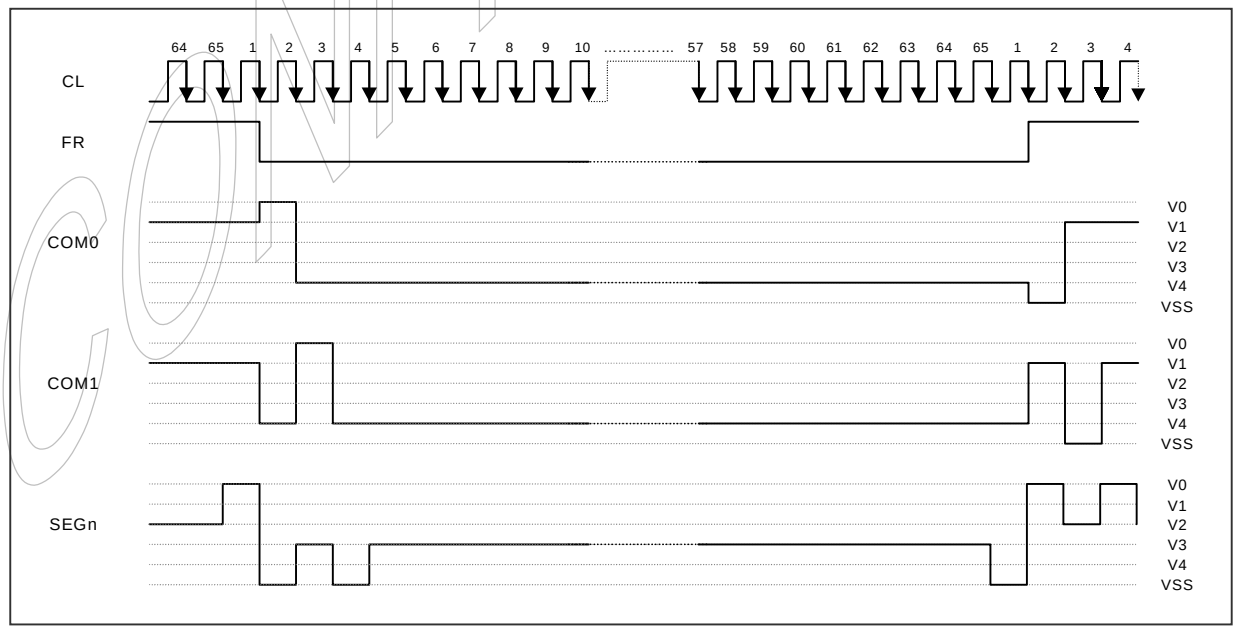

Figure 6-7. 2-frame AC driving waveform (Duty ratio = 1/65)

c. Common output control circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL select instruction specifies the scanning direction of the common output pins.

Table 6-5. The relationship between duty ratio and common output

Duty	SHL	Common output pins							
		COM [0:15]	COM [16:23]	COM [24:26]	COM [27:36]	COM [37:39]	COM [40:47]	COM [48:63]	COMS
1/33	0	COM[0:15]	*NC					COM[16:31]	COMS
	1	COM[31:16]	*NC					COM[15:0]	
1/49	0	COM[0:23]		*NC			COM[24:47]		COMS
	1	COM[47:24]		*NC			COM[23:0]		
1/55	0	COM[0:26]			*NC	COM[27:53]			COMS
	1	COM[53:27]			*NC	COM[26:0]			
1/65	0	COM[0:63]							COMS
	1	COM[63:0]							

*NC : No Connection

6-4. LCD DRIVER CIRCUIT

This driver circuit is configured by 66-channel common drivers (including 2COMS channels) and 132-channel segment drivers. This LCD panel driver voltage depends on the combination of display data and FR signal.

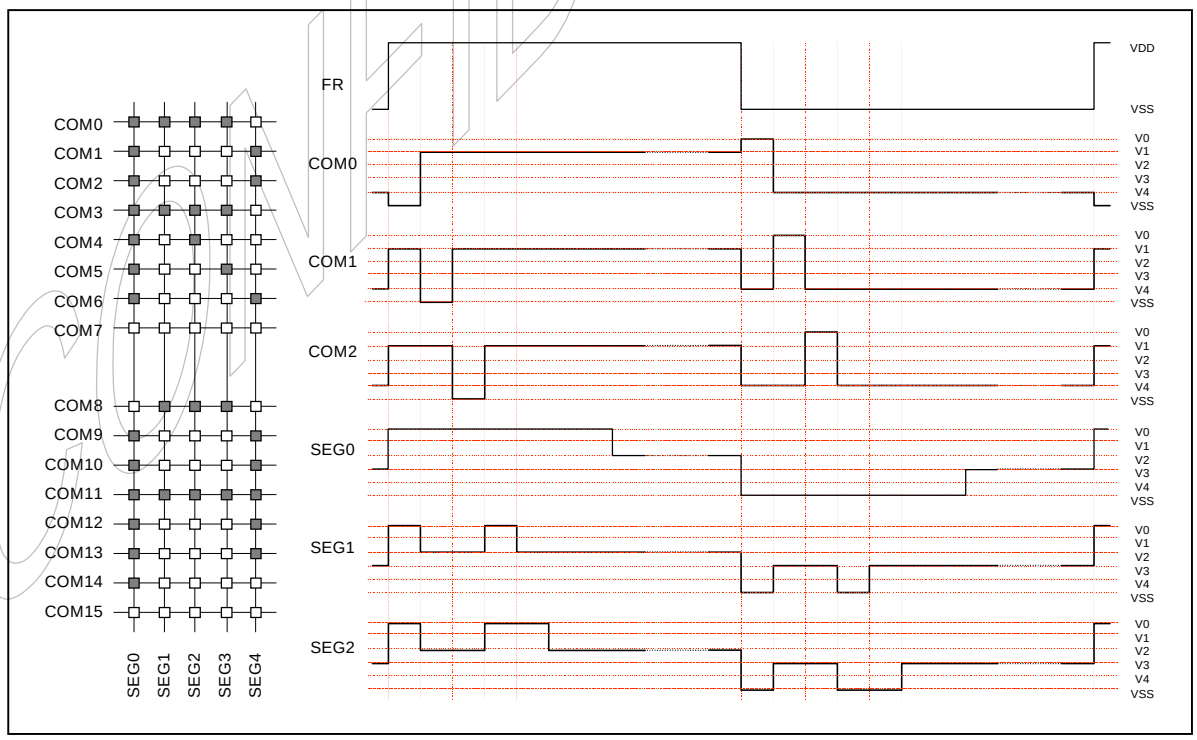

Figure 6-8. Segment and common timing

6-5. POWER SUPPLY CIRCUITS

The power supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction.
For details, refers to "Instruction description". Table 6-6 shows the referenced combinations in using power supply circuits.

Table 6-6. Recommended power supply combinations

Mode Settings	VC,VR,VF	Voltage converter	Voltage regulator	Voltage follower	VOUT	V0	V1 to V4
All Internal power supply	1, 1, 1	ON	ON	ON	Open	Open	Open
Voltage regulator and voltage follower	0, 1, 1	OFF	ON	ON	External input	Open	Open
Voltage follower	0 , 0, 1	OFF	OFF	ON	Open	External input	Open
All external power supply	0, 0, 0	OFF	OFF	OFF	Open	External input	External input

a. Voltage converter circuits

These circuits boost up the electric potential between VCI and VSS to 2, 3, 4 or 5 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7μF]

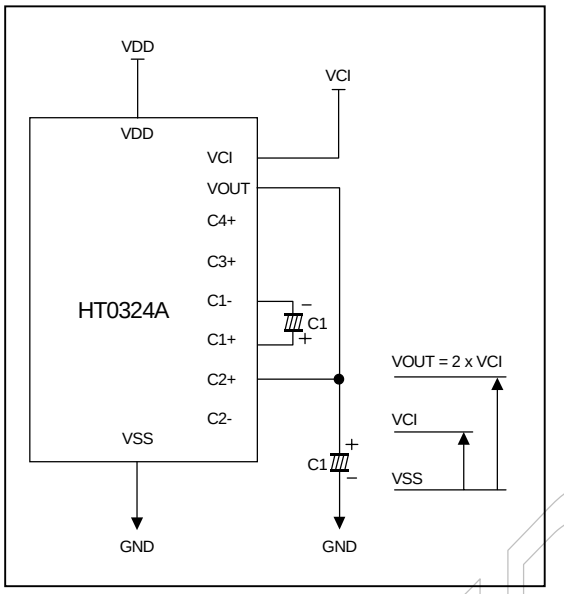

Figure 6-9. Two times boosting circuit

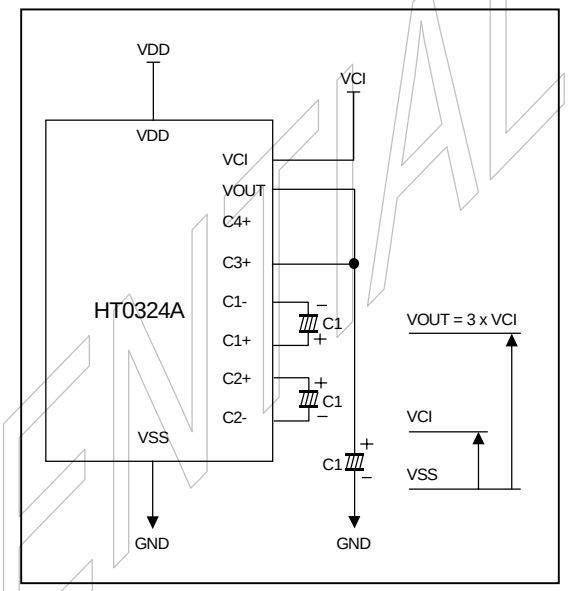

Figure 6-10. Three times boosting circuit

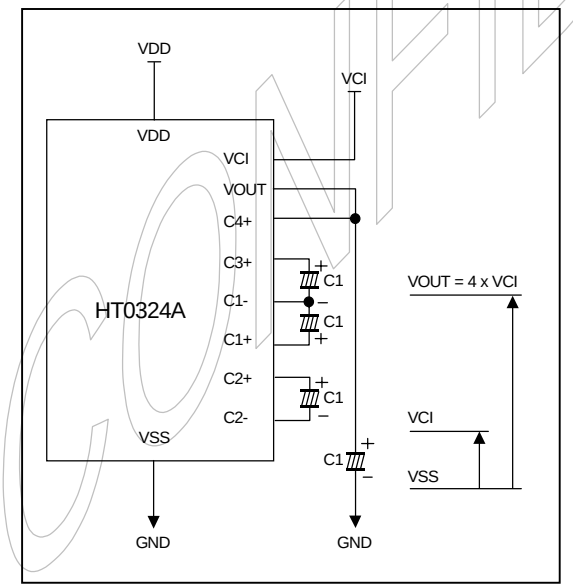

Figure 6-11. Four times boosting circuit

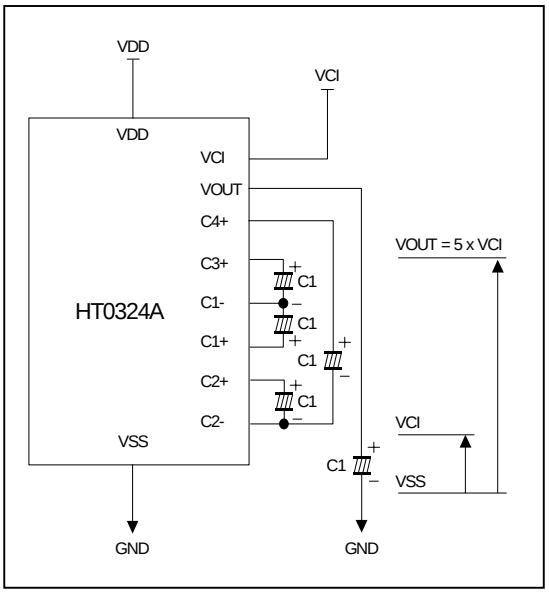

Figure 6-12. Five times boosting circuit

*. The VCI voltage range must be set so that the VOUT voltage does not exceed the absolute maximum rated value.

b. Voltage regulator circuits

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0, by the adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits as shown in figure 6-13, it is necessary to be applied internally or externally.

For the equation 1, we determine V0 by Ra, Rb and V_{EV}. Ra and Rb are connected internally or externally by INTRS pin. The voltage of electronic volume, V_{EV}, is determined by equation 2, where the reference voltage parameter α is the value selected by instruction, "Set reference voltage register", within the range 0 to 63. Refer to table 6-8. VREF voltage at Ta =25°C is show in table 6-7.

$$V0 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV} \quad [V] \quad \text{------ (Equation 1)}$$

$$V_{EV} = \left(1 - \frac{(63-\alpha)}{162}\right) \times VREF \quad [V] \quad \text{------ (Equation 2)}$$

Table 6-7. VREF voltage at Ta =25°C

REF	Temp. coefficient	V_{REF}[V]
H	-0.05% / °C	2.1
L	External input	VEXT

Table 6-8. Electronic contrast control register (Reference Voltage Parameter : α, 64step)

SV5	SV4	SV3	SV2	SV1	SV0	Reference Voltage Parameter (α)	V0	Contrast
0	0	0	0	0	0	0	Minimum	Low
0	0	0	0	0	1	1	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62	:	:
1	1	1	1	1	1	63	Maximum	High

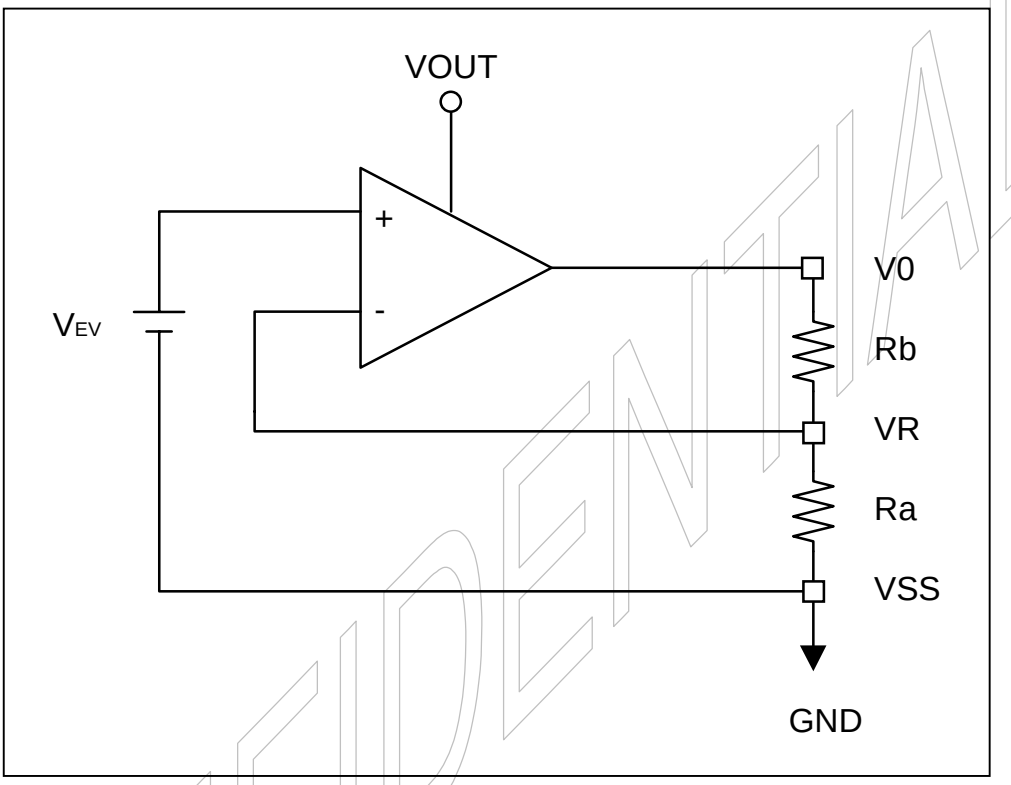

Figure 6-13. Internal voltage regulator circuit

b-1. In case of using internal resistors, Ra and Rb (INTRS = "H")

When INTRS pin is “H”, resistor Ra is connected internally between VR pin and VSS, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator resistor select" and "Set reference voltage".

Table 6-9. Internal Rb / Ra ratio depending on 3-bit Data (R2, R1, R0)

	3-bit data settings(R2 R1 R0: gain)							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
1+(Rb/Ra)	3.0	3.5	4.0	4.5	5.0	5.5	6.0	6.4

The following figure shows V0 voltage measured by adjusting internal regulator resistor ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

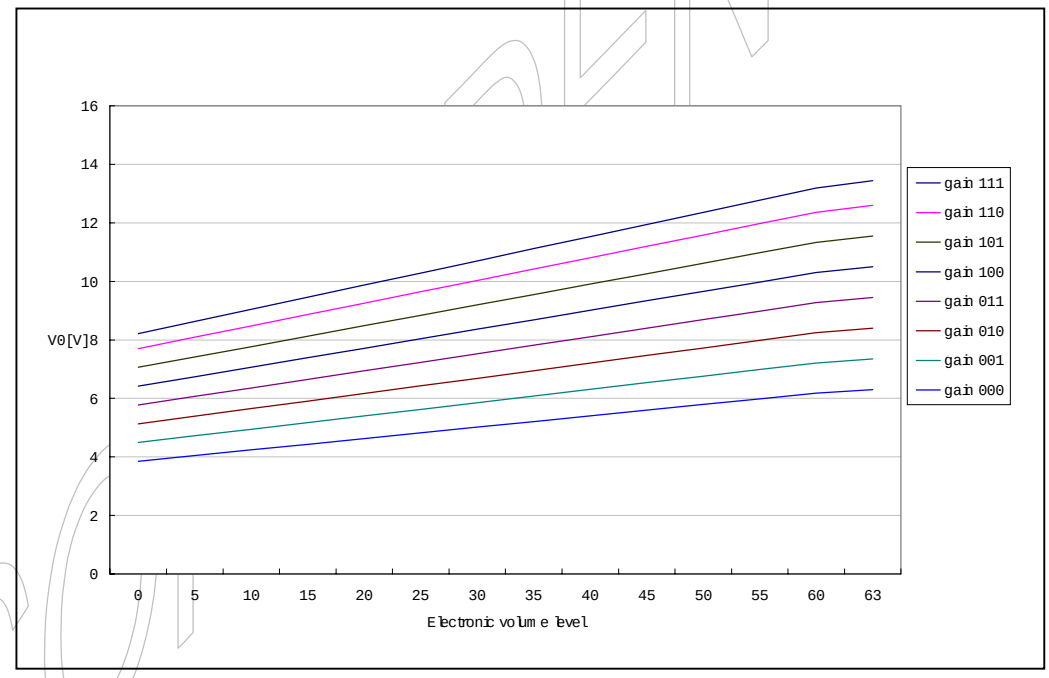

Figure 6-13. Electronic volume level

b-2. In case of using external resistors, Ra and Rb. (INTRS = "L")

When INTRS pin is “L”, it is necessary to connect external regulator resistor Ra between VR and V_{SS}, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0 : α = 32)
3. Maximum current flowing Ra, Rb = 1[μA]

From equation 1

$$10 = \left(1 + \frac{Rb}{Ra}\right) \times V_{EV}\ [V] \quad \text{------} \quad \text{(Equation 3)}$$

From equation 2

$$V_{EV} = \left(1 - \frac{(63-32)}{162}\right) \times 2.1 \cong 1.698\ [V] \quad \text{------ (Equation 4)}$$

From equation 3

$$\frac{10}{(Ra + Rb)} = 1[\mu A] \quad \text{------ (Equation 5)}$$

From equation 3, 4 and 5

Ra = 1.69[MΩ]
Rb = 8.31[MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 6-10. V0 depending on electronic volume level

	Electric Volume Level				
	0	**------**	**32**	**-------**	**63**
V0	7.57	------	10.00	-------	12.43

c. Voltage follower circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4) and those output impedance are converted by the voltage follower for increasing drive capability. The following table shows the relationship between V1 to V4 level and each duty ratio.

Table 6-11. The relationship between V1 to V4 level and duty ratio

Duty Ratio	DSEL1	DSEL0	LCD Bias	V1	V2	V3	V4
1/33	L	L	1/5	(4/5) x V0	(3/5) x V0	(2/5) x V0	(1/5) x V0
			1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
1/49	L	H	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/55	H	L	1/6	(5/6) x V0	(4/6) x V0	(2/6) x V0	(1/6) x V0
			1/8	(7/8) x V0	(6/8) x V0	(2/8) x V0	(1/8) x V0
1/65	H	H	1/7	(6/7) x V0	(5/7) x V0	(2/7) x V0	(1/7) x V0
			1/9	(8/9) x V0	(7/9) x V0	(2/9) x V0	(1/9) x V0

d. High power mode

The power supply circuit equipped in the HT0324A for LCD drive has very low power consumption (in normal mode : /HPM = “H”). If use for LCD panels with large loads, this low-power supply may cause display quality to degrade. When this occurs, setting the /HPM pin to “L”(high power mode) can improve the quality of the display. Moreover, if the quality of display is inadequate even after High Power mode has been set, then it is necessary to add a liquid crystal drive power supply externally (VOUT or V0 or V1 V2 V3 V4).

6-6. REFERECE CIRCUIT EXAMPLS

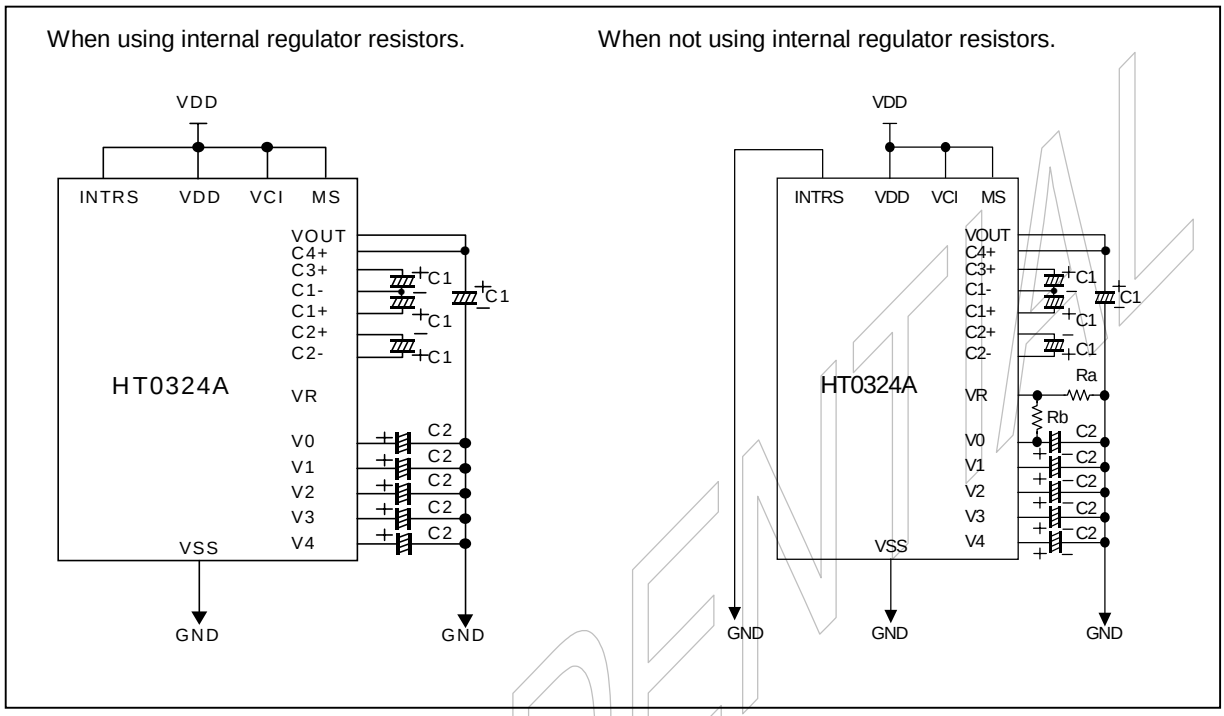

Figure 6-15. When using all LCD power circuits (VCI = VDD, 4-time, V/C: ON, V/R: ON, V/F: ON)

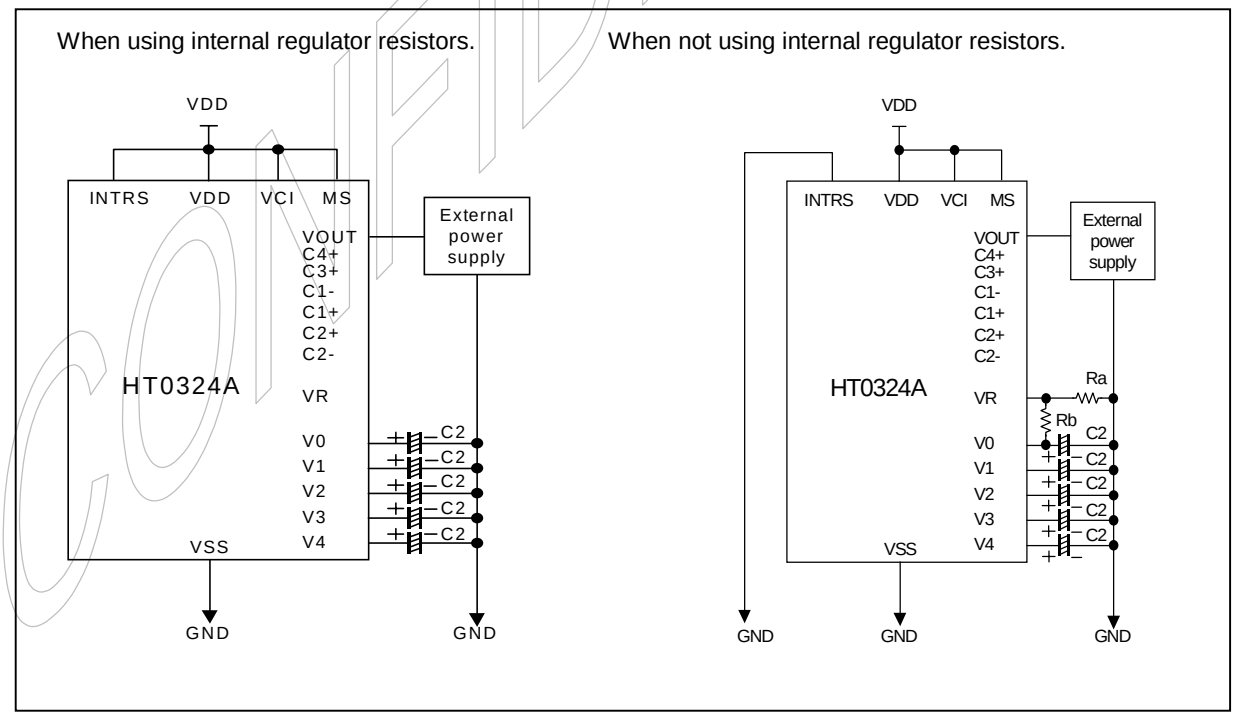

Figure 6-16. When using some LCD power circuits (VCI = VDD, V/C: OFF, V/R: ON, V/F: ON)

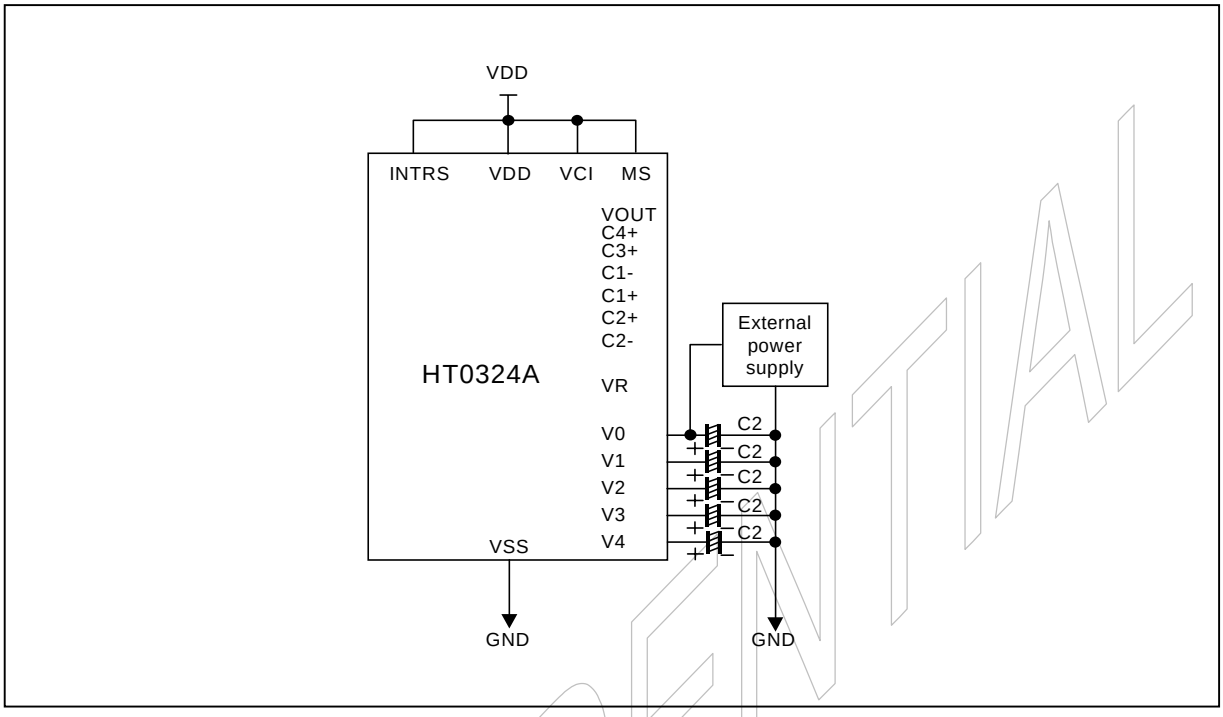

Figure 6-17. When using some LCD power circuits (VCI = VDD, V/C: OFF, V/R: OFF, V/F: ON)

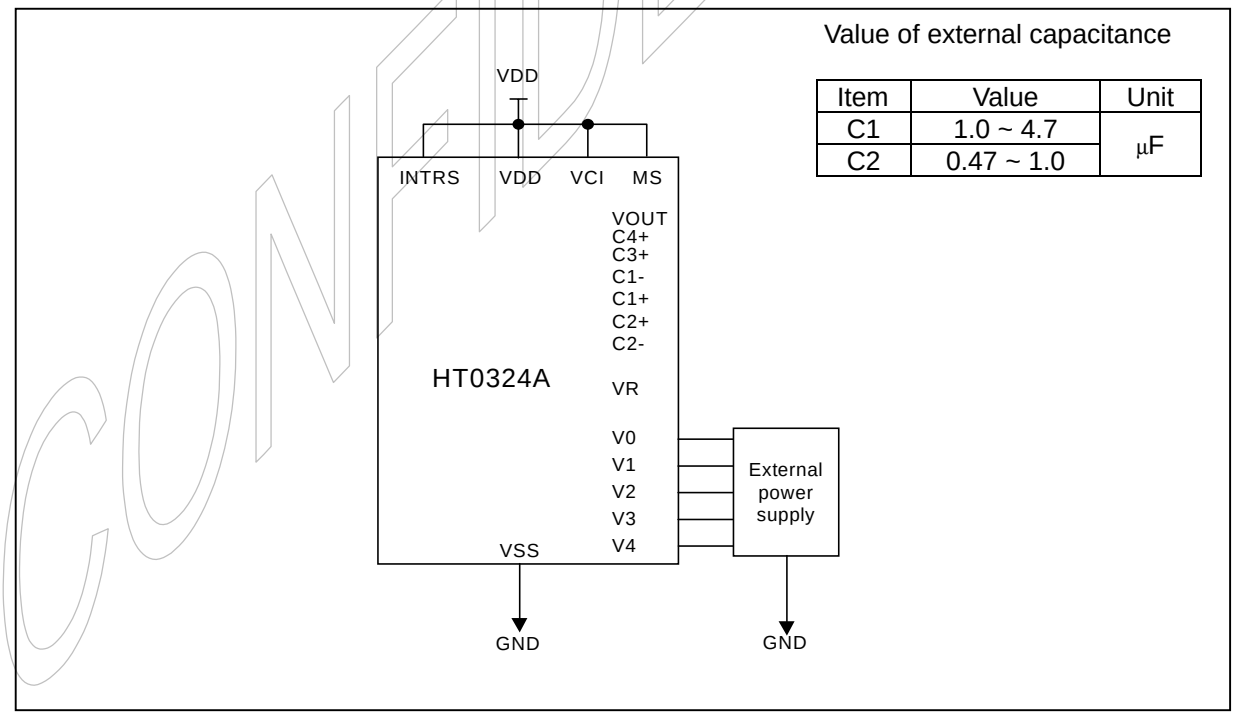

Figure 6-18. When not using any LCD power supply circuits (VCI = VDD, V/C: OFF, V/R: OFF, V/F: OFF)

*. C1 and C2 are determined by the size of the LCD being driven.
Select a value that will stabilize the liquid crystal drive voltage.

6-7. RESET CIRCUIT

Setting /RESET to “L” or reset instruction can initialize internal function.
When /RESET becomes “L”, following procedure is occurred.

Display ON / OFF: OFF (DON = 0).
Entire display ON / OFF: OFF (normal = 0).
ADC select: OFF (normal = 0)
Reverse display ON / OFF: OFF (normal = 0).
Power control register (VC, VR, VF) = (0, 0, 0)
Serial interface internal register data clear
LCD power supply bias ratio: bias bit 0

(Refer to LCD bias select of instruction table and duty ratio by DSEL1, DSEL0 pin setting)

Duty ratio	DSEL1	DSEL0	Liquid crystal bias	
			Bias = 0	Bias = 1
1/33	0	0	1/6	1/5
1/49	0	1	1/8	1/6
1/55	1	0	1/8	1/6
1/65	1	1	1/9	1/7

On-chip oscillator OFF (while /RESET is “L”)
Power save release
Set modify-read: OFF
SHL select: OFF (normal = 0).
Static indicator mode: OFF.
Static indicator register: (S1, S0) = (0, 0)
Display start line: 0 (first)
Column address: 0.
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

When RESET instruction is issued, following procedure is occurred.

Set modify-read: OFF
Static indicator mode: OFF
Static indicator register: (S1, S0) = (0, 0)
SHL select: OFF (normal = 0)
Display start line: 0 (first)
Column address: 0
Page address: 0
Regulator resistor select register: (R2, R1, R0) = (1, 0, 0)
Reference voltage set: OFF
Reference voltage control register: (SV5, SV4, SV3, SV2, SV1, SV0) = (1, 0, 0, 0, 0, 0)
Test mode release

While /RESET is “L”, or Reset instruction is executed, no instruction except read status can be accepted. Reset status appears at DB4. After DB4 becomes “L”, any instruction can be accepted. /RESET must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by /RESET is essential before used.

7. PROGRAM INSTRUCTION DESCRIPTION

Table 7-1. Instruction table X: Don't' care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON / OFF	/RESET	0	0	0	0	Read the internal status
Display ON / OFF	0	0	1	0	1	0	1	1	1	DON	Turn ON / OFF LCD panel When DON = 0: display OFF When DON=1 : display ON
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0	Specify DDRAM line for COM0
Set reference voltage mode	0	0	1	0	0	0	0	0	0	1	Set reference voltage mode
Set reference voltage register	0	0	X	X	SV5	SV4	SV3	SV2	SV1	SV0	Set reference voltage register
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
ADC select	0	0	1	0	1	0	0	0	0	ADC	Select SEG output direction. When ADC = 0 : normal direction (SEG0 ⇒ SEG131) When ADC = 1 ; reverse direction (SEG131⇒ SEG 0)
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	Select normal / reverse display When REV = 0 : normal display When REV = 1 : reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	Select normal / entire display ON When EON = 0 : normal display When EON = 1 : entire display ON
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS	Select LCD bias
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	Release modify-read mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal function
SHL select	0	0	1	1	0	0	SHL	X	X	X	Select COM output direction When SHL = 0 : normal direction (COM0⇒ COM63) When SHL = 1 : reverse direction (COM63 ⇒ COM0)
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM	Set static indicator mode
Set static indicator register	0	0	X	X	X	X	X	X	S1	S0	Set static indicator register
Power save	-	-	-	-	-	-	-	-	-	-	Compound instruction of display OFF and entire display ON
NOP	0	0	1	1	1	0	0	0	1	1	Non-Operation command
Test Instruction_1	0	0	1	1	1	1	X	X	X	X	Don't use this instruction
Test Instruction_2	0	0	1	0	0	1	X	X	X	X	Don't use this instruction

7-1. Read display data

The 8-bit data from DDRAM specified by the column address and the page address can be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the MPU can continuously read the data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

7-2. Write display data

8-bit data of display data from the MPU can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the MPU can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

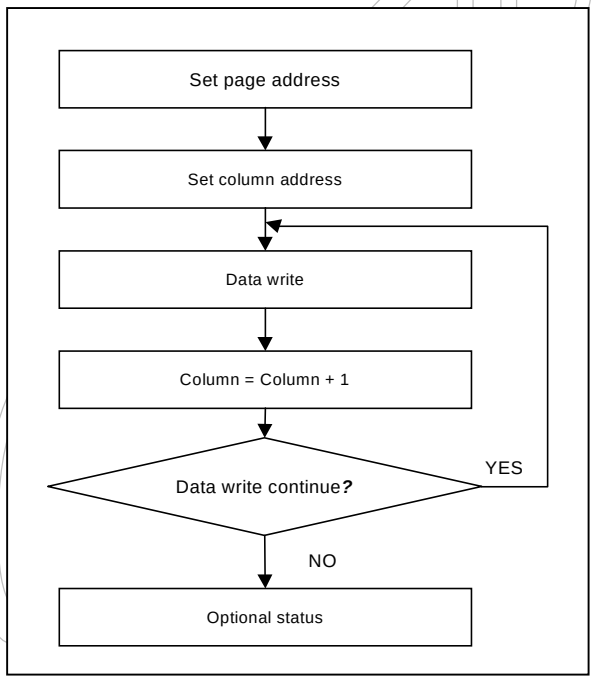

Figure 7-1. Sequence for writing display data

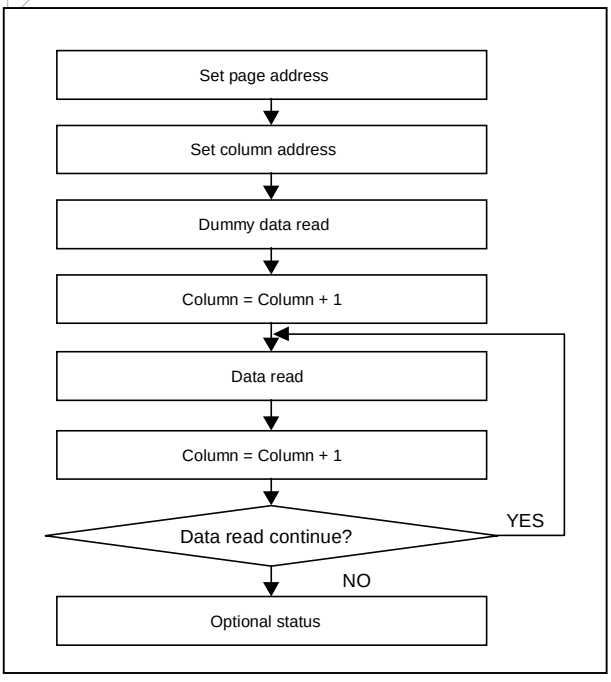

Figure 7-2. Sequence for reading display data

7-3. Read status

Indicates the internal status of the HT0324A.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON/OFF	/RESET	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset. Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG131 –>SEG0), 1: normal direction (SEG0 –>SEG131)
ON / OFF	Indicates display ON / OFF status 0: display ON, 1: display OFF
/RESET	Indicate the /RESET. 0: chip is active, 1: chip is being reset

7-4. Display ON / OFF

Turns the display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	DON

DON = 1: display ON
DON = 0: display OFF

7-5. Initial Display Line

Sets the line address of DDRAM to determine the initial display line. The RAM display data is displayed at the top row (COM0 when SHL = L, COM63 when SHL = H) of LCD panel.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

ST5	ST4	ST3	ST2	ST1	ST0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

7-6. Reference voltage select

Consists of 2-byte instruction the first instruction sets reference voltage mode, the second one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The first instruction: Set reference voltage select mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The second instruction: Set reference voltages select mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	SV5	SV4	SV3	SV2	SV1	SV0

SV5	SV4	SV3	SV2	SV1	SV0	Reference voltage parameter (α)	V0	Contrast
0	0	0	0	0	0	0	Min	Low
0	0	0	0	0	1	1	:	:
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	32 (default)	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	0	62	:	:
1	1	1	1	1	1	63	Max	High

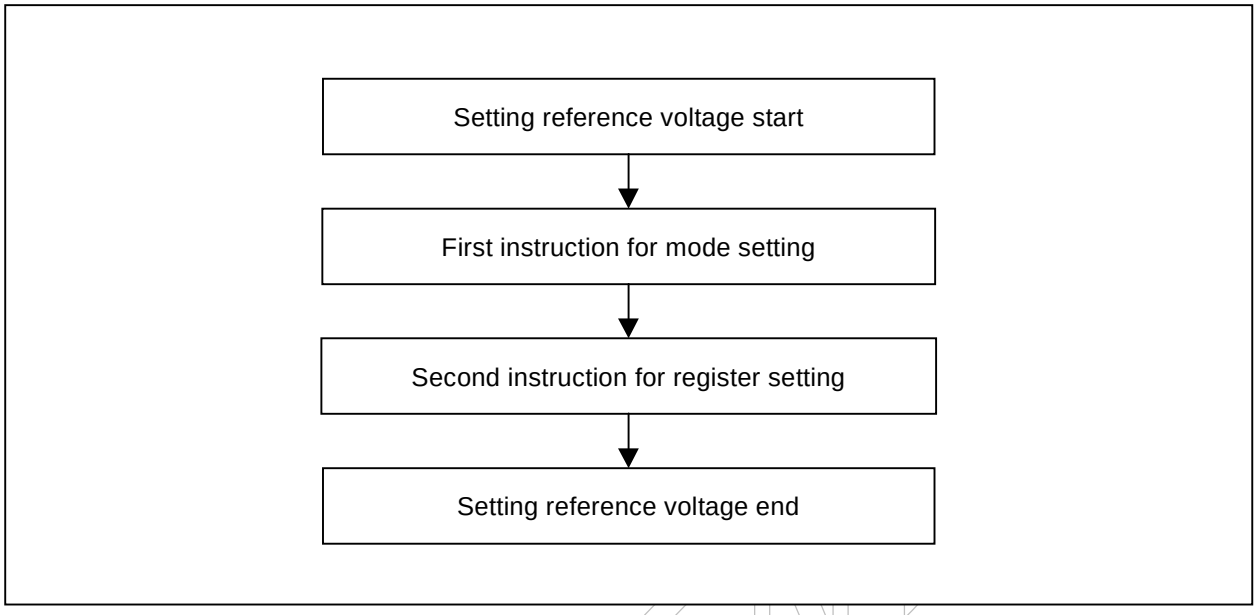

Figure 7-3. Sequence for setting the reference voltage

7-7. Set page address

Sets the page address of DDRAM from the MPU into the page address register. Any RAM data bit can be accessed when its page address and column address are specified. Along with the column address, the page address defines the address of the DDRAM to write or read display data. Changing the page address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P 3	P 2	P 1	P 0	Page
0	0	0	0	0
0	0	0	1	1
:	:	:	:	:
0	1	1	1	7
1	0	0	0	8

7-8. Set column address

Sets the column address of DDRAM from the MPU into the column address register. Along with the column address, the column address defines the address of the DDRAM to write or read display data. When the MPU reads or writes display data to or from DDRAM, column addresses are automatically increased.

Set column address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set column address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
:	:	:	:	:	:			:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

7-9. ADC select

Changes the relationship between DDRAM column address and segment driver. The direction of segment driver output pin can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 ⇒ SEG131)
ADC = 1: reverse direction (SEG131 ⇒ SEG0)

7-10. Reverse display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the DDRAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = “1”	RAM bit data = “0”
0(Normal)	Liquid crystal pixel is illuminated	Liquid crystal pixel is not illuminated
1(Reversed)	Liquid crystal pixel is not illuminated	Liquid crystal pixel is illuminated

7-11. Entire display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the DDRAM. At this time, the contents of the DDRAM are held. This instruction has priority over the reverse display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON = 0: normal display
EON = 1: entire display ON

7-12. Select LCD bias

Selects LCD bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	1	Bias

Duty ratio	DSEL1	DSEL0	Liquid crystal bias	
			Bias = 0	Bias = 1
1/33	0	0	1/6	1/5
1/49	0	1	1/8	1/6
1/55	1	0	1/8	1/6
1/65	1	1	1/9	1/7

7-13. Set modify-read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of the MPU when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

7-14. Reset modify-read

This instruction cancels the modify-read mode, and makes the column address return to its initial value just before the set modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

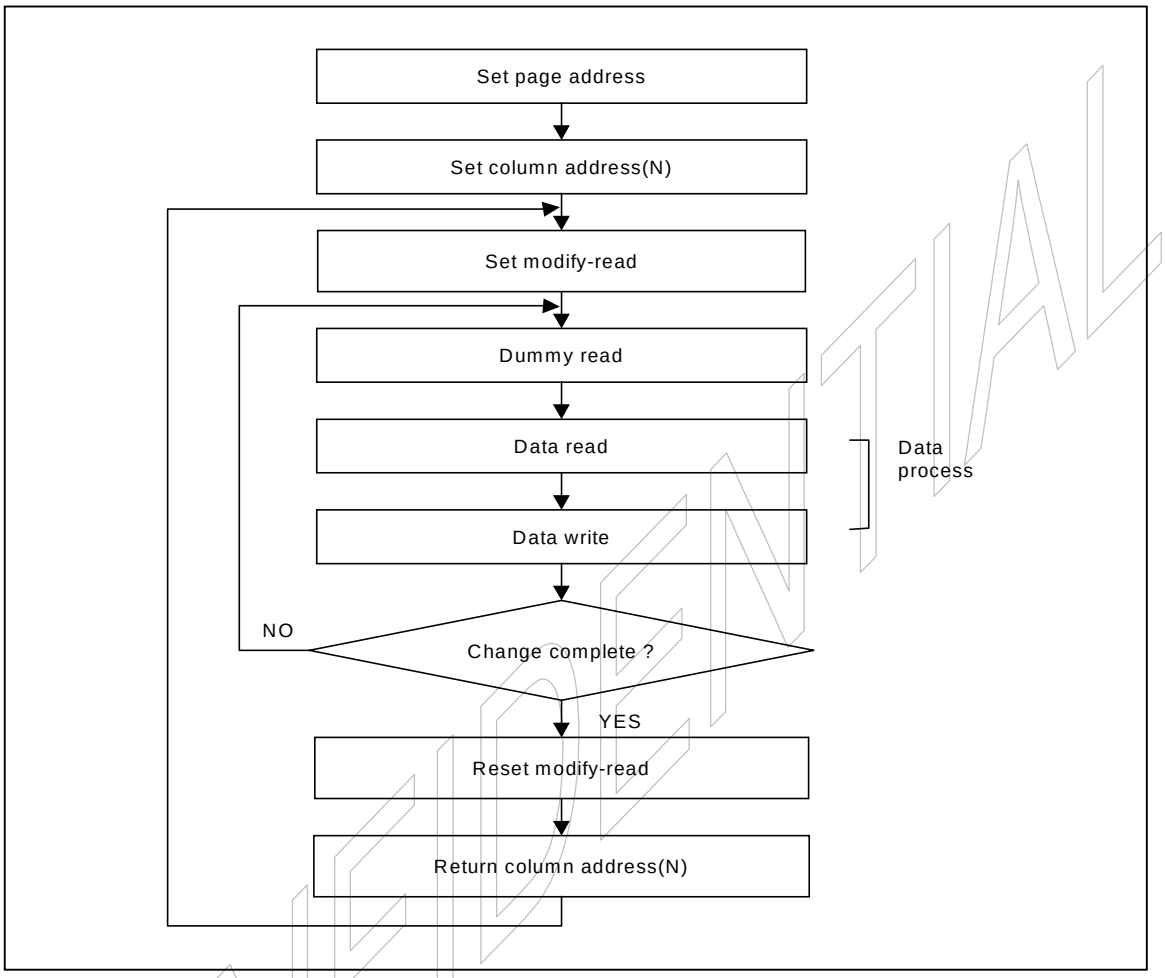

Figure 7-4. Sequence for cursor display

7-15. Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affects the contents of DDRAM. This instruction can not initialize the LCD power supply which is initialized by the /RESET pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

7-16. SHL select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	X	X	X

SHL = 0: normal direction (COM0 ⇒ COM63) X : Don't care
SHL = 1: reverse direction (COM63 ⇒ COM0)

7-17. Power control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Internal power supply circuits status
0 1			Voltage converter circuit is OFF Voltage converter circuit is ON
	0 1		Voltage regulator circuit is OFF Voltage regulator circuit is ON
		0 1	Voltage follower circuit is OFF Voltage Follower circuit is ON

7-18. Regulator resistor select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 6-9.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	(1 + Rb / Ra) ratio
0	0	0	3.0
0	0	1	3.5
0	1	0	4.0
0	1	1	4.5
1	0	0	5.0 (default)
1	0	1	5.5
1	1	0	6.0
1	1	1	6.4

7-19. Set static indicator state

Consists of two bytes instruction. The first byte instruction (set static indicator mode) enables the second byte instruction (set static indicator register) to be valid. The first byte sets the static indicator ON / OFF. When it is ON, the second byte updates the contents of static indicator register without issuing any other instruction and this static indicator state is released after setting the data of indicator register.

The first instruction: Set static indicator mode (ON / OFF)

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	0	SM

SM = 0: static indicator OFF
SM = 1: static indicator ON

The second instruction: Set static indicator register

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	X	X	X	X	X	X	S1	S0

S1	S0	Static indicator output status
0	0	OFF
0	1	ON (about 1 second blinking)
1	0	ON (about 0.5 second blinking)
1	1	ON (always ON)

7-20. NOP

Non Operation Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

7-21. Test Instruction (Test Instruction_1 & Test Instruction_2)

These are the instruction for IC chip testing. Please do not use it. If the Test Instruction is used by accident, it can be cleared by applying “0” signal to the /RESET input pin or the reset instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	X	X	X	X

0	0	1	0	0	1	X	X	X	X

7-22. Power save (Compound instruction).

If the entire display ON / OFF instruction is issued during the display OFF state, HT0324A enters the power save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, power save is entered to one of two modes (sleep and standby mode). When static indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued. Power save mode is released by the display OFF instruction.

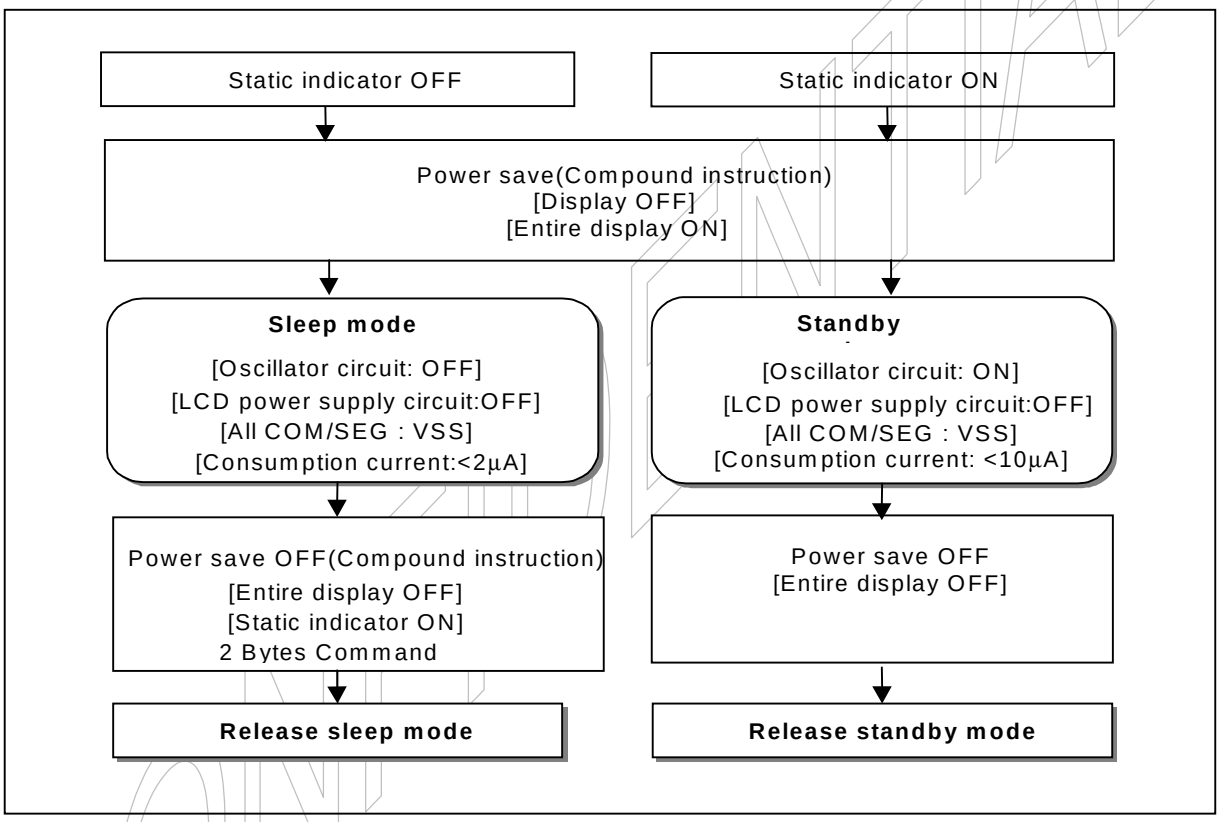

Figure 7-5. Power save routine

-Sleep Mode

This stops all operations in the LCD display system, and as long as there are no access from the MPU, the consumption current is reduced to a value near the static current. The internal modes during sleep mode are as follows:

a. The oscillator circuit and the LCD power supply circuit are halted.
b. All liquid crystal drive circuits are halted, and the segment in common drive outputs output a VSS level.

-Standby Mode

The duty LCD display system operations are halted and only the static drive system for the indicator continues to operate, providing the minimum required consumption current for the static drive.
The internal modes are in the following states during standby mode.

a. The LCD power supply circuits are halted. The oscillator circuit continues to operate.
b. The duty drive system liquid crystal drive circuits are halted and the segment and common drive outputs

a VSS level. When a reset command is performed while in standby mode, the system enters sleep mode.

7-23. Referential instruction setup flow (1)

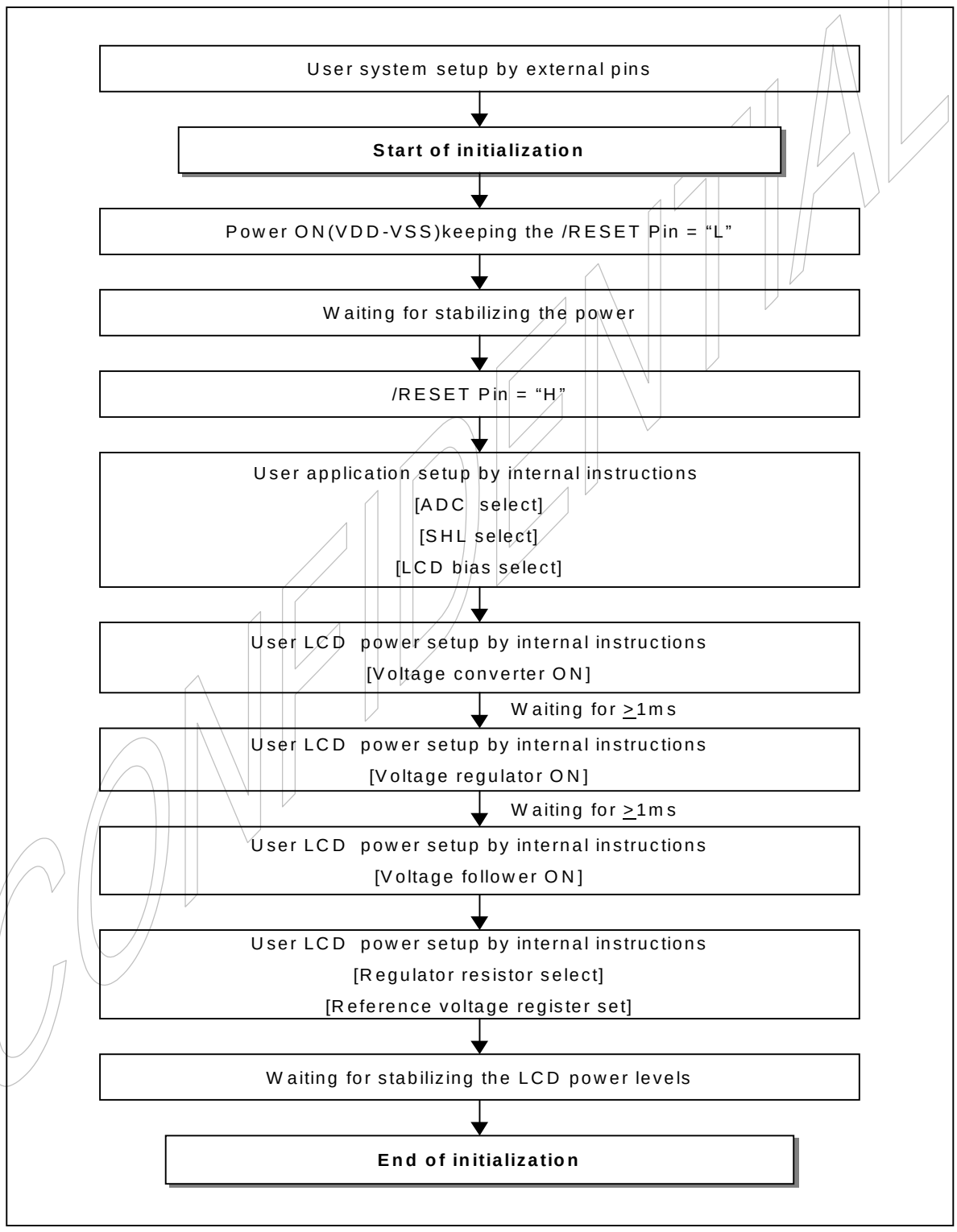

Figure 7-6. Initializing with the built-in power supply circuits

Referential instruction setup flow (2)

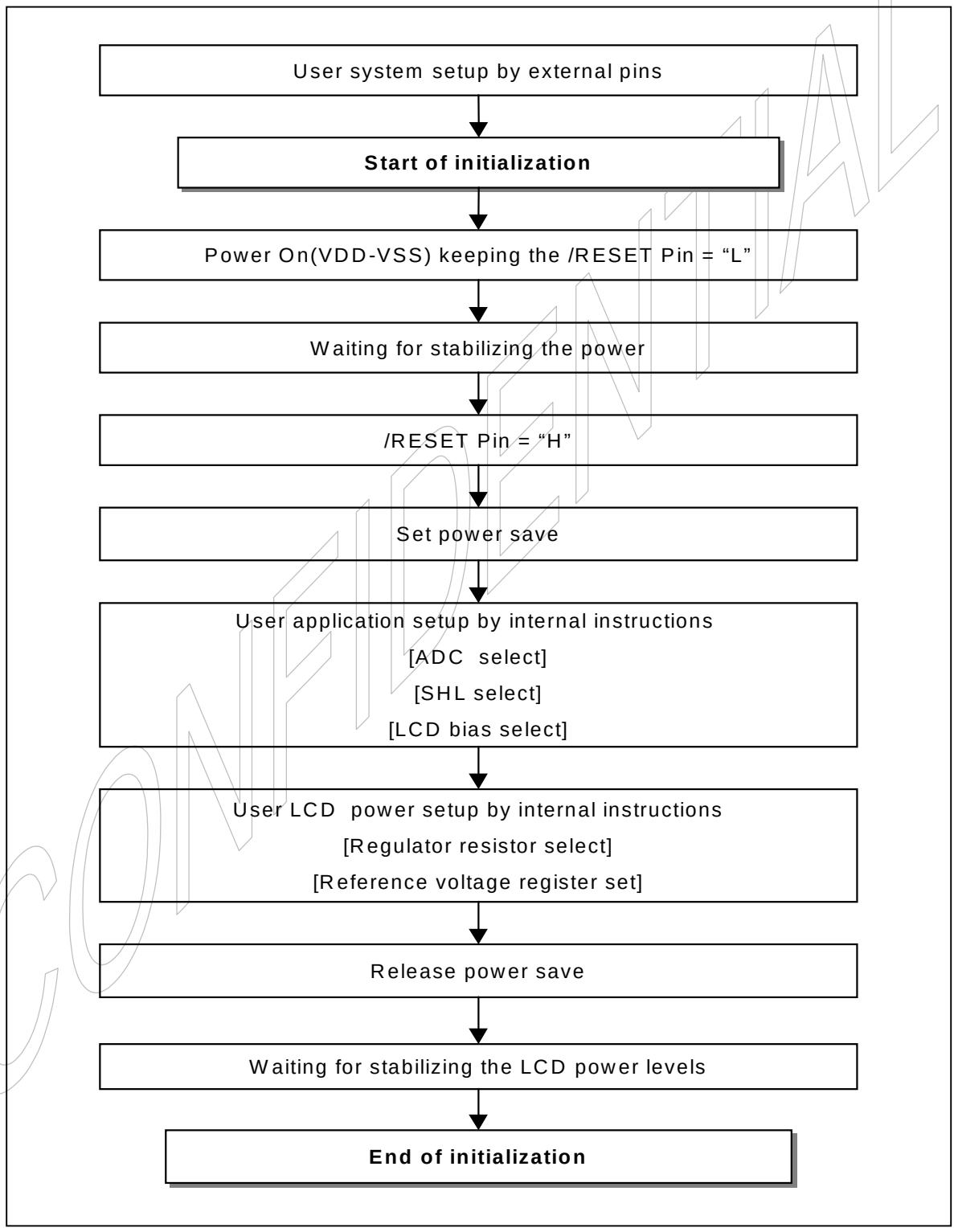

Figure 7-7. Initializing without the built -in power supply circuits

Referential Instruction Setup Flow (3)

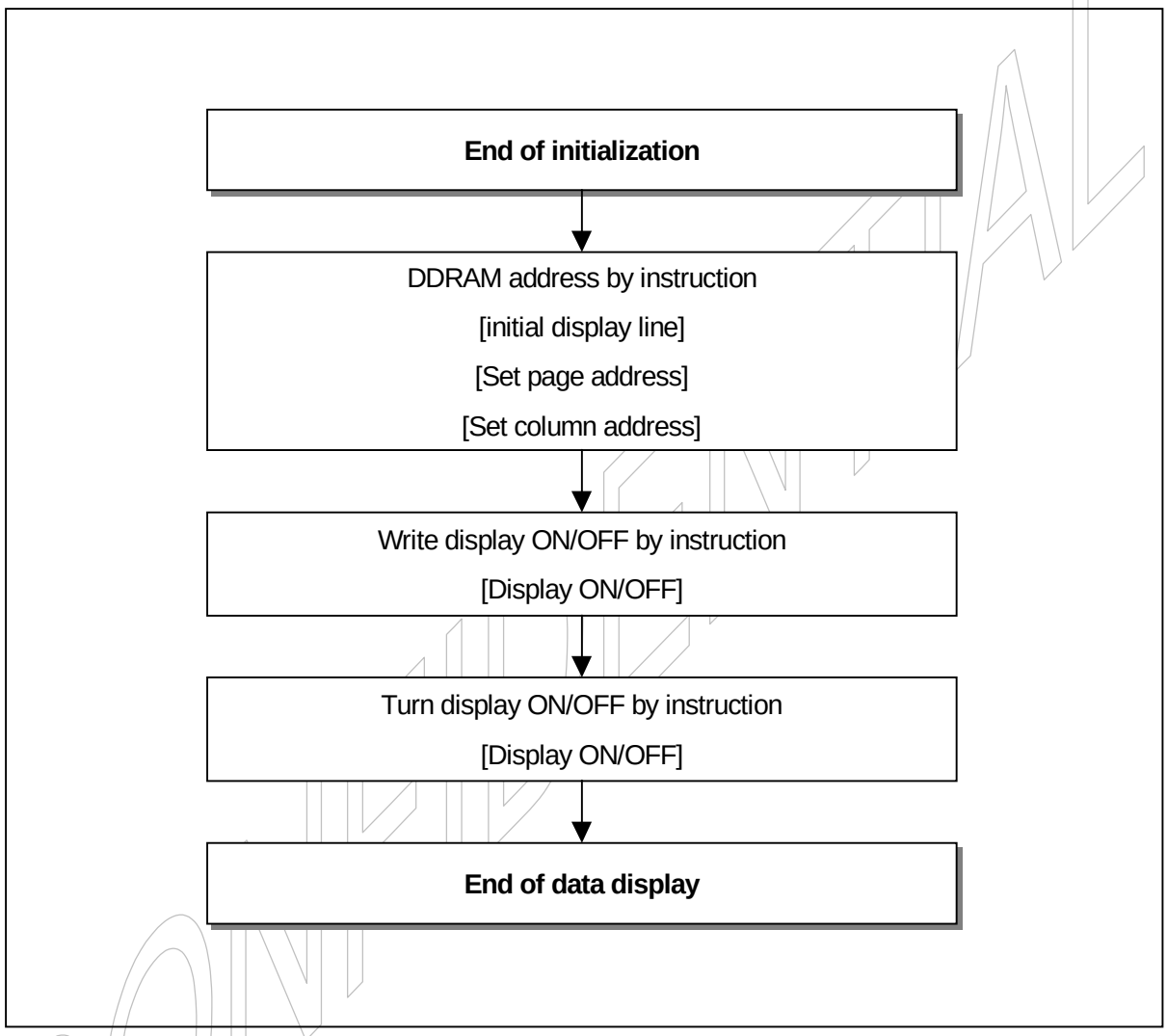

Figure 7-8. Data display

Referential instruction setup flow (4)

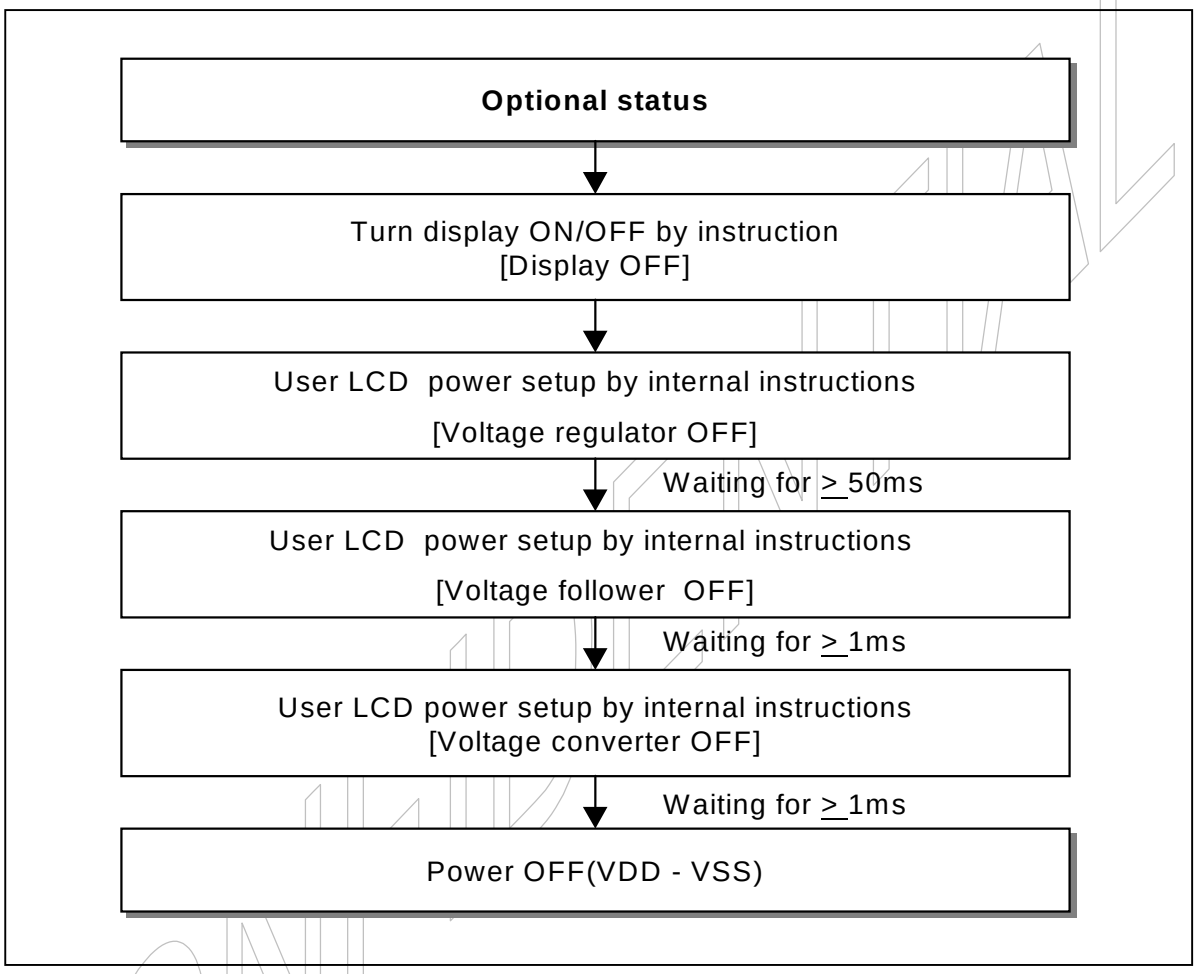

Figure 7-9. Power off.

8. SPECIFICATIONS

8-1. Absolute maximum ratings

Table 8-1. Absolute maximum ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	-0.3 to +7.0	V
	V_{LCD}	-0.3 to +17.0	
Input voltage range	V_{IN}	-0.3 to V_{DD} +0.3	
Operating temperature range	T_{OPR}	-40 to +85	^{o}C
Storage temperature range	T_{STR}	-55 to +125	

Notes:
1. VDD and VLCD are based on VSS = 0V.
2. Voltages V0 ≥V1≥V2≥V3≥V4≥VSS(GND) must always be satisfied.(VLCD = V0 - VSS)
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

8-2. DC Characteristics

Table 8-2. DC characteristics (VSS = 0V, VDD = 2.4V to 5.5V, Ta = -40 to +85^{o}C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Pin Used
Operating voltage(1)		V_{DD}		2.4	-	5.5	V	VDD *1
Operating voltage(2)		V0		4.5	-	15.0		V0 *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}		*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH}=-0.5mA	0.8V_{DD}	-	V_{DD}		*4
	Low	V_{OL}	I_{OL}=0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN}=VDD or VSS	-1.0	-	+1.0	μA	*5
Output leakage current		I_{OZ}	V_{IN}=VDD or VSS	-3.0	-	+3.0		*6
LCD driver ON resistance		R_{ON}	Ta = 25 ^{o}C V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *7
Oscillator frequency	Internal	f_{OSC}	Ta = 25 ^{o}C Duty ratio = 1/65	32.7	43.6	54.5	kHz	CL*8
	External	f_{CL}		4.09	5.45	6.81		

Table 8-2. DC characteristics (continued)) (VSS = 0V, VDD = 2.4V to 5.5V, Ta = -40 to +85°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Voltage converter input voltage	VCI	x 2	2.4	-	5.5	V	VCI
		x 3	2.4		5.3		
		x 4	2.4		4.0		
		x 5	2.4		3.2		
Voltage converter output voltage	VOUT	x 2 / x 3 / x 4 / x 5 voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator operating voltage	VOUT	-	6.0	-	16.0	V	VOUT
Voltage follower operating voltage	V0	-	4.5	-	15.0		V0*9
Reference voltage	VREF	Ta = 25 °C -0.05%/ °C	2.04	2.1	2.16		*10

Table 8-2. DC Characteristics (Continued) (VSS = 0V, VDD = 2.4V to 5.5V, Ta = -40 to +85°C)

Dynamic current consumption (1): Built-in circuit OFF (At operating mode)							
Dynamic current consumption (1)	IDD1	VDD = 3.0V, V0 – VSS= 11.0V, 1/65 duty ratio, display pattern OFF	-	15	23	µA	*11
Dynamic Current Consumption (2): Built-in circuit ON (At operating mode)							
Dynamic current consumption (2)	IDD2	VDD = 3.0V, (VCI=VDD,4times boosting) V0 – VSS= 11.0V, 1/65 duty ratio, display pattern OFF, normal power mode	-	40	60	µA	*12
		VDD = 3.0V, (VCI=VDD, 4 times boosting) V0 – VSS= 11.0V, 1/65 duty ratio, display pattern check, normal power mode	-	150	200	µA	*12
Current consumption during power save mode							
Sleep mode current	IDDS1	During sleep	-	-	2.0	µA	

Standby mode current	IDDS2	During standby			10.0	μA	

Table 8-3. The relationship between oscillation frequency and frame frequency

Duty ratio	Item	f_{CL}	f_{FR}
1/65	On-chip oscillator circuit is used	f_{OSC} / 8	f_{OSC} / (2 x 8 x 65)
	External clock is used	External Input(f_{CL})	f_{CL} / (2 x 65)
1/55	On-chip oscillator circuit is used	**F**osc / 9	**F**osc / (2 x 9 x 55)
	External clock is used	External input (f_{CL})	f_{CL} / (2 x 55)
1/49	On-chip oscillator circuit is used	f_{OSC} / 10	f_{OSC} / (2 x 10 x 49)
	External clock is used	External Input (f_{CL})	f_{CL} / (2 x 49)
1/33	On-chip oscillator circuit is used	f_{OSC} / 15	f_{OSC} / (2 x 15 x 33)
	External clock is used	External Input (f_{CL})	f_{CL} / (2 x 33)

*(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: LCD AC signal frequency)

<* Remark solves>

*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU
*2. In case of external power supply is applied.
*3. /CS1, CS2, RS, DB7 to DB0, E_/RD, RW_/RW, /RESET, MS, C68, PS, INTRS, /HPM, CLS, CL, M, DISP pins.
*4. DB0 to DB7, M, FR, FRS, DISP, CL pin.
*5. /CS1, CS2, RS, DB7 to DB0, E_/RD, RW_/WR, /RESET, MS, C68, PS, INTRS, /HPM, CLS, CL, M, DISP pins.
*6. Applies when then DB7 to DB0, M, FR, FRS, DISP, and CL, pins are in high impedance.
*7. Resistance value when ±0.1[mA] is applied during the ON status of the output pin SEGn or COMn.
RON = ΔV / 0.1[kΩ] (ΔV :Voltage change when ±0.1[mA]is applied in the on status)
*8. See table 8-3 for the relationship between oscillation frequency and frame frequency.
*9. The Voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
*10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*11, 12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built -in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD penal capacity, wiring capacity, etc.

8-3. AC CHARACTERISTICS

a. Read / write characteristics (8080-series MPU)

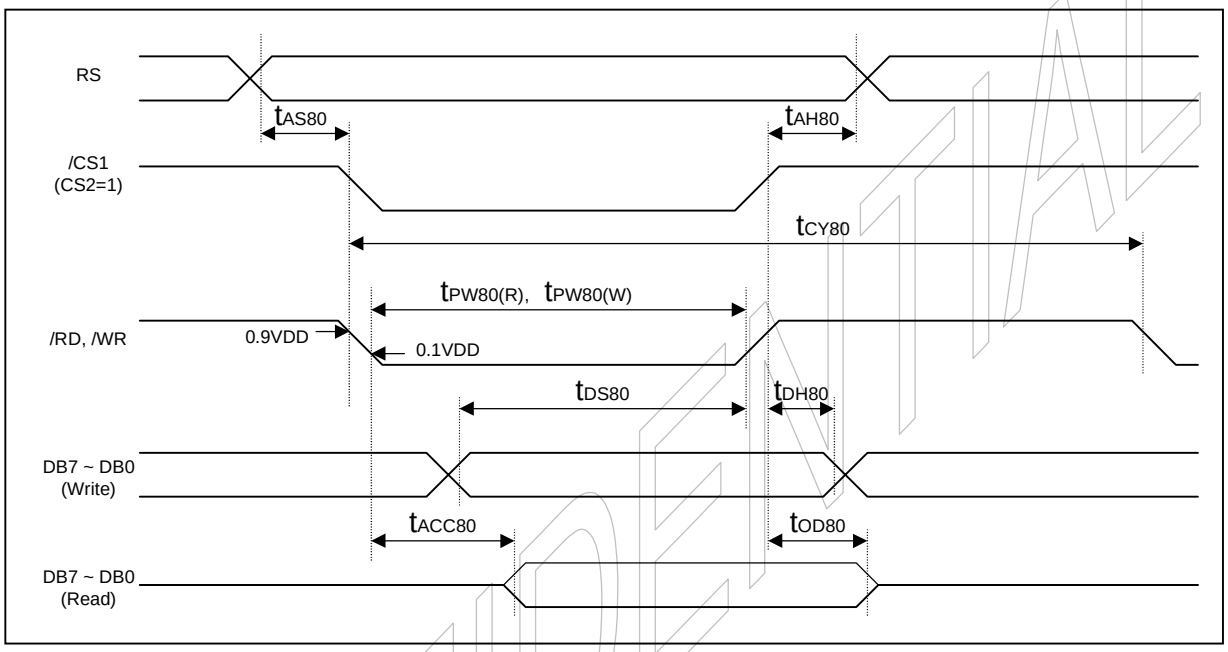

Figure 8-4. Read / write timing chart (8080-series MPU)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time	RS	t_{CY80}	300	-	-	ns	
Pulse width(/WR)	RW-/WR	t_{PW80} (W)	60	-	-	ns	
Pulse width(/RD)	E-/RD	t_{PW80} (R)	60	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	40 15	-	-	ns	
Read access time Output disable time		t_{ACC80} t_{OD80}	- 10	-	140 100	ns	CL = 100pF

(VDD = 3.6 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time	RS	t_{AS80} t_{AH80}	0 0	-	-	ns	
System cycle time	RS	t_{CY80}	166	-	-	ns	
Pulse width(/WR)	RW-/WR	t_{PW80} (W)	30	-	-	ns	
Pulse width(/RD)	E-/RD	t_{PW80} (R)	30	-	-	ns	
Data setup time Data hold time	DB7 to DB0	t_{DS80} t_{DH80}	30 10	-	-	ns	

Read access time Output disable time		$t_{ACC}80$ $t_{OD}80$	- 5	-	70 50	ns	CL = 100pF

b. Read / write characteristics (6800-series MPU)

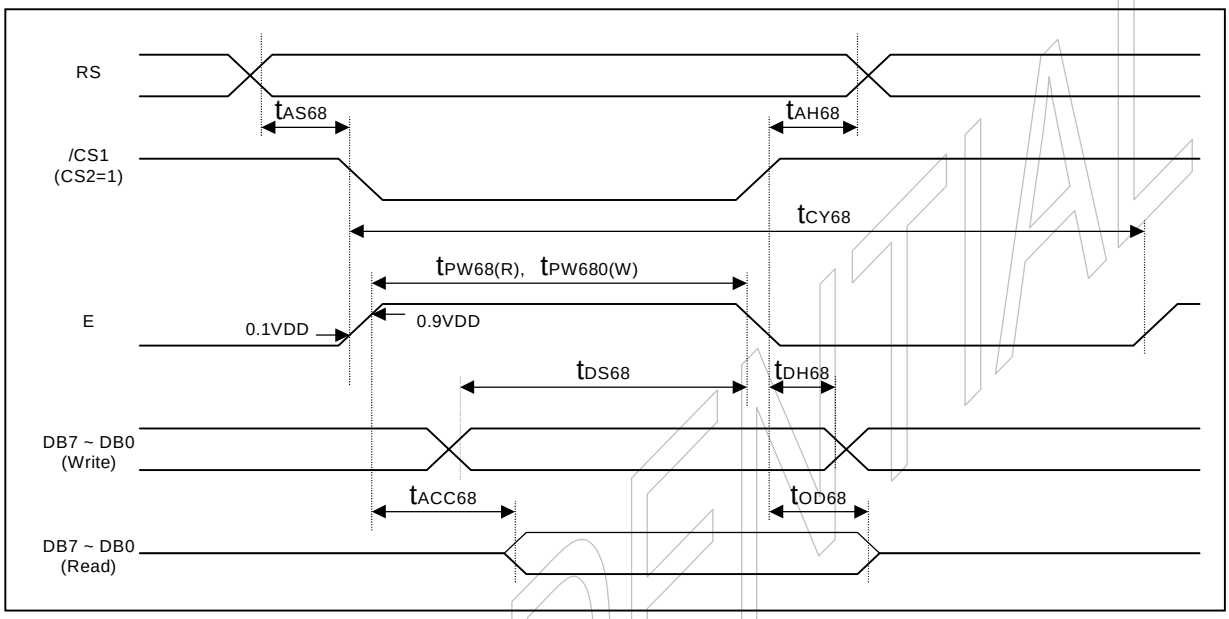

Figure 8-5. Read / write timing chart (6800-series MPU)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	$t_{AS}68$ $t_{AH}68$	0 0	-	-	ns	
System cycle time		RS	$t_{AH}68$	300	-	-	ns	
Enable pulse width	Read Write	E-/RD	$t_{PW}68$ (R) $t_{PW}68$ (W)	120 60	-	-	-	
Data setup time Data hold time		DB7 to DB0	$t_{DS}68$ $t_{DH}68$	40 15	-	-	ns	
Access time Output disable time			$T_{ACC}68$ $t_{OD}68$	- 10	-	140 100	ns	CL = 100pF

(VDD = 3.6 to 5.5V, Ta = -40 to +85°C)

Item		Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Address setup time Address hold time		RS	$t_{AS}68$ $t_{AH}68$	0 0	-	-	ns	
System cycle time		RS	$t_{AH}68$	166	-	-	ns	
Enable pulse width	Read Write	E-/RD	$t_{PW}68$ (R) $t_{PW}68$ (W)	70 30	-	-	-	
Data setup time Data hold time		DB7 to DB0	$t_{DS}68$ $t_{DH}68$	30 10	-	-	ns	
Access time Output disable time			$T_{ACC}68$ $t_{OD}68$	- 10	-	70 50	ns	CL = 100pF

c. Serial interface characteristics

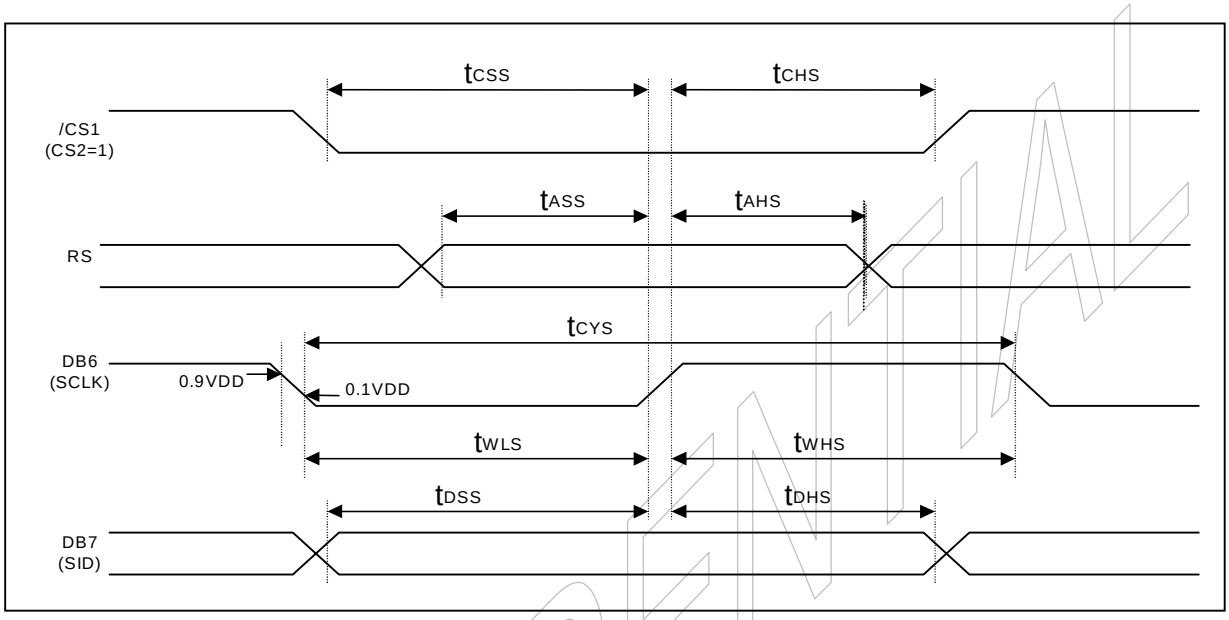

Figure 8-6. Serial interface characteristics

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYC} t_{WHS} t_{WLS}	250 100 100	-	-	ns	
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	150 150	-	-	ns	
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	100 100	-	-	ns	
/CS1 set up time /CS1 hold time	/CS1	t_{CSS} t_{CHS}	150 150	-	-	ns	

(VDD = 3.6 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{CYC} t_{WHS} t_{WLS}	200 75 75	-	-	ns	
Address setup time Address hold time	RS	t_{ASS} t_{AHS}	50 100	-	-	ns	
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}	50 50	-	-	ns	
/CS1 set up time /CS1 hold time	/CS1	t_{CSS} t_{CHS}	100 100	-	-	ns	

d. Reset input timing

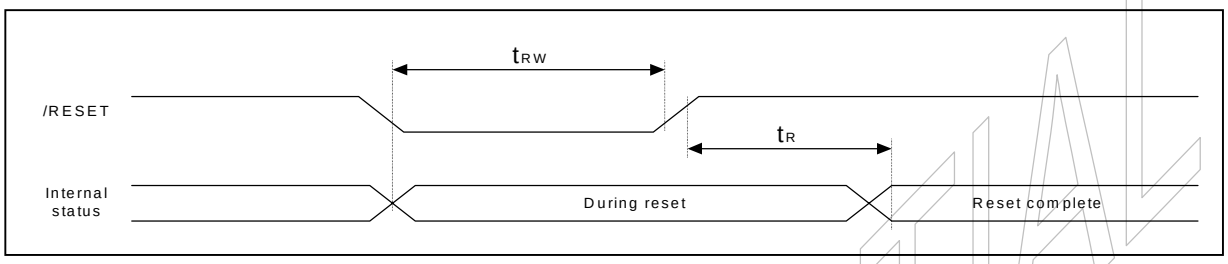

Figure 8-7. Reset input timing

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	/RESET	t_{RW}	1.0	-	-	µs	
Reset time	-	t_R	-	-	1.0	µs	

(VDD = 3.6 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
Reset low pulse width	/RESET	t_{RW}	0.5	-	-	µs	
Reset time	-	t_R	-	-	0.5	µs	

e. Display control output timing

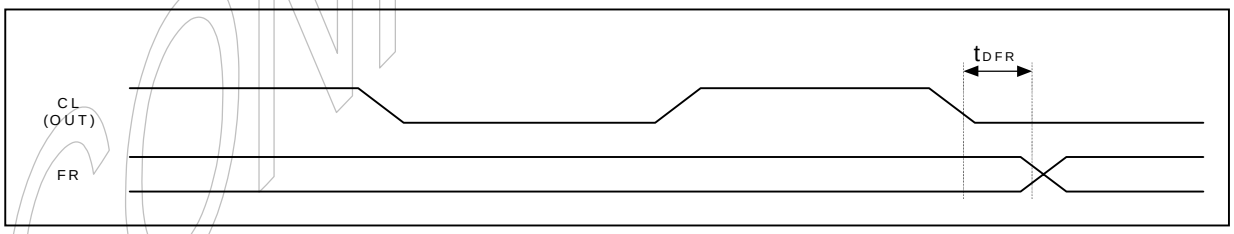

Figure 8-8. Display control output timing

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	t_{DFR}	-	20	80	ns	C_L = 50 pF

(VDD = 3.6 to 5.5V, Ta = -40 to +85°C)

Item	Signal	Symbol	Min.	Typ.	Max.	Unit	Remark
FR delay time	FR	t_{DFR}	-	10	40	ns	CL = 50 pF

9. REFERENCE APPLICATION

9-1. Microprocessor interface

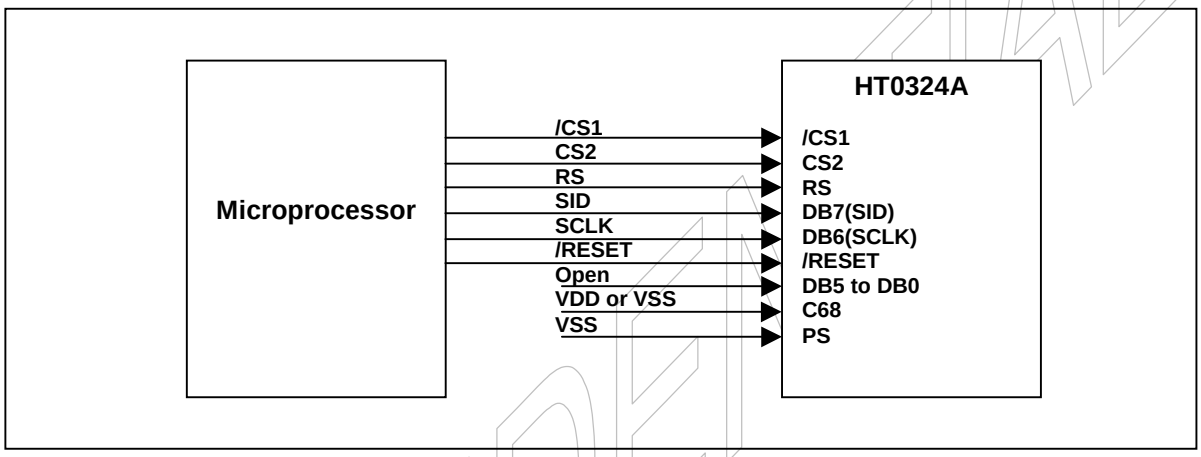

Figure 9-1. Serial Interface (PS = "L", C68 = " H or L", E_/RD = "H or L", RW_/WR = "H or L")

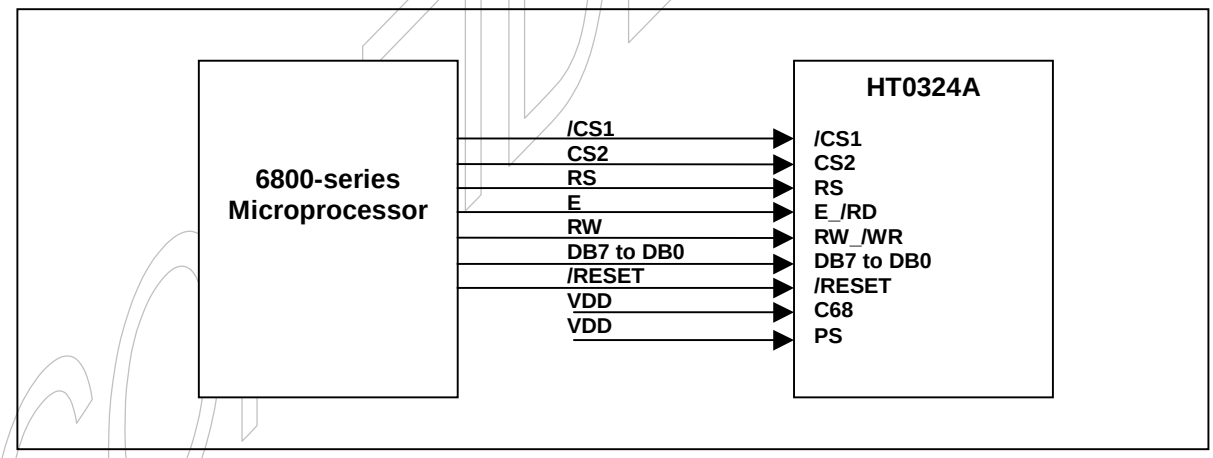

Figure 9-2. 6800-series MPU Interface (PS = "H", C68 = " H")

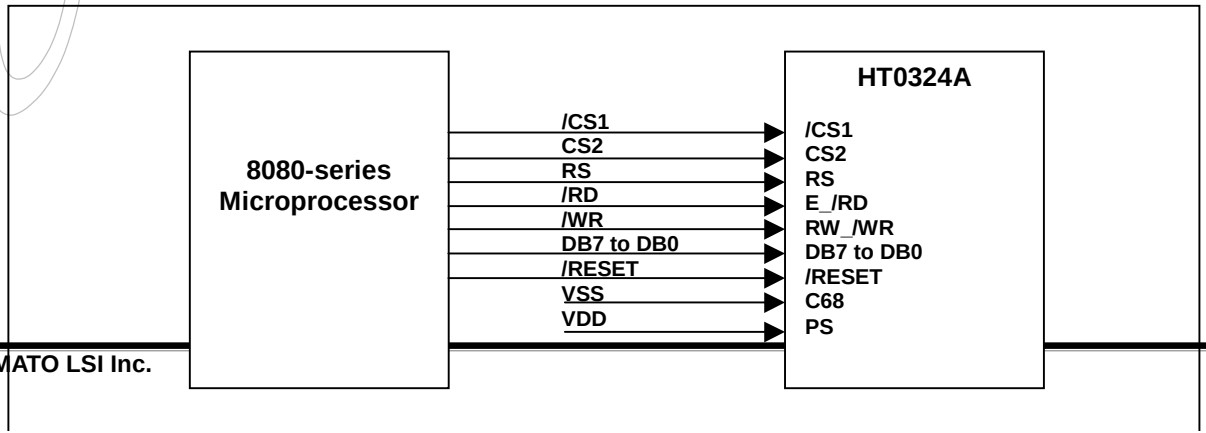

Figure 9-3. 8080-series MPU Interface (PS = "H", C68 = " L")

9-2. CONNECTIONS BETWEEN HT0324A AND LCD PANEL

a. Single chip configuration (1/65 duty configurations)

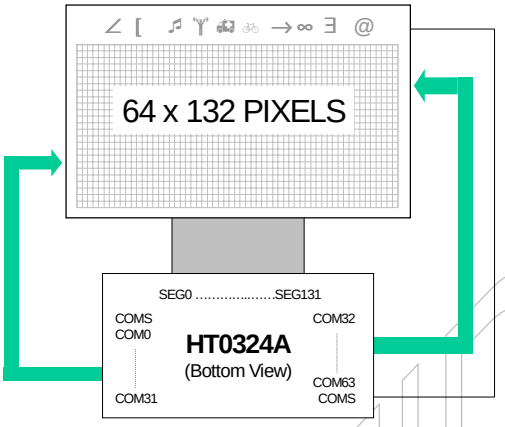

Figure 9-4. SHL = 1, ADC = 0

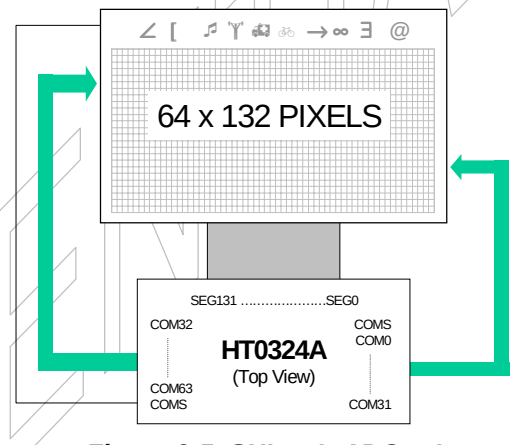

Figure 9-5. SHL = 1, ADC = 1

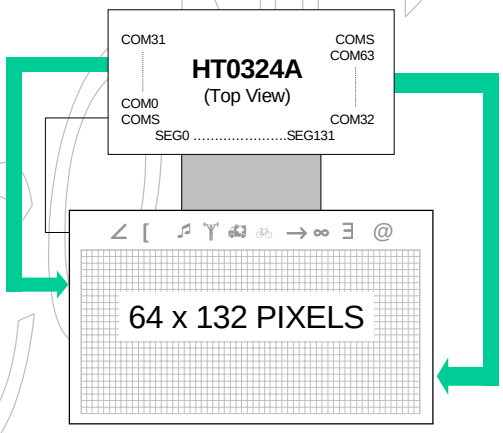

Figure 9-6. SHL = 0, ADC = 0

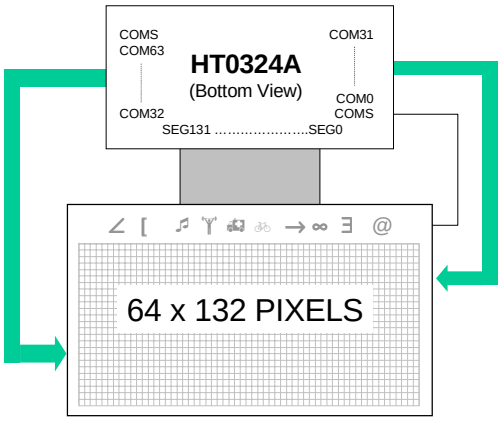

Figure 9-7. SHL = 0, ADC = 1

b. Single chip configuration (1/55 duty configurations)

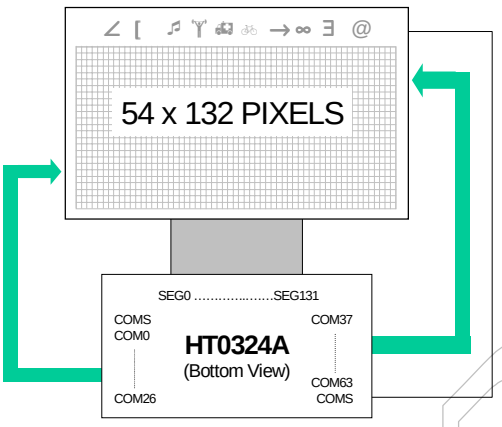

Figure 9-8. SHL = 1, ADC = 0

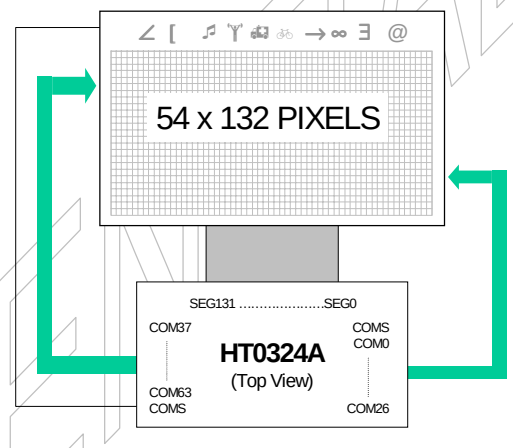

Figure 9-9. SHL = 1, ADC = 1

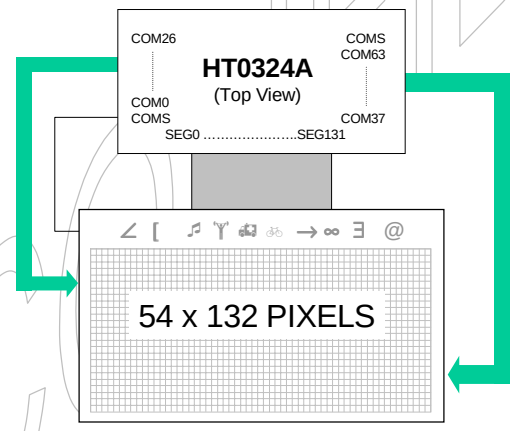

Figure 9-10. SHL = 0, ADC = 0

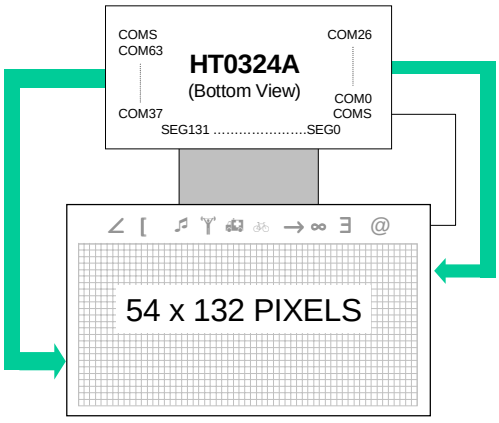

Figure 9-11. SHL = 0, ADC = 1

c. Single chip configuration (1/49 duty configurations)

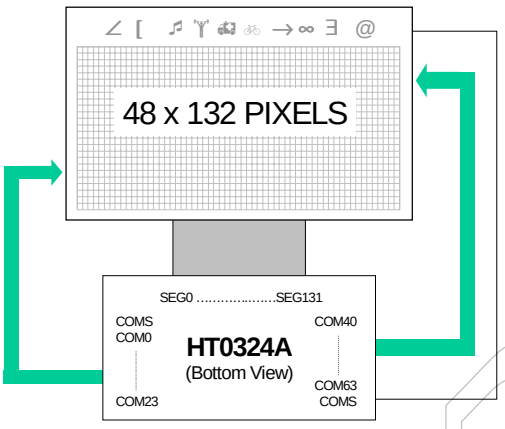

Figure 9-12. SHL = 1, ADC = 0

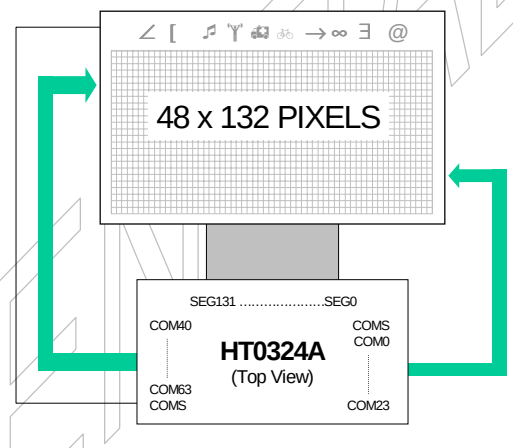

Figure 9-13. SHL = 1, ADC = 1

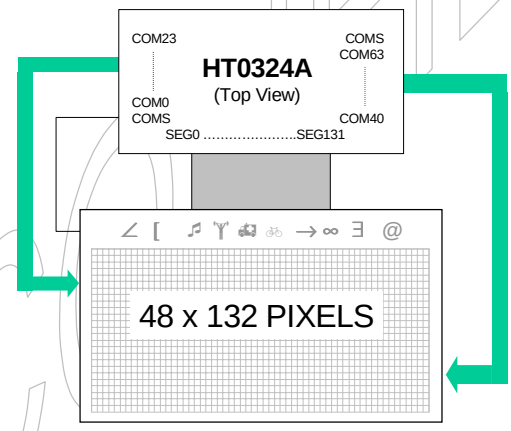

Figure 9-14. SHL = 0, ADC = 0

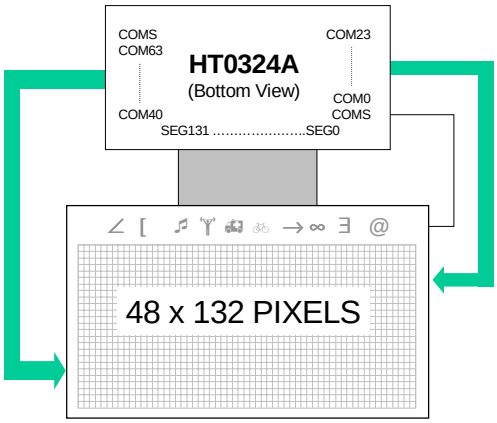

Figure 9-15. SHL = 0, ADC = 1

d. Single chip configuration (1/33 duty configurations)

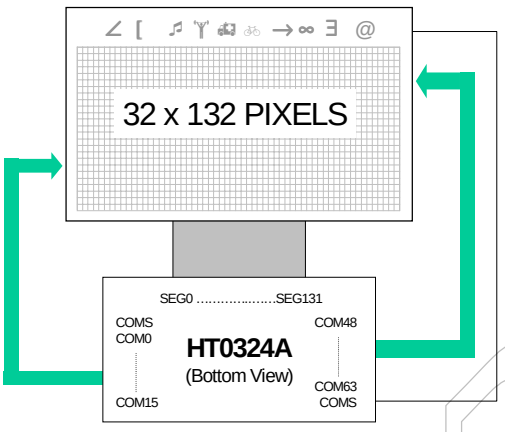

Figure 9-16. SHL = 1, ADC = 0

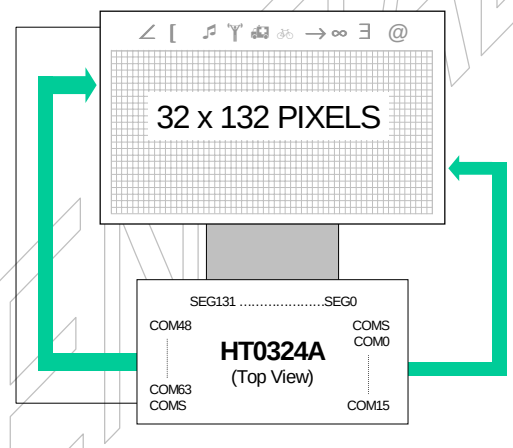

Figure 9-17. SHL = 1, ADC = 1

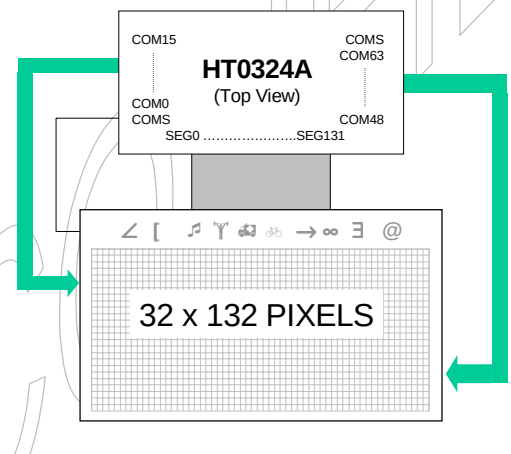

Figure 9-18. SHL = 0, ADC = 0

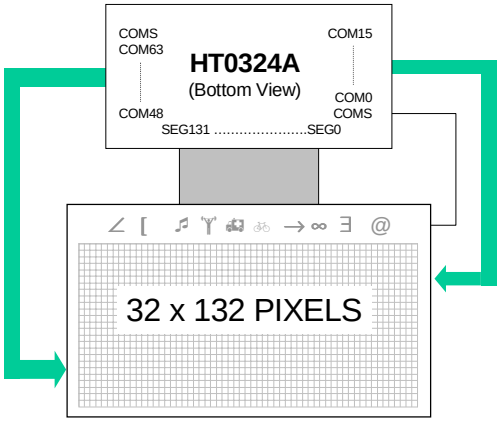

Figure 9-19. SHL = 0, ADC = 1

e. Multiple chip configuration

- 65COM (64COM + 1COMS) x 264SEG (132SEG x 2)

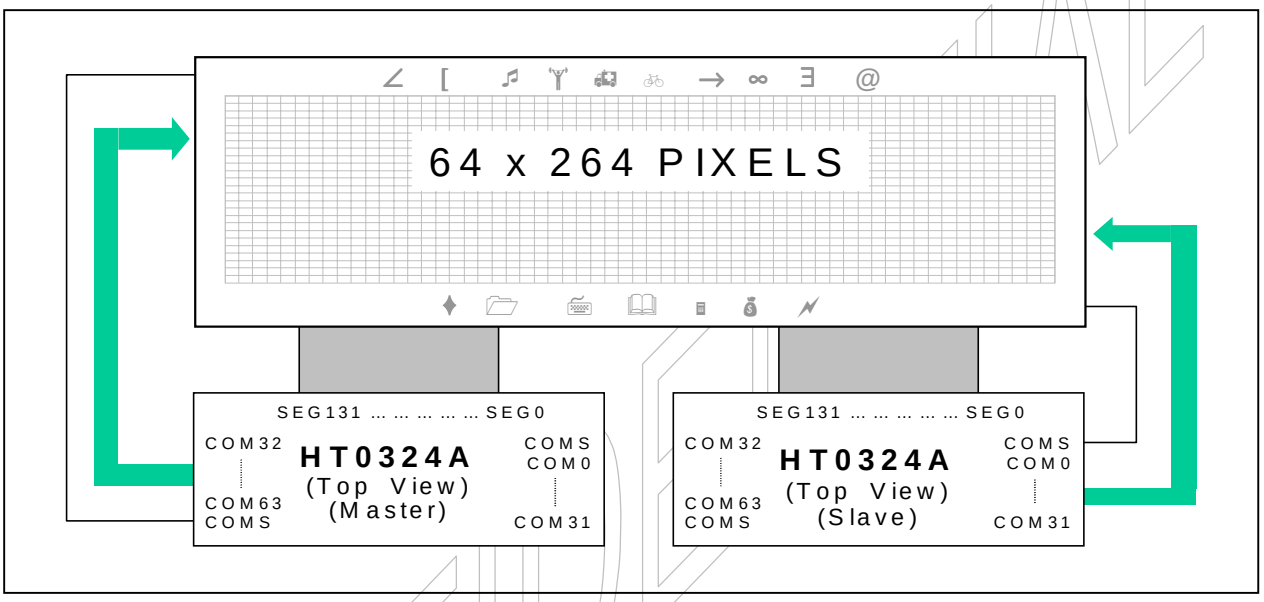

Figure 9-20. SHL = 1, ADC = 1

∗ Connect the following pins of two chips each other
- Display clock pins: CL, M
- Display control pin: DISP
- LCD power pins: V0, V1, V2, V3, V4

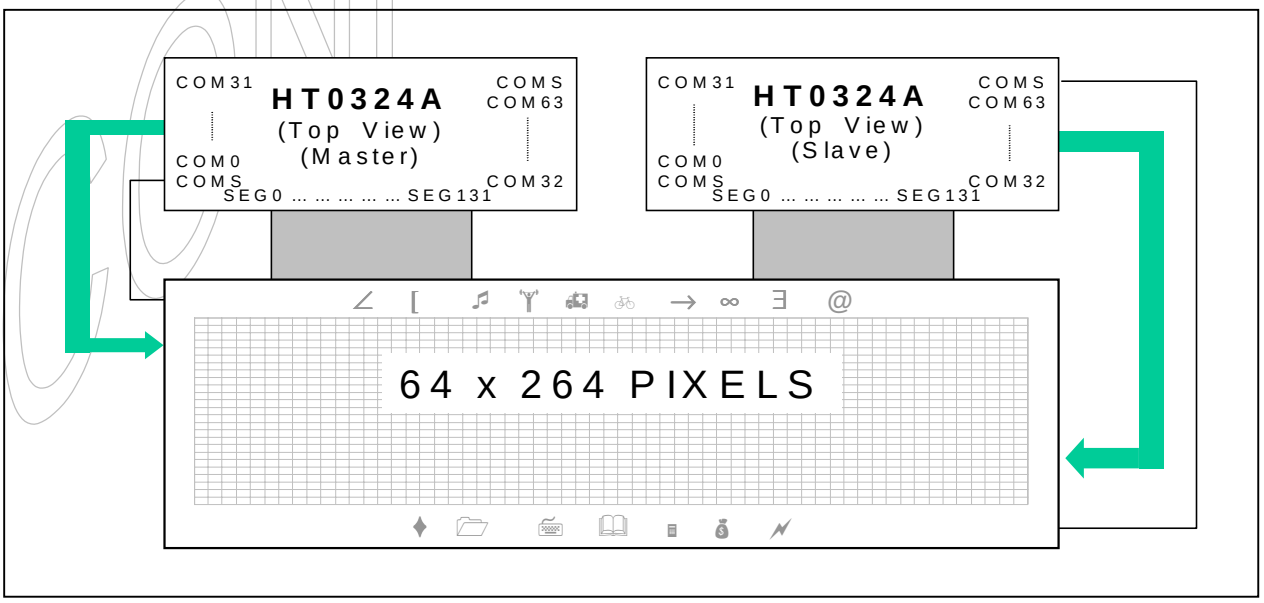

Figure 9-21. SHL = 0, ADC = 0

∗ Connect the following pins of two chips each other
- Display clock pins: CL, M
- Display control pin: DISP
- LCD power pins: V0, V1, V2, V3, V4

- **130COM (128COM + 2COMS) x 132SEG**

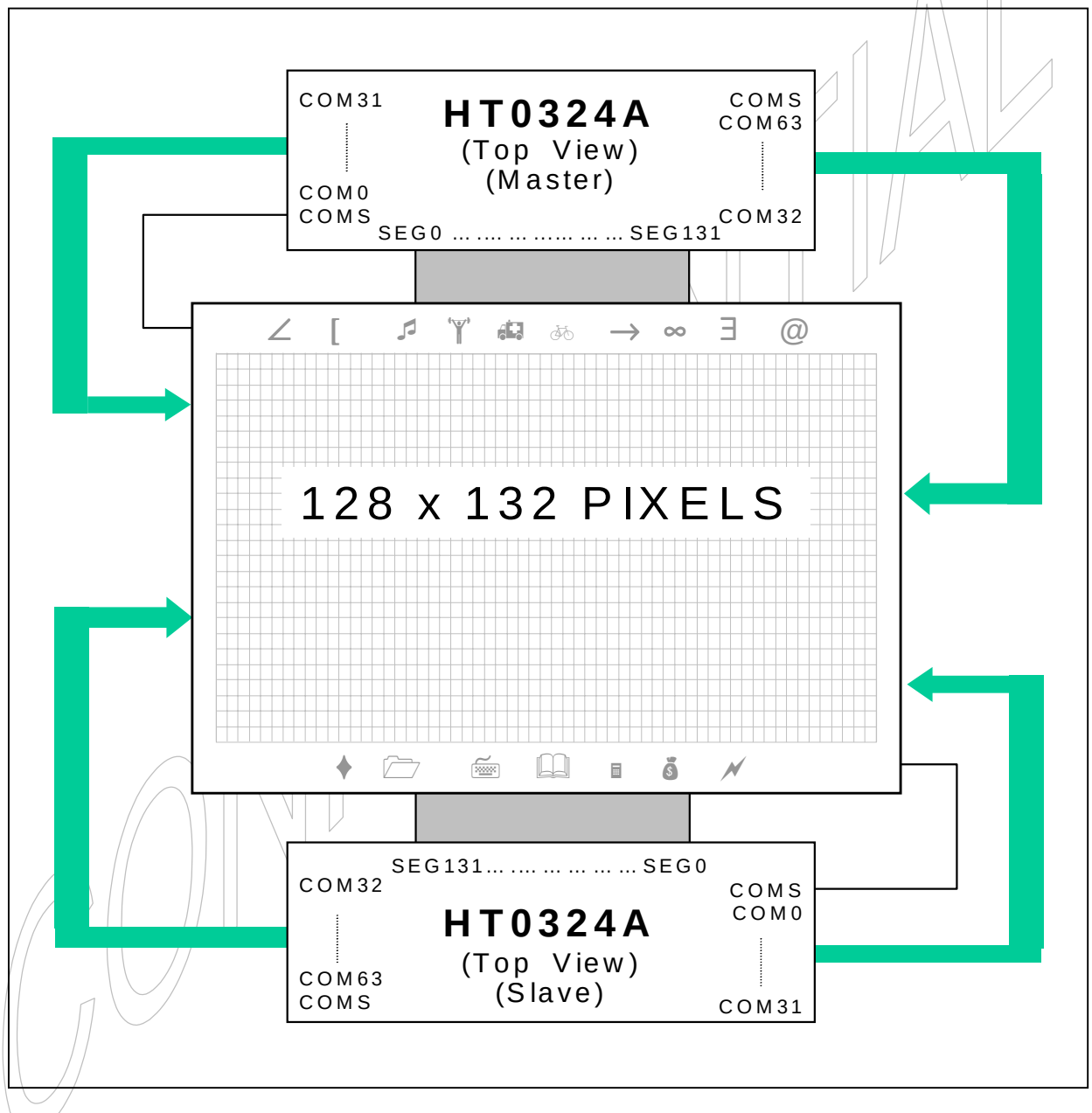

Figure 9-21. 130COM (128COM + 2COMS) x 132SEG

∗ Connect the following pins of two chips each other
- Display clock pins: CL, M
- Display control pin: DISP
- LCD power pins: V0, V1, V2, V3, V4

* Common / Segment output direction select
  - Master chip: SHL = 0, ADC = 0
  - Slave chip: SHL = 1, ADC = 1

9-3. TCP Pin lay out (sample)

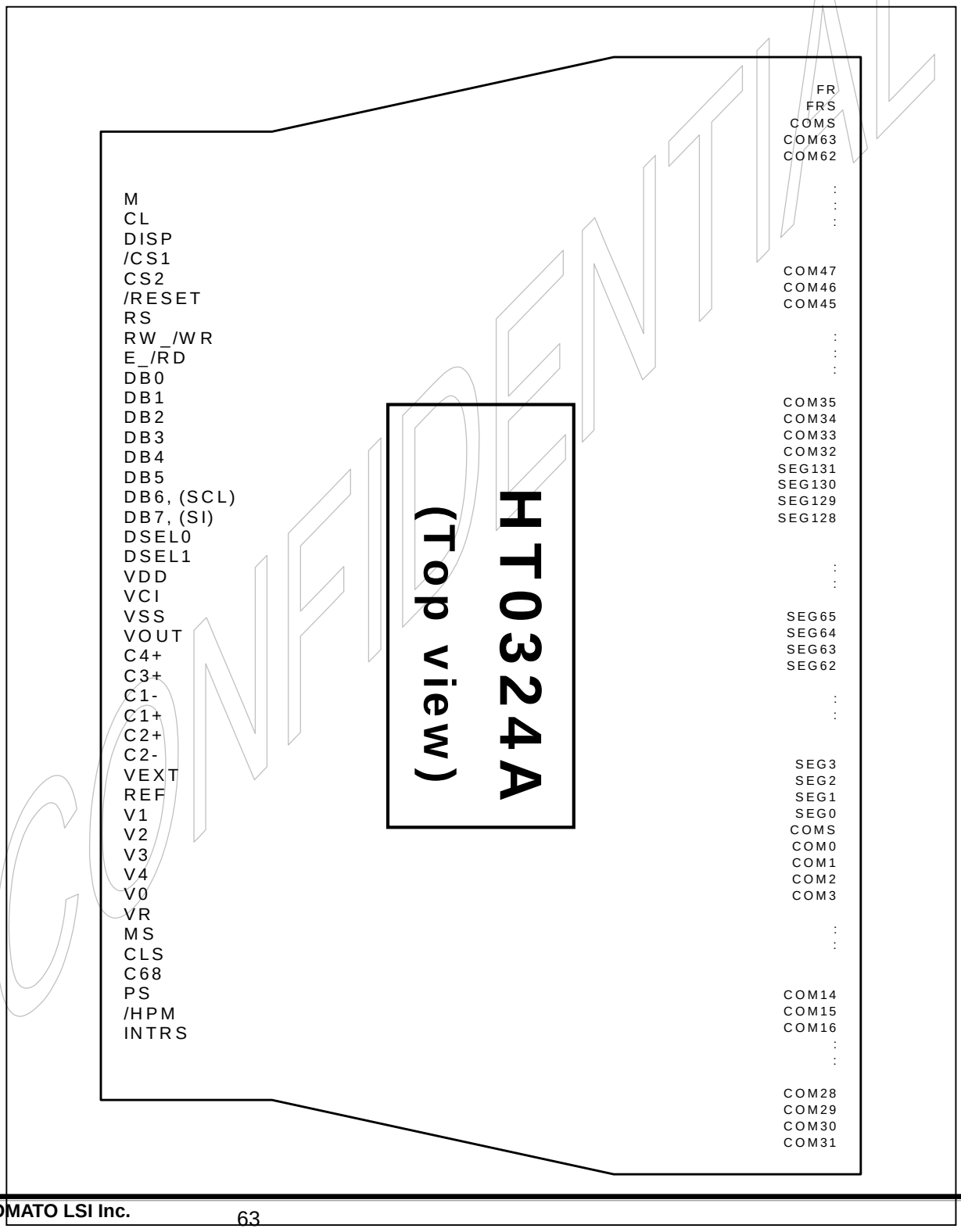

Figure 9-22. TCP pin layout

9-4. Application circuit for serial

-. Package type: TCP
-. Device mode: Master mode, Internal OSC, normal mode, 4-times boost-up, internal resistor

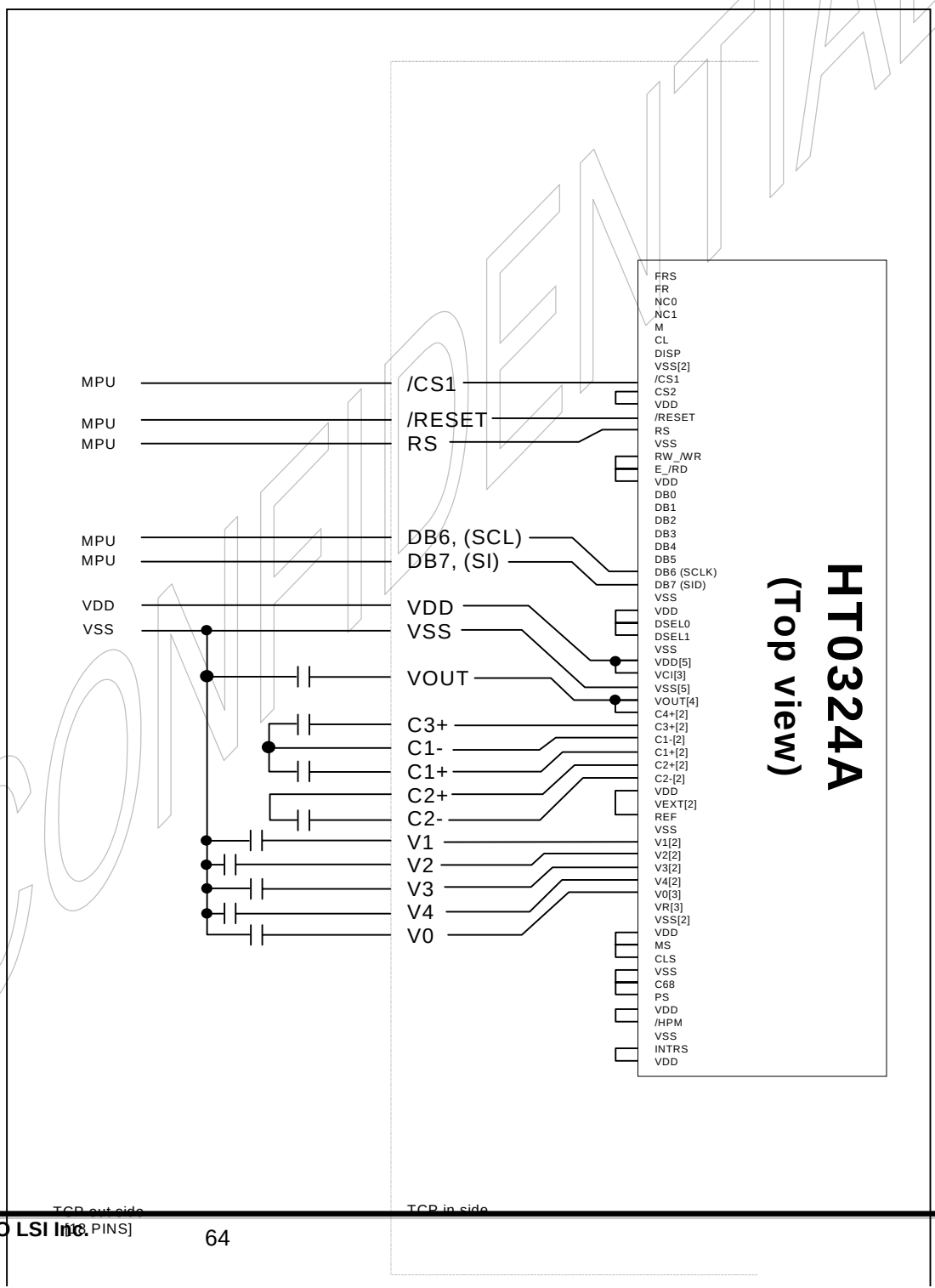

Figure 9-23. HT0324A Application circuit for serial