LCD Controller Product Line Selection Table

HT162X	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626	HT1627	HT16270
COM	4	4	8	8	8	8	16	**16**	16
SEG	32	32	32	32	48	64	48	**64**	64
Built-in Osc.		√	√		√	√	√	√	
Crystal Osc.	√	√		√					√

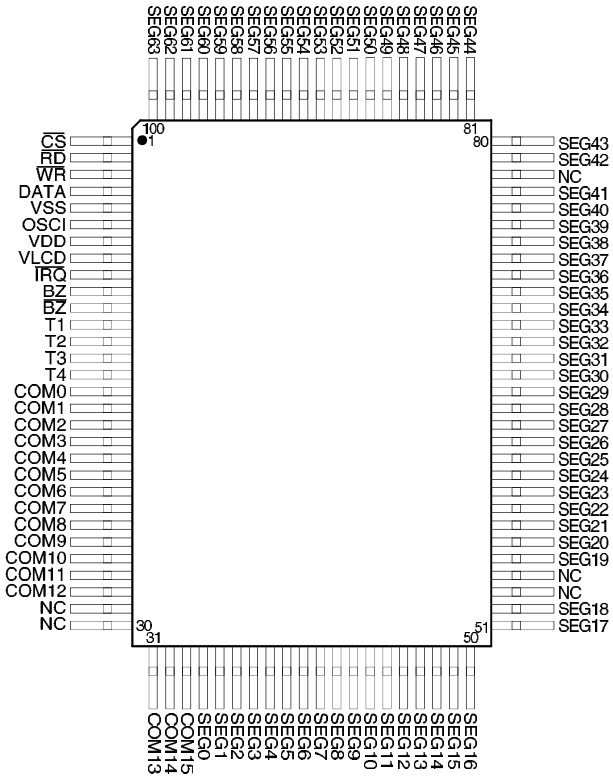
Features

- Operating voltage: 2.7V~5.2V
- Built-in RC oscillator
- Standby current < 2μA
- 1/5 bias, 1/16 duty, frame frequency is 64Hz
- Max. 64×16 patterns, 16 commons, 64 segments
- Built-in internal resistor type bias generator
- 3 wires serial interface
- 8 kinds time base /WDT selection
- Time base or WDT overflow output
- Built-in LCD display RAM
- R/W address auto increment
- Built-in buzzer driver (2K/4K)
- Power down command reduces power consumption
- Software configuration feature
- Data mode and Command mode instructions
- Three data accessing modes
- Provide VLCD pin to adjust LCD operating voltage

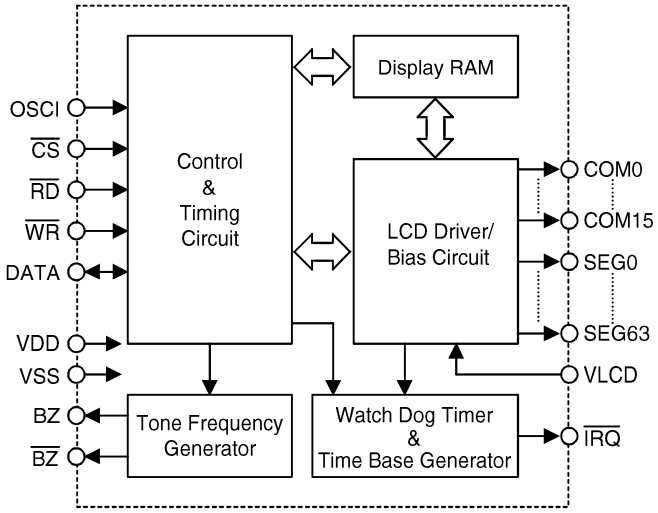
General Description

HT1627 is a peripheral device specially designed for I/O type μC used to expand the display capability. The max. display segment of the device are 1024 patterns (64×16). It also supports serial interface, buzzer sound, watchdog timer or time base timer functions. The HT1627 is a memory mapping and multifunction LCD controller. The software configuration feature of the HT1627 make it suitable for multiple LCD applications including LCD modules and display subsystems. Only 3 lines are required for the interface between the host controller and the HT1627. The HT162X series have many kinds of products that match various applications.

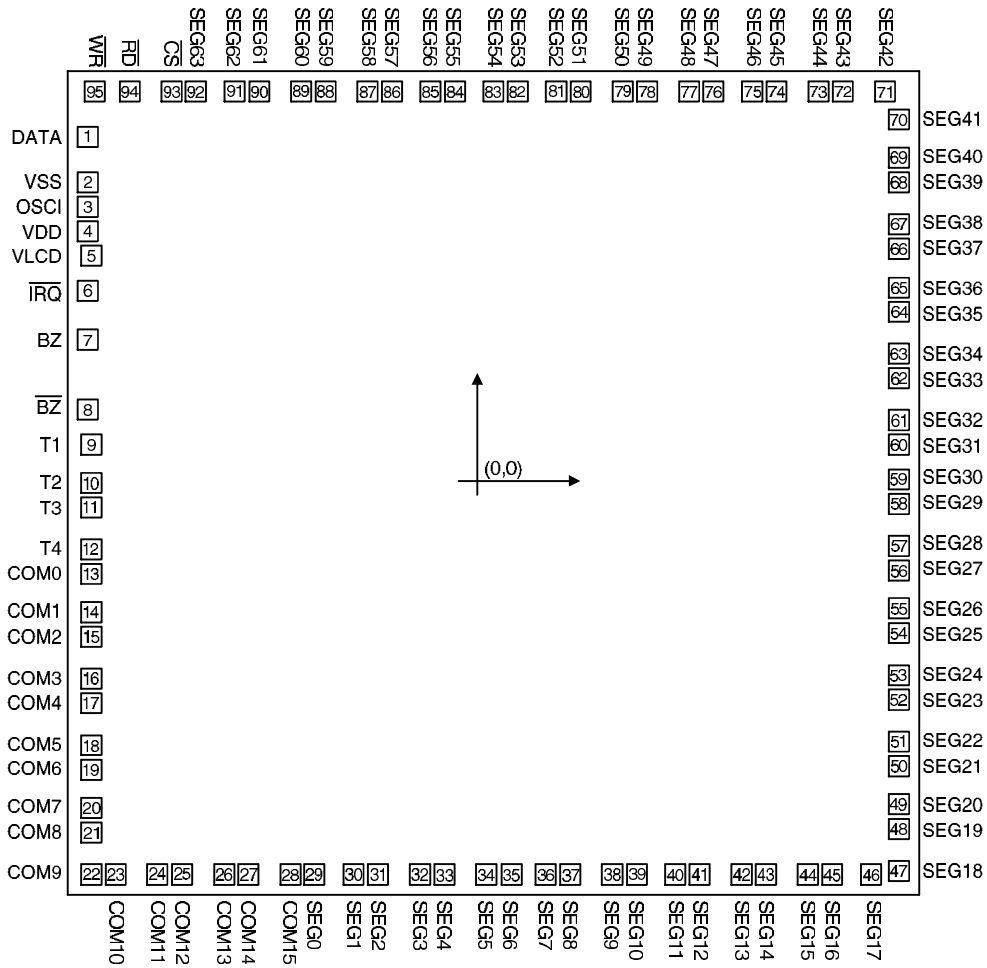
Pin Assignment (PQFP100)



Block Diagram



Pad Assignment (Layout Plot)



Chip size: 245×237 (mil)^2

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Unit: mil

Pad No.	X	Y	Pad No.	X	Y
1	–116.62	99.88	49	116.15	–93.20
2	–116.71	86.32	50	116.15	–81.22
3	–116.71	78.75	51	116.15	–74.59
4	–116.71	72.12	52	116.15	–62.60
5	–115.94	65.49	53	116.15	–55.97
6	–116.71	55.97	54	116.15	–43.99
7	–116.71	41.44	55	116.15	–37.36
8	–116.71	21.84	56	116.15	–25.37
9	–115.94	11.39	57	116.15	–18.74
10	–115.94	–0.60	58	116.15	–6.76
11	–115.94	–7.22	59	116.15	–0.13
12	–115.94	–19.21	60	116.15	11.86
13	–115.94	–25.84	61	116.15	18.49
14	–115.94	–37.83	62	116.15	30.47
15	–115.94	–44.46	63	116.15	37.10
16	–115.94	–56.44	64	116.15	49.09
17	–115.94	–63.07	65	116.15	55.72
18	–115.94	–75.06	66	116.15	67.70
19	–115.94	–81.68	67	116.15	74.33
20	–115.94	–93.67	68	116.15	86.32
21	–115.94	–100.30	69	116.15	92.95
22	–115.94	–112.29	70	116.15	104.93
23	–108.04	–112.03	71	112.03	112.24
24	–96.05	–112.03	72	100.04	112.24
25	–89.42	–112.03	73	93.42	112.24
26	–77.43	–112.03	74	81.43	112.24
27	–70.81	–112.03	75	74.80	112.24
28	–58.82	–112.03	76	62.81	112.24
29	–52.19	–112.03	77	56.19	112.24
30	–40.21	–112.03	78	44.20	112.24
31	–33.58	–112.03	79	37.57	112.24
32	–21.59	–112.03	80	25.58	112.24
33	–14.96	–112.03	81	18.95	112.24
34	–2.97	–112.03	82	6.97	112.24
35	3.65	–112.03	83	0.34	112.24
36	15.64	–112.03	84	–11.65	112.24
37	22.27	–112.03	85	–18.27	112.24
38	34.26	–112.03	86	–30.26	112.24
39	40.88	–112.03	87	–36.89	112.24
40	52.87	–112.03	88	–48.88	112.24
41	59.50	–112.03	89	–55.51	112.24
42	71.49	–112.03	90	–67.49	112.24
43	78.11	–112.03	91	–74.12	112.24
44	90.10	–112.03	92	–86.11	112.24
45	96.73	–112.03	93	–92.74	112.24
46	108.71	–112.03	94	–104.72	112.24
47	116.15	–111.82	95	–114.24	112.24
48	116.15	–99.83			

Pad Description

Pad No.	Pad Name	I/O	Description
93	$\overline{CS}$	I	Chip selection input with pull high resistor. When the $\overline{CS}$ is logic high, the data and command read from or written to the HT1627 are disabled. The serial interface circuit is also reset But if the $\overline{CS}$ is at a logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1627
94	$\overline{RD}$	I	READ clock input with pull high resistor.Data in the RAM of the HT1627 are clocked out on the rising edge of the $\overline{RD}$ signal. The clocked out data will appear on the data line. The host controller can use the next falling edge to latch the clocked out data.
95	$\overline{WR}$	I	WRITE clock input with a pull high resistor. Data on the DATA line are latched into the HT1627 on the rising edge of the $\overline{WR}$ signal.
1	DATA	I/O	Serial data input/output with a pull high resistor
2	VSS	I	Negative power supply, Ground
3	OSCI	I	If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad.
4	VDD	I	Positive power supply
5	VLCD	I	LCD operating voltage input pad.
6	$\overline{IRQ}$	O	Time base or Watch Dog Timer overflow flag, NMOS open drain output
7, 8	BZ, $\overline{BZ}$	O	2K or 4K frequency output pair (Tristate output buffer)
9~12	T1~T4	I	Not connected
13~28	COM0~COM15	O	LCD common outputs
29~92	SEG0~SEG63	O	LCD segment outputs

Absolute Maximum Ratings*

Supply Voltage ..... –0.3V to 5.5V

Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V

Storage Temperature..... –50°C to 125°C

Operating Temperature..... –25°C to 75°C

*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damageto the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating voltage	—	—	2.7	—	5.2	V
I_{DD1}	Operating current	3V	No load/LCD on On chip RC oscillator		200	300	μA
		5V			300	400	μA
I_{DD2}	Operating current	3V	No load/LCD off On chip RC oscillator		15	40	μA
		5V			30	60	μA
I_{STB}	Standby current	3V	No load Power down mode			1	μA
		5V				2	μA
V_{IL}	Input low voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	0		0.6	V
		5V		0		1.0	V
V_{IH}	Input high voltage	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	2.4		3	V
		5V		4.0		5	V
I_{OL1}	BZ, $\overline{BZ}$, $\overline{IRQ}$	3V	V_{OL}=0.3V	0.9	1.8		mA
		5V	V_{OL}=0.5V	1.7	3		mA
I_{OH1}	BZ, $\overline{BZ}$	3V	V_{OH}=2.7V	0.9	1.8		mA
		5V	V_{OH}=4.5V	1.7	3		mA
I_{OL2}	DATA	3V	V_{OL}=0.3V	0.9	1.8		mA
		5V	V_{OL}=0.5V	1.7	3		mA
I_{OH2}	DATA	3V	V_{OH}=2.7V	0.9	1.8		mA
		5V	V_{OH}=4.5V	1.7	3		mA
I_{OL3}	LCD common sink current	3V	V_{OL}=0.3V	80	160		μA
		5V	V_{OL}=0.5V	180	360		μA
I_{OH3}	LCD common source current	3V	V_{OH}=2.7V	40	80		μA
		5V	V_{OH}=4.5V	90	180		μA
I_{OL4}	LCD segment sink current	3V	V_{OL}=0.3V	50	100		μA
		5V	V_{OL}=0.5V	120	240		μA
I_{OH4}	LCD segment source current	3V	V_{OH}=2.7V	30	60		μA
		5V	V_{OH}=4.5V	70	140		μA
R_{PH}	Pull-high resistor	3V	DATA, $\overline{WR}$, $\overline{CS}$, $\overline{RD}$	100	200		kΩ
		5V		50	100		kΩ

A.C. Characteristics

(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
f_{SYS1}	System Clock	3V	On chip RC oscillator	22	32	40	kHz
		5V		24	32	40	kHz
f_{SYS2}	System Clock	3V	External clock source		32		kHz
		5V			32		kHz
f_{LCD1}	LCD Frame Frequency	—	On chip RC oscillator	44	64	80	Hz
				48	64	80	Hz
f_{LCD2}	LCD Frame Frequency	3V	External clock source		64		Hz
		5V			64		Hz
t_{COM}	LCD Common Period	—	n: Number of COM		n/f_{LCD}		sec
f_{CLK1}	Serial Data Clock ($\overline{WR}$ Pin)	3V	Duty cycle 50%			150	kHz
		5V				300	kHz
f_{CLK2}	Serial Data Clock ($\overline{RD}$ Pin)	3V	Duty cycle 50%			75	kHz
		5V				150	kHz
t_{CS}	Serial Interface Reset Pulse Width	—	$\overline{CS}$	—	250	—	ns
t_W	Pulse Width Serial Data Clock (Figure 1)	3V	Write mode	3.34	—	—	μs
			Read mode	6.67			
		5V	Write mode	1.67	—	—	μs
			Read mode	3.34			
t_{rtf}	Rise/Fall Time Serial Data Clock (Figure 1)	3V	—	—	120	—	ns
		5V					
t_{su}	Setup Time DATA to Serial Data Clock (Figure 2)	3V	—	—	120	—	ns
		5V					
t_h	Hold Time DATA to Serial Data Clock (Figure 3)	3V	—	—	120	—	ns
		5V					
t_n	Low to $\overline{CS}$ High Serial Data Clock (Figure 3)	3V	—	—	100	—	ns
		5V					
t_{rec}	$\overline{CS}$ High to Serial Data Clock High (Figure 3)	3V	—	—	100	—	ns
		5V					

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
t_w	Serial Interface Reset High (Figure 3)	3V	—	—	250	—	ns
		5V					
t_{su}	$\overline{CS}$ Low to Serial Pulse Width Serial Data Clock High (Figure 3)	3V	—	—	100	—	ns
		5V					

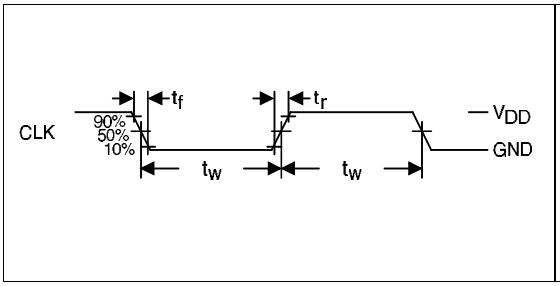


Figure 1.

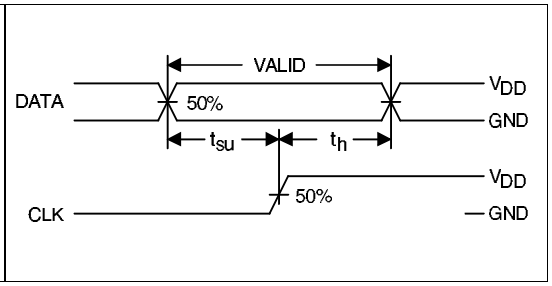


Figure 2.

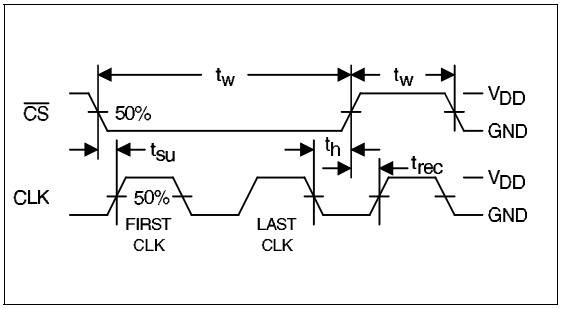
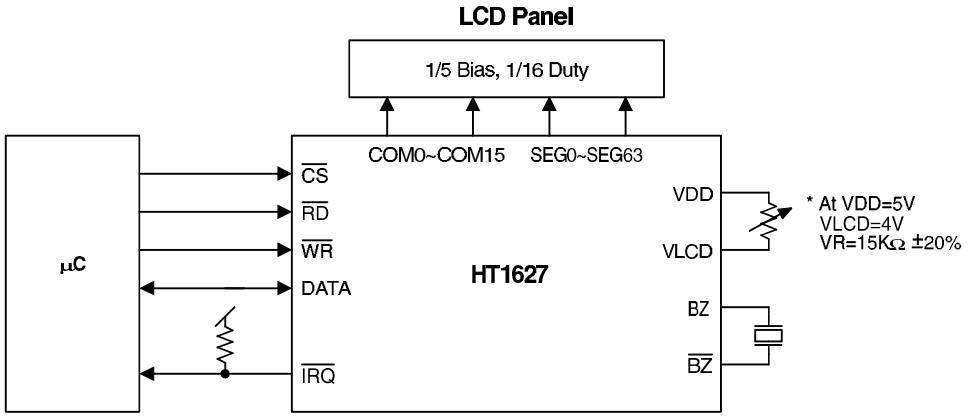


Figure 3.

Application Diagram



* The connection of $\overline{IRQ}$ and $\overline{RD}$ pin can be selected depending on the requirement of the host controller.

* Note: The VDD voltage must greater than VLCD PIN. (VDD ≥ VLCD)

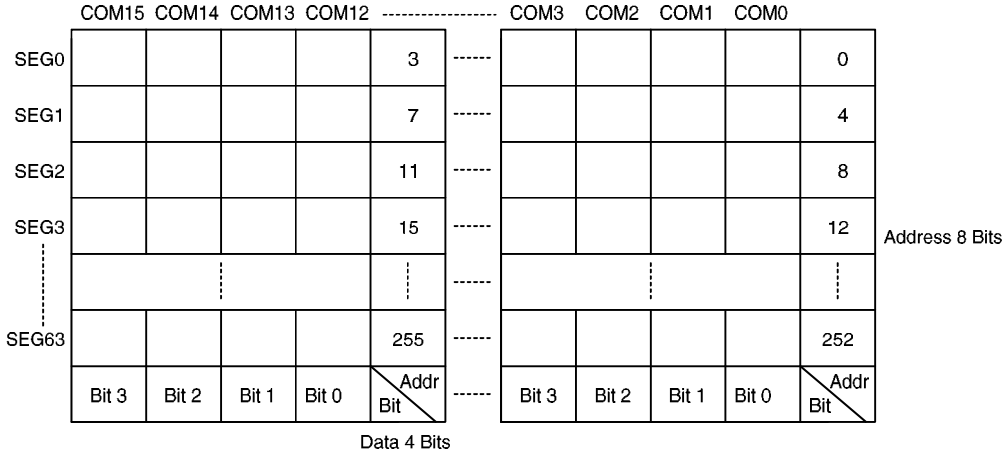
System Architecture

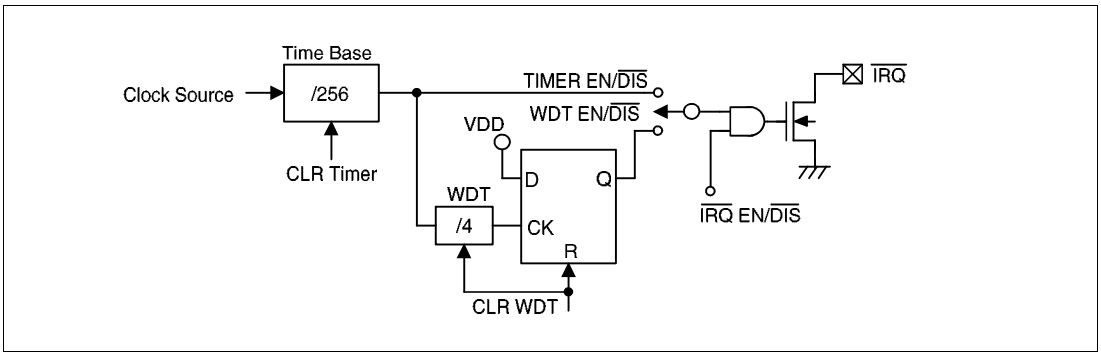
Display memory - RAM structure

The static display RAM is organized into 256*4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

Time base and watchdog timer (WDT)

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and $\overline{IRQ}$ EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{IRQ}$ pin will stay at a logic low level until the CLR WDT or the $\overline{IRQ}$ DIS command is issued.





Time base and WDT configurations

If an external clock is selected as the source of system frequency, the SYS DIS command turns out invalid and the power down mode fails to be carried out until the external clock source is removed.

Buzzer tone output

A simple tone generator is implemented in the HT1627. The tone generator can output a pair of differential driving signals on the BZ and $\overline{BZ}$ which are used to generate a single tone.

Command format

The HT1627 can be configured by the software setting. There are two mode commands to configure the HT1627 resource and to transfer the LCD display data.

The following are the data mode ID and the command mode ID:

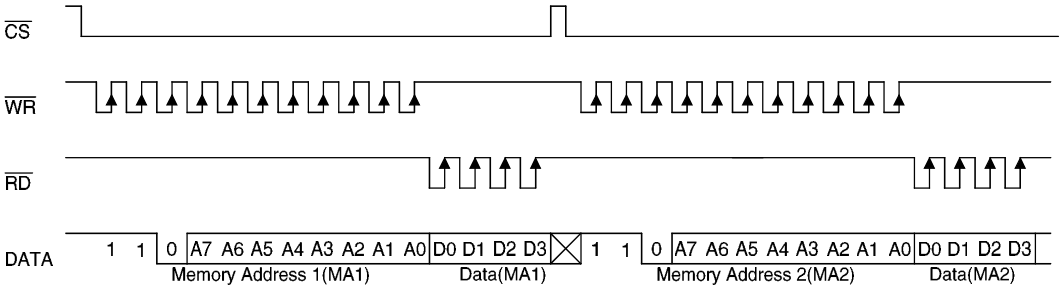
Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

If successive commands have been issued, the command mode ID can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the $\overline{CS}$ pin should be set to "1" and the previous operation mode will be reset also. The $\overline{CS}$ pin returns to "0", a new operation mode ID should be issued first.

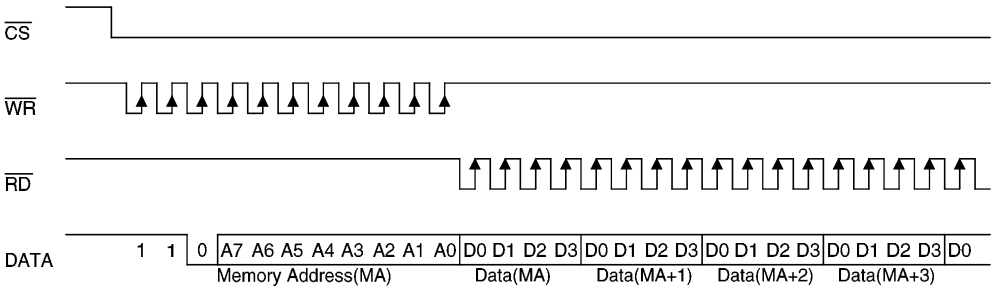
Name	Command Code	Function
TONE OFF	0000-1000-X	Turn-off tone output
TONE 4K	010X-XXXX-X	Turn-on tone output, tone frequency is 4kHz
TONE 2K	0110-XXXX-X	Turn-on tone output, tone frequency is 2kHz

Timing Diagrams

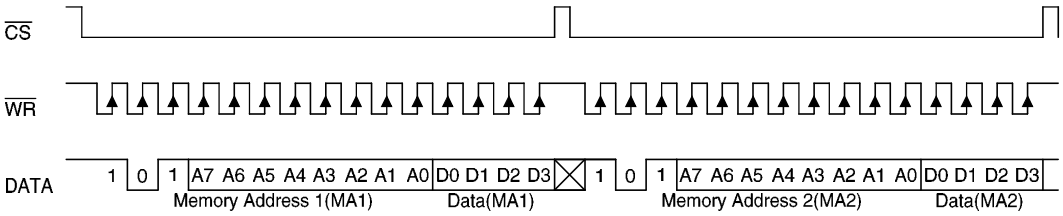
READ mode (command code : 1 1 0)



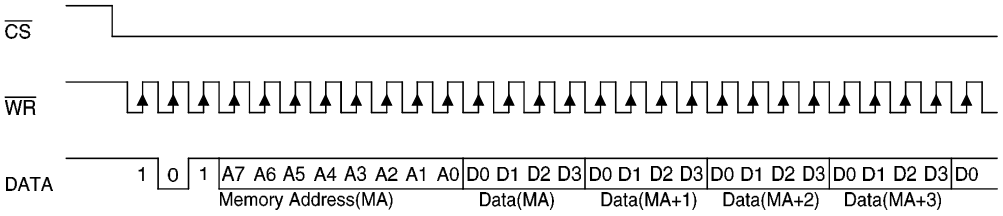
READ mode (successive address reading)



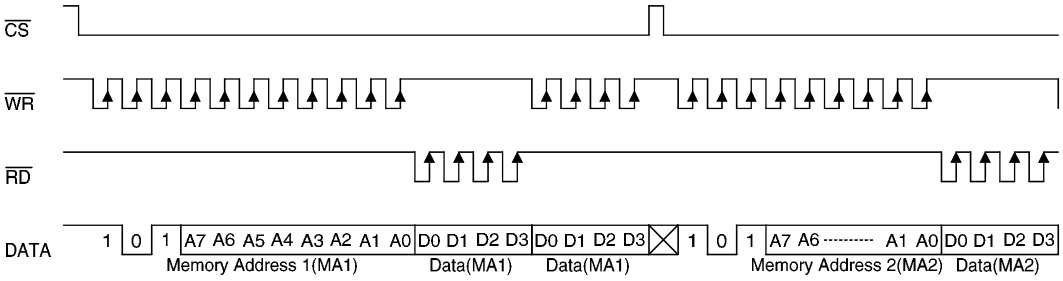
WRITE mode (command code : 1 0 1)



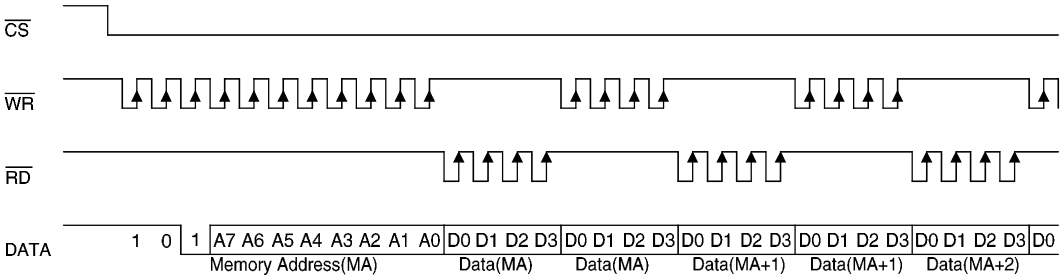
WRITE mode (successive address writing)



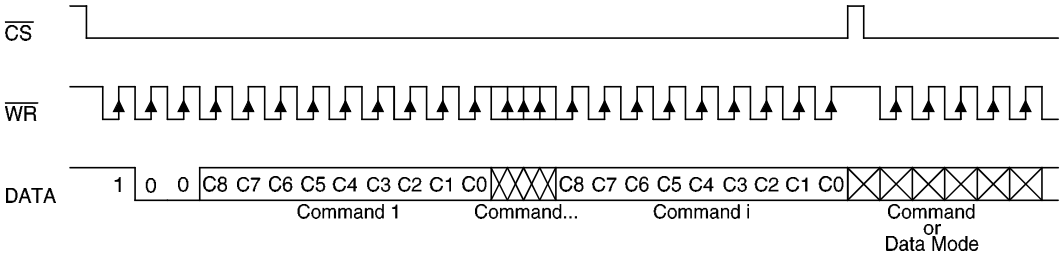
READ-MODIFY-WRITE mode (command code : 1 0 1)



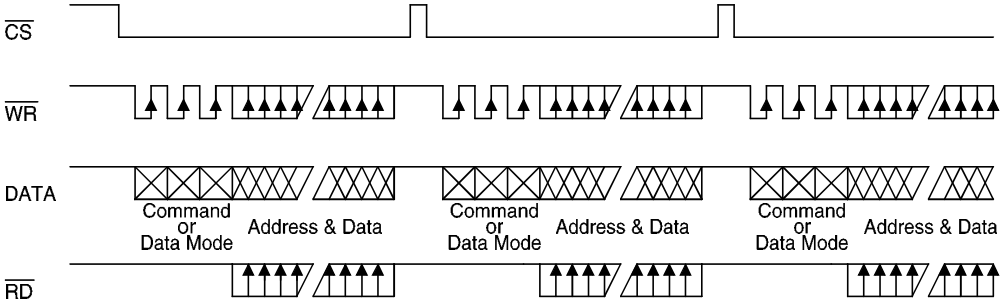
READ-MODIFY-WRITE mode (successive address accessing)



Command mode (command code : 1 0 0)



Mode (data & command mode)



Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	a7a6a5a4a3a2a1a0 d0d1d2d3	D	Read data from the RAM	
WRITE	101	a7a6a5a4a3a2a1a0 d0d1d2d3	D	Write data to the RAM	
Read-modify-write	101	a7a6a5a4a3a2a1a0 d0d1d2d3	D	Read and Write data to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off system oscillator	O
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD display	O
LCD ON	100	0000-0011-X	C	Turn on LCD display	
TIMER DIS	100	0000-0100-X	C	Disable time base output	O
WDT DIS	100	0000-0101-X	C	Disable WDT time-out flag output	O
TIMER EN	100	0000-0110-X	C	Enable time base output	
WDT EN	100	0000-0111-X	C	Enable WDT time-out flag output	
TONE OFF	100	0000-1000-X	C	Turn off tone outputs	O
CLR TIMER	100	0000-1101-X	C	Clear the contents of the time base generator	
CLR WDT	100	0000-1111-X	C	Clear the contents of WDT stage	
RC 32K	100	0001-10XX-X	C	System clock source, on-chip RC oscillator	O
EXT	100	0001-11XX-X	C	System clock source, external clock source	
TONE 4K	100	010X-XXXX-X	C	Tone frequency output: 4kHz	
TONE 2K	100	0110-XXXX-X	C	Tone frequency output: 2kHz	
$\overline{\text{IRQ}}$ DIS	100	100X-0XXX-X	C	Disable $\overline{\text{IRQ}}$ output	O
$\overline{\text{IRQ}}$ EN	100	100X-1XXX-X	C	Enable $\overline{\text{IRQ}}$ output	
F1	100	101X-0000-X	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	100	101X-0001-X	C	Time base clock output: 2Hz The WDT time-out flag after: 2s	
F4	100	101X-0010-X	C	Time base clock output: 4Hz The WDT time-out flag after: 1s	
F8	100	101X-0011-X	C	Time base clock output: 8Hz The WDT time-out flag after: 1/2s	
F16	100	101X-0100-X	C	Time base clock output: 16Hz The WDT time-out flag after: 1/4s	

Name	ID	Command Code	D/C	Function	Def.
F32	100	101X-0101-X	C	Time base clock output: 32Hz The WDT time-out flag after: 1/8s	
F64	100	101X-0110-X	C	Time base clock output: 64Hz The WDT time-out flag after: 1/16s	
F128	100	101X-0111-X	C	Time base clock output: 128Hz The WDT time-out flag after: 1/32s	O
TOPT	100	1110-0000-X	C	Test mode	
NORMAL	100	1110-0011-X	C	Normal mode	O

Note: X: Don't care

a7~a0: RAM address

d3~d0: RAM data

D/C: Data/Command mode

Def.: Default