Direct Rambus™ RIMM™ Memory Module Specification

GENERAL DESCRIPTION

This document outlines specifications for HCD's Direct Rambus RIMM Module which consists of 128Mb / 144Mb Direct Rambus DRAM devices. HCD supports applications with 600, 700 and 800 MHz speed grades in both ECC and non-ECC modules.

Table 1: Model Numbers by Frequency

Model Numbers	Description	Components
HR064N04E	64MB 16bit 600MHz non-ECC	128Mb x 4pcs
HR064N04D	64MB 16bit 700MHz non-ECC	128Mb x 4pcs
HR064N04C	64MB 16bit 700MHz non-ECC	128Mb x 4pcs
HR064N04B	64MB 16bit 800Mhz non-ECC	128Mb x 4pcs
HR064E04E	64MB 18bit 600MHz ECC	144Mb x 4pcs
HR064E04D	64MB 18bit 700MHz ECC	144Mb x 4pcs
HR064E04C	64MB 18bit 700MHz ECC	144Mb x 4pcs
HR064E04B	64MB 18bit 800MHz ECC	144Mb x 4pcs

FEATURES

- 184-pin 1mm pin spacing.
- 128Mb/144Mb Direct RDRAM CSPs.
- Operates from a 2.5 volt supply (± 5%).
- Serial Presence Detect support (SPD).
- Low power and power down self-refresh modes.
- Gold contacts.
- Optimizes time delays.
- Superior design and manufacturing techniques.

Figure 1: Direct Rambus™ RIMM™ Module without Heat Spreader

Table 2: Module Pad Number and Signal Names

Pad	Signal Name	Pad	Signal Name
A1	Gnd	B1	Gnd
A2	LDQA8	B2	LDQA7
A3	Gnd	B3	Gnd
A4	LDQA6	B4	LDQA5
A5	Gnd	B5	Gnd
A6	LDQA4	B6	LDQA3
A7	Gnd	B7	Gnd
A8	LDQA2	B8	LDQA1
A9	Gnd	B9	Gnd
A10	LDQA0	B10	LCFM
A11	Gnd	B11	Gnd
A12	LCTMN	B12	LCFMN
A13	Gnd	B13	Gnd
A14	LCTM	B14	NC
A15	Gnd	B15	Gnd
A16	NC	B16	LROW2
A17	Gnd	B17	Gnd
A18	LROW1	B18	LROW0
A19	Gnd	B19	Gnd
A20	LCOL4	B20	LCOL3
A21	Gnd	B21	Gnd
A22	LCOL2	B22	LCOL1
A23	Gnd	B23	Gnd
A24	LCOL0	B24	LDQB0
A25	Gnd	B25	Gnd
A26	LDQB1	B26	LDQB2
A27	Gnd	B27	Gnd
A28	LDQB3	B28	LDQB4
A29	Gnd	B29	Gnd
A30	LDQB5	B30	LDQB6
A31	Gnd	B31	Gnd
A32	LDQB7	B32	LDQB8
A33	Gnd	B33	Gnd
A34	LSCK	B34	LCMD
A35	Vcmos	B35	Vcmos
A36	SOUT	B36	SIN
A37	Vcmos	B37	Vcmos
A38	NC	B38	NC
A39	Gnd	B39	Gnd
A40	NC	B40	NC
A41	Vdd	B41	Vdd
A42	Vdd	B42	Vdd
A43	NC	B43	NC
A44	NC	B44	NC
A45	NC	B45	NC
A46	NC	B46	NC

Pad	Signal Name	Pad	Signal Name
A47	NC	B47	NC
A48	NC	B48	NC
A49	NC	B49	NC
A50	NC	B50	NC
A51	Vref	B51	Vref
A52	Gnd	B52	Gnd
A53	SCL	B53	SA0
A54	Vdd	B54	Vdd
A55	SDA	B55	SA1
A56	SVdd	B56	SVdd
A57	SWP	B57	SA2
A58	Vdd	B58	Vdd
A59	RSCK	B59	RCMD
A60	Gnd	B60	Gnd
A61	RDQB7	B61	RDQB8
A62	Gnd	B62	Gnd
A63	RDQB5	B63	RDQB6
A64	Gnd	B64	Gnd
A65	RDQB3	B65	RDQB4
A66	Gnd	B66	Gnd
A67	RDQB1	B67	RDQB2
A68	Gnd	B68	Gnd
A69	RCOL0	B69	RDQB0
A70	Gnd	B701	Gnd
A71	RCOL2	B71	RCOL1
A72	Gnd	B72	Gnd
A73	RCOL4	B73	RCOL3
A74	Gnd	B74	Gnd
A75	RROW1	B75	RROW0
A76	Gnd	B76	Gnd
A77	NC	B77	RROW2
A78	Gnd	B78	Gnd
A79	RCTM	B79	NC
A80	Gnd	B80	Gnd
A81	RCTMN	B81	RCFMN
A82	Gnd	B82	Gnd
A83	RDQA0	B83	RCFM
A84	Gnd	B84	Gnd
A85	RDQA2	B85	RDQA1
A86	Gnd	B86	Gnd
A87	RDQA4	B87	RDQA3
A88	Gnd	B88	Gnd
A89	RDQA6	B89	RDQA5
A90	Gnd	B90	Gnd
A91	RDQA8	B91	RDQA7
A92	Gnd	B92	Gnd

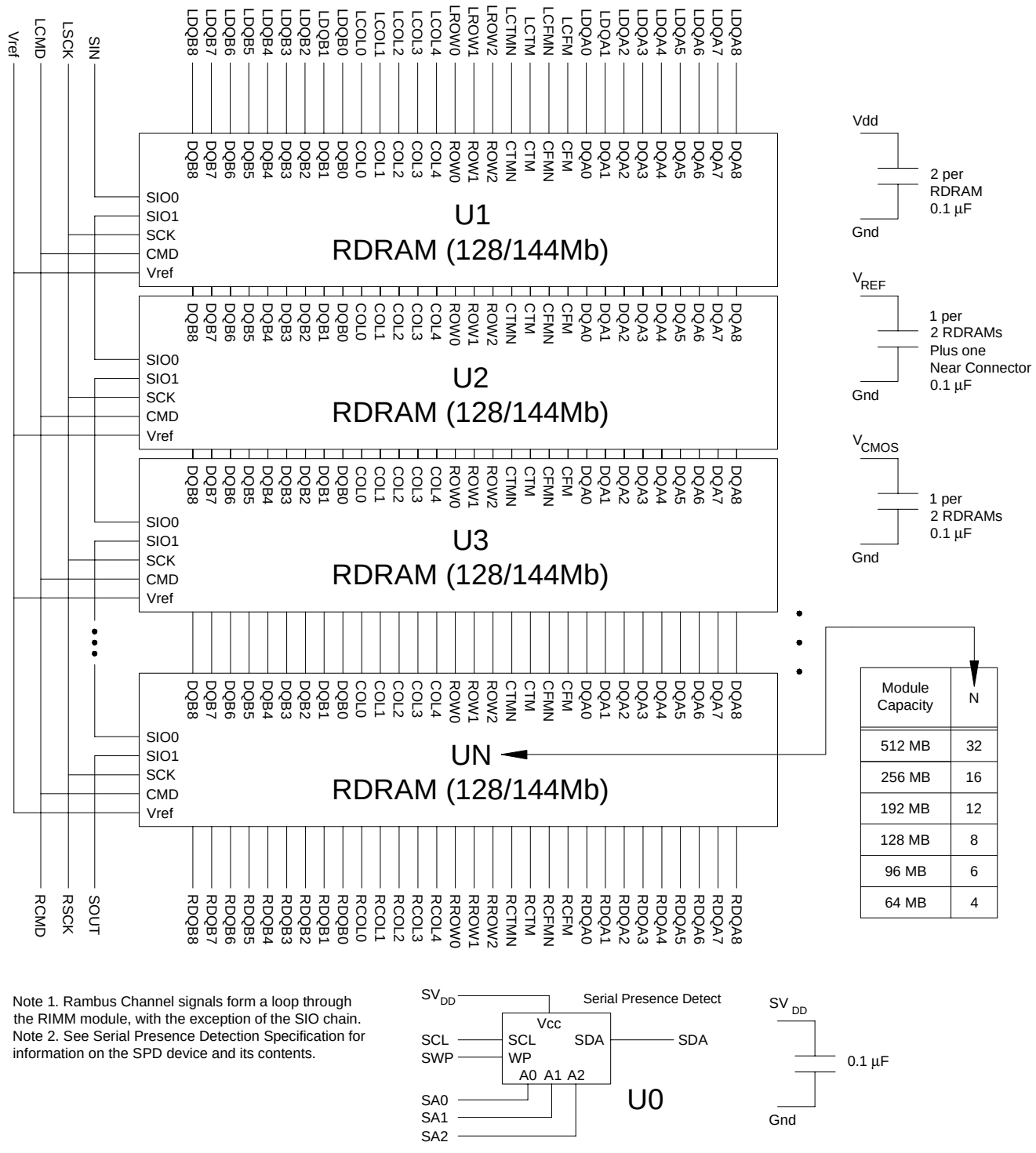
Table 3: Module Connector Pad Description

Signal	Module Connector Pads	I/O	Type	Description
Gnd	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A39, A52, A60, A62, A64 A66, A68, A70, A72, A74, A76, A78 A80, A82, A84, A86, A88, A90, A92 B1, B3, B5, B7, B9, B11, B13, B15 B17, B19, B21, B23, B25, B27, B29 B31, B33, B39, B52, B60, B62, B64 B66, B68, B70, B72, B74, B76, B78 B80, B82, B84, B86, B88, B90, B92			Ground reference for RDRAM core and interface, 72PCB connector pads.
LCFM	B10	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	B12	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	B34	I	V_{CMOS}	Serial Command used to read from and write to the control registers. Also used for power management.
LCOL4 LCOL0	A20, B20, A22, B22, A24	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	A14	I	RSL	Clock to Master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	A12	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8 LDQA0	A2, B2, A4, B4, A6, B6, A8, B8, A10	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices.
LDQB8 LDQB0	B32, A32, B30, A30, B28, A28, B26, A26, B24	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices.
LROW2L ROW0	B16, A18, B18	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	A34	I	V_{CMOS}	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
NC	A16, B14, A38, B38, A40, B40, A43, B43, A44, B44, A45, B45, A46, B46, A47, B47, A48, B48, A49, B49, A50, B50, A77, B79			These pads are not connected. These 24 connector pads are reserved for future use.
RCFM	B83	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	B81	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.

Table 3: Module Connector Pad Description (cont.)

Signal	Module Connector Pads	I/O	Type	Description
RCMD	B59	I	V_{CMOS}	Serial Command Input. Pin used to read from and write to the control registers. Also used for power management.
RCOL4 RCOL0	A73, B73, A71, B71, A69	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	A79	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	A81	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8 RDQA0	A91, B91, A89, B89, A87, B87, A85, B85, A83	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules with x16 RDRAM devices.
RDQB8.. RDQB0	B61, A61, B63, A63, B65, A65, B67, A67, B69	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules with x16 RDRAM devices.
RROW2 RROW0	B77, A75, B75	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
RSCK	A59	I	V_{CMOS}	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	B53	I	SV_{DD}	Serial Presence Detect Address 0.
SA1	B55	I	SV_{DD}	Serial Presence Detect Address 1.
SA2	B57	I	SV_{DD}	Serial Presence Detect Address 2.
SCL	A53	I	SV_{DD}	Serial Presence Detect Clock.
SDA	A55	I/O	SV_{DD}	Serial Presence Detect Data (Open Collector I/O).
SIN	B36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	A36	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SV_{dd}	A56, B56			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	A57	I	SV_{DD}	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	A35, B35, A37, B37			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A41, A42, A54, A58, B41, B42, B54, B58			Supply voltage for the RDRAM core and interface logic.
Vref	A51, B51			Logic threshold reference voltage for RSL signals.

Figure 2: Functional Block Diagram



Note 1. Rambus Channel signals form a loop through the RIMM module, with the exception of the SIO chain.
Note 2. See Serial Presence Detection Specification for information on the SPD device and its contents.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS signal pad with respect to Gnd.	- 0.3	V_{DD}+ 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd.	- 0.5	V_{DD}+ 1.0	V
T_{STORE}	Storage temperature.	- 50	100	°C

Table 5: DC Recommended Electrical Conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	2.5-0.13	2.5+0.13	V
V_{CMOS}	CMOS I/O power supply at pad for 2.5V controllers: CMOS I/O power supply at pad for 1.8V controllers:	2.5 - 0.13 1.8 - 0.1	2.5 + 0.25 1.8 + 0.2	V
V_{REF}	Reference voltage	1.4 - 0.2	1.4 + 0.2	V
V_{IL}	RSL input low voltage	V_{REF} - 0.5	V_{REF} - 0.2	V
V_{IH}	RSL input high voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
$V_{IL,CMOS}$	CMOS input low voltage	-0.3	$0.5V_{CMOS}$-0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	$0.5V_{CMOS}$+0.25	$0.5V_{CMOS}$ +0 .3	V
$V_{OL,CMOS}$	CMOS output low voltage @ $I_{OH,CMOS}$ = 1mA		0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$ = -0.25mA	V_{CMOS}-0.3		V
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	µA
$I_{SCK,CMD}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	µA
$I_{SIN,SOUT}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10.0	10.0	µA

Table 6: RIMM Module Capacity

RIMM Module Capacity:	256/288 MB	128/144 MB	96/108 MB	64/72 MB
Number of 128Mb or 144 Mb RDRAM devices:	16	8	6	4

Table 7: AC Electrical Specifications

Symbol	Parameter and Conditions	Min	Typ	Max	Units
Z	Module Impedance (RSL).	25.2	28	30.8	Ω
	Module Impedance (CMOS).	23.8	28	32.2	Ω
T_{PD}	Propagation delay, all RSL signals[a].	-		See Table [b]	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD}[c,d] for 4, 6, 8, and 12device modules.	-21		21	ps
	Propagation delay variation of RSL signals with respect to T_{PD}[c,d] for 16 device modules.	-24		24	ps
$\Delta T_{PD-CMOS}$	Propagation Delay variation of SCK and CMD signals with respect to an average clock delay [c].	-100		100	ps
V_{α}/V_{IN}	Attenuation Limit.			See Table [b]	%
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time @20-80%).			See Table [b]	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time @20-80%).			See Table [b]	%

a. Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).
b. Table 8 lists parameters and specifications for different storage capacity RIMM Modules that use 128Mb or 144Mb RDRAM devices.
c. T_{PD} or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).
d. If the RIMM module meets the following specification, then it is compliant to the specification.

Table 8: AC Electrical Specifications for RIMM Modules

Symbol	RIMM Module Capacity		256/288 MB	128/144MB	96/MB	64/72 MB	Units
	Number of 128/144 Mb RDRAMs:		16	8	6	4	
	Parameter and Condition for RIMM modules	Freq.	Max	Max	Max	Max	
T_{PD}	Propagation Delay, all RSL signals.	-800	2.06	1.56	1.40	1.25	ns
		-711	2.06	1.56	1.40	1.25	ns
		-600	2.10	1.60	1.40	1.25	ns
V_{α}/V_{IN}	Attenuation Limit.	-800	25	16	14	12	%
		-711	25	16	14	12	%
		-600	21	10	9	8	%
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time @20-80%).	-800	8	4	3	2	%
		-711	8	4	3	2	%
		-600	8	4	3	2	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time @20-80%).	-800	2.5	2.0	1.8	1.5	%
		-711	2.5	2.0	1.8	1.5	%
		-600	2.5	2.0	1.8	1.5	%
R_{DC}	DC Resistance.	-800	1.2	0.8	0.7	0.6	Ω
		-711	1.2	0.8	0.7	0.6	Ω
		-600	1.2	0.8	0.7	0.6	Ω

Figure 3: Physical Dimension

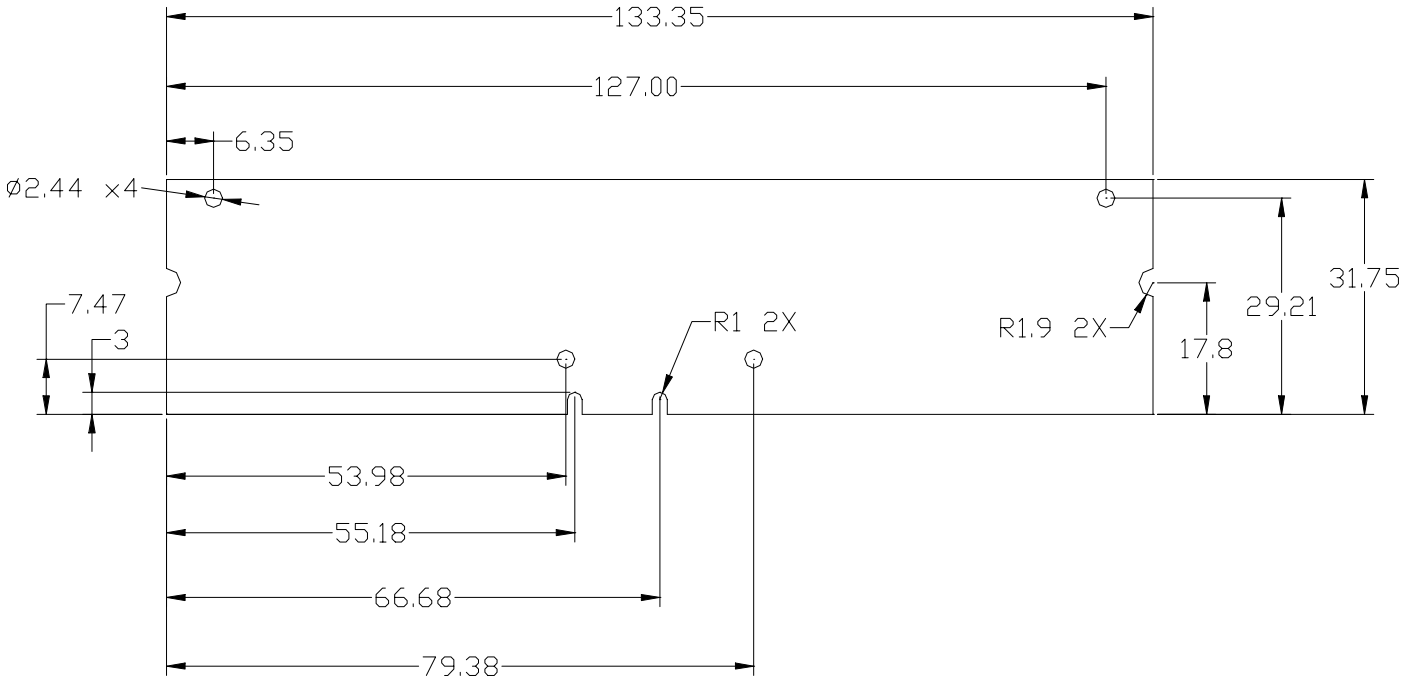
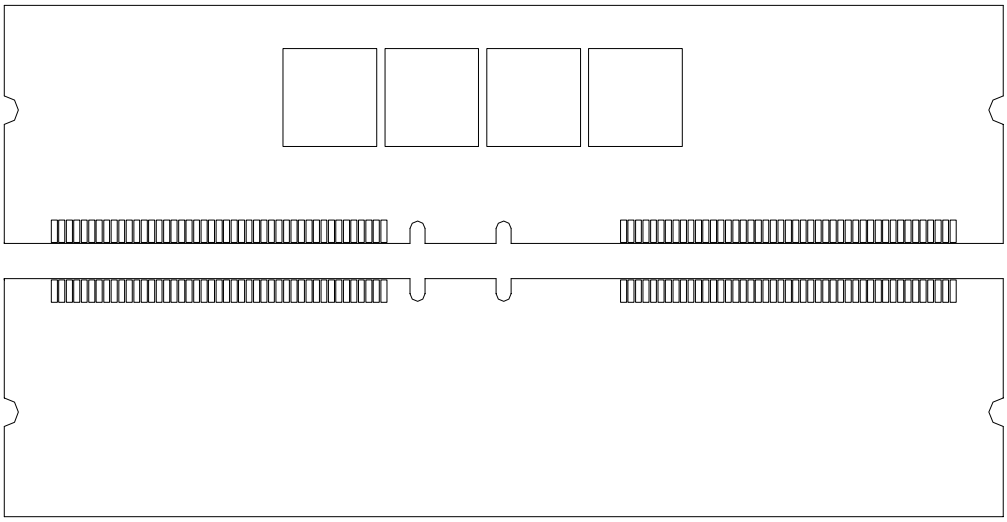


Figure 4: 184 Pin Rambus RIMM Module



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