Direct Rambus™ SO-RIMM™ Memory Module Specification

GENERAL DESCRIPTION

This document outlines specifications for HCD's Direct Rambus SO-RIMM Module which consists of 128Mb / 144Mb Direct Rambus DRAM devices. HCD supports applications with 600, 700 and 800 MHz speed grades in both ECC and non-ECC modules.

Table 1: Model Number by Frequency

Model Numbers	Description	**Components**
HS128N08E	128MB 16bit 600MHz non-ECC	128Mb x 8pcs
HS128N08D	128MB 16bit 700MHz non-ECC	128Mb x 8pcs
HS128N08C	128MB 16bit 700MHz non-ECC	128Mb x 8pcs
HS128N08B	128MB 16bit 800MHz non-ECC	128Mb x 8pcs
HS128E08E	128MB 18bit 600MHz ECC	144Mb x 8pcs
HS128E08D	128MB 18bit 700MHz ECC	144Mb x 8pcs
HS128E08C	128MB 18bit 700MHz ECC	144Mb x 8pcs
HS128E08B	128MB 18bit 800MHz ECC	144Mb x 8pcs

FEATURES

- 160-pin 0.67mm pin spacing.
- 128Mb/144Mb Direct RDRAM CSPs.
- Maximum module PCB size: 67.60mm x 31.25mm x 1.00mm (2.667" x 1.230" x 0.043").
- Gold contacts.
- Operates from a 2.5 volt supply (± 5%).
- Serial Presence Detect support (SPD).
- Low power and power down self-refresh modes.
- Optimizes time delays.
- Superior design and manufacturing techniques.

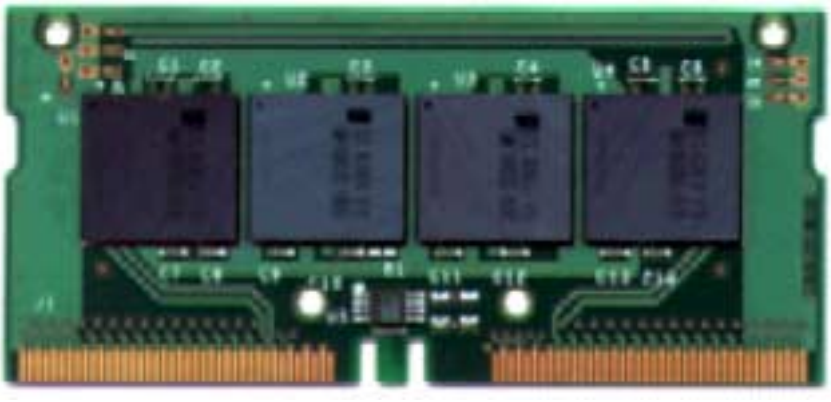


FIGURE 1: Rambus SO-RIMM™ Module without Heat Spreader
(Note: 4 additional RDRAMs are installed on the back side of the PCB)

Table 2: Module Pad Number and Signal Names

Pad	Signal Name	Pad	Signal Name
A1	Gnd	B1	Gnd
A2	LDQA8	B2	LDQA7
A3	Gnd	B3	Gnd
A4	LDQA6	B4	LDQA5
A5	Gnd	B5	Gnd
A6	LDQA4	B6	LDQA3
A7	Gnd	B7	Gnd
A8	LDQA2	B8	LDQA1
A9	Gnd	B9	Gnd
A10	LDQA0	B10	LCFM
A11	Gnd	B11	Gnd
A12	LCTM	B12	LCFMN
A13	Gnd	B13	Gnd
A14	LCTMN	B14	LROW2
A15	Gnd	B15	Gnd
A16	LROW1	B16	LROW0
A17	Gnd	B17	Gnd
A18	LCOL4	B18	LCOL3
A19	Gnd	B19	Gnd
A20	LCOL2	B20	LCOL1
A21	Gnd	B21	Gnd
A22	LCOL0	B22	LDQB1
A23	Gnd	B23	Gnd
A24	LDQB0	B24	LDQB3
A25	Gnd	B25	Gnd
A26	LDQB2	B26	LDQB5
A27	Gnd	B27	Gnd
A28	LDQB4	B28	LDQB7
A29	Gnd	B29	Gnd
A30	LDQB6	B30	LDQB8
A31	Gnd	B31	Gnd
A32	LSCK	B32	LCMD
A33	Gnd	B33	Gnd
A34	SOUT	B34	SIN
A35	Vdd	B35	Vdd
A36	NC	B36	NC
A37	Gnd	B37	Gnd
A38	NC	B38	NC
A39	Vcmos	B39	Vcmos
A40	NC	B40	NC

Pad	Signal Name	Pad	Signal Name
A41	NC	B41	NC
A42	Vref	B42	Vref
A43	SCL	B43	SA0
A44	Vdd	B44	Vdd
A45	SDA	B45	SA1
A46	Vdd	B46	Vdd
A47	SVdd	B47	SWP
A48	Gnd	B48	Gnd
A49	RSCK	B49	RCMD
A50	Gnd	B50	Gnd
A51	RDQB8	B51	RDQB6
A52	Gnd	B52	Gnd
A53	RDQB7	B53	RDQB4
A54	Gnd	B54	Gnd
A55	RDQB5	B55	RDQB2
A56	Gnd	B56	Gnd
A57	RDQB3	B57	RDQB0
A58	Gnd	B58	Gnd
A59	RDQB1	B59	RCOL0
A60	Gnd	B60	Gnd
A61	RCOL1	B61	RCOL2
A62	Gnd	B62	Gnd
A63	RCOL3	B63	RCOL4
A64	Gnd	B641	Gnd
A65	RROW0	B65	RROW1
A66	Gnd	B66	Gnd
A67	RROW2	B67	RCTMN
A68	Gnd	B68	Gnd
A69	RCFMN	B69	RCTM
A70	Gnd	B70	Gnd
A71	RCFM	B71	RDQA0
A72	Gnd	B72	Gnd
A73	RDQA1	B73	RDQA2
A74	Gnd	B74	Gnd
A75	RDQA3	B75	RDQA4
A76	Gnd	B76	Gnd
A77	RDQA5	B77	RDQA6
A78	Gnd	B78	Gnd
A79	RDQA7	B79	RDQA8
A80	Gnd	B80	Gnd

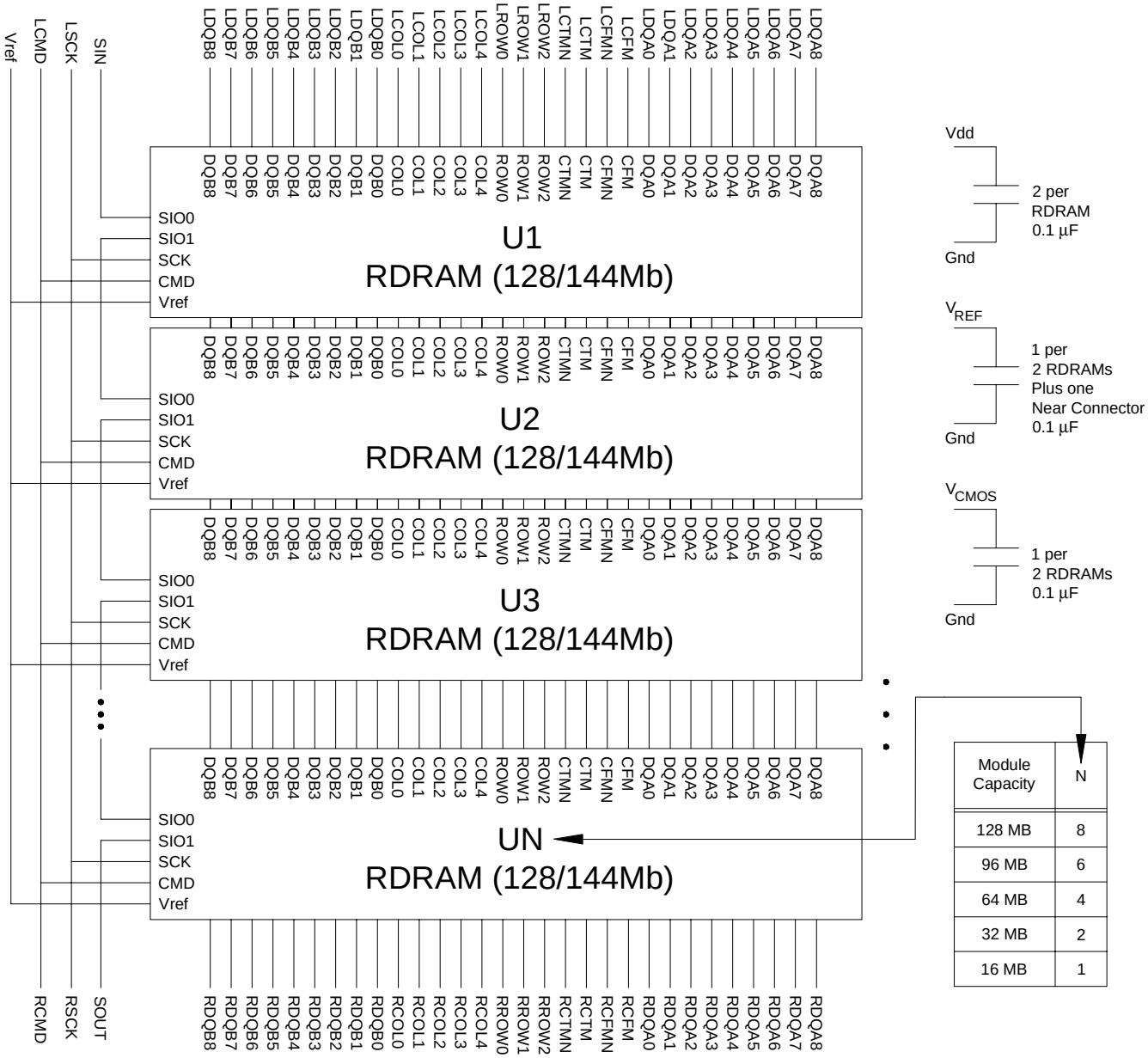
Table 3: Module Connector Pad Description

Signal	Module Connector Pads	I/O	Type	Description
Gnd	A1, A3, A5, A7, A9, A11, A13, A15, A17, A19, A21, A23, A25, A27, A29, A31, A33, A37, A48, A50, A52, A54 A56, A58, A60, A62, A64, A66, A68 A70, A72, A74, A76, A78, A80, B1, B3, B5, B7, B9, B11, B13, B15 B17, B19, B21, B23, B25, B27, B29 B31, B33, B37, B48, B50, B52, B54 B56, B58, B60, B62, B64, B66, B68 B70, B72, B74, B76, B78, B80			Ground reference for RDRAM core and interface, 72PCB connector pads.
LCFM	B10	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
LCFMN	B12	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.
LCMD	B32	I	V_{CMOS}	Serial Command used to read from and write to the control registers. Also used for power management.
LCOL4 LCOL0	A18, B18, A20, B20, A22	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
LCTM	A12	I	RSL	Clock to Master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
LCTMN	A14	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
LDQA8 LDQA0	A2, B2, A4, B4, A6, B6, A8, B8, A10	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQA8 is non-functional on modules with x16 RDRAM devices.
LDQB8 LDQB0	B30, B28, A30, B26, A28, B24, A26, B22, A24	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. LDQB8 is non-functional on modules with x16 RDRAM devices.
LROW2L ROW0	B14, A16, B16	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
LSCK	A32	I	V_{CMOS}	Serial clock input. Clock source used to read from and write to the RDRAM control registers.
NC	A36, B36, A38, B38, A40, B40, A41, B41			These pads are not connected. These 8 connector pads are reserved for future use.
RCFM	A71	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Positive polarity.
RCFMN	A69	I	RSL	Clock from master. Interface clock used for receiving RSL signals from the Channel. Negative polarity.

Table 3: Module Connector Pad Description (cont.)

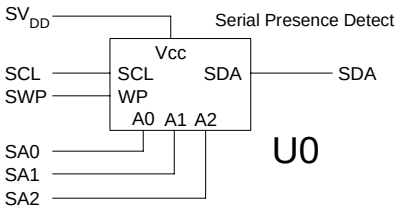
Signal	Module Connector Pads	I/O	Type	Description
RCMD	B49	I	V_{CMOS}	Serial Command Input. Pin used to read from and write to the control registers. Also used for power management.
RCOL4 RCOL0	B63, A63, B61, A61, B59	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	B69	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	B67	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8 RDQA0	B79, A79, B77, A77, B75, A75, B73, A73, B71	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQA8 is non-functional on modules with x16 RDRAM devices.
RDQB8.. RDQB0	A51, A53, B51, A55, B53, A57, B55, A59, B57	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM. RDQB8 is non-functional on modules with x16 RDRAM devices.
RROW2 RROW0	A67, B65, A65	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.
RSCK	A49	I	V_{CMOS}	Serial Clock input. Clock source used to read from and write to the RDRAM control registers.
SA0	B43	I	SV_{DD}	Serial Presence Detect Address 0.
SA1	B45	I	SV_{DD}	Serial Presence Detect Address 1.
SCL	A43	I	SV_{DD}	Serial Presence Detect Clock.
SDA	A45	I/O	SV_{DD}	Serial Presence Detect Data (Open Collector I/O).
SIN	B34	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO0 of the first RDRAM on the module.
SOUT	A34	I/O	V_{CMOS}	Serial I/O for reading from and writing to the control registers. Attaches to SIO1 of the last RDRAM on the module.
SV_{dd}	A47			SPD Voltage. Used for signals SCL, SDA, SWE, SA0, SA1 and SA2.
SWP	B47	I	SV_{DD}	Serial Presence Detect Write Protect (active high). When low, the SPD can be written as well as read.
V_{CMOS}	A39. B39			CMOS I/O Voltage. Used for signals CMD, SCK, SIN, SOUT.
Vdd	A35, B35, A44, B44, A46, B46			Supply voltage for the RDRAM core and interface logic.
Vref	A42, B42			Logic threshold reference voltage for RSL signals.

Figure 2: Functional Block Diagram



Module Capacity	N
128 MB	8
96 MB	6
64 MB	4
32 MB	2
16 MB	1

Note 1. Rambus Channel signals form a loop through the RIMM module, with the exception of the SIO chain.
Note 2. See Serial Presence Detection Specification for information on the SPD device and its contents.



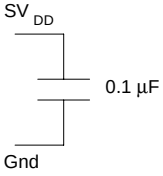


Table 4: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS signal pad with respect to Gnd.	- 0.3	V_{DD}+ 0.3	V
$V_{DD,ABS}$	Voltage on VDD with respect to Gnd.	- 0.5	V_{DD}+ 1.0	V
T_{STORE}	Storage temperature.	- 50	100	°C

Table 5: DC Recommended Electrical Conditions

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage	2.50-0.13	2.5+0.13	V
V_{CMOS}	CMOS I/O power supply at pad for 2.5V controllers: CMOS I/O power supply at pad for 1.8V controllers:	2.5 - 0.13 1.8 - 0.1	2.5 + 0.25 1.8 + 0.2	V
V_{REF}	Reference voltage	1.4 - 0.2	1.4 + 0.2	V
V_{IL}	RSL input low voltage	V_{REF} - 0.5	V_{REF} - 0.2	V
V_{IH}	RSL input high voltage	V_{REF} + 0.2	V_{REF} + 0.5	V
$V_{IL,CMOS}$	CMOS input low voltage	-0.3	$0.5V_{CMOS}$-0.25	V
$V_{IH,CMOS}$	CMOS input high voltage	$0.5V_{CMOS}$+0.25	$0.5V_{CMOS}$ +0 .3	V
$V_{OL,CMOS}$	CMOS output low voltage @ $I_{OH,CMOS}$ = 1mA		0.3	V
$V_{OH,CMOS}$	CMOS output high voltage @ $I_{OH,CMOS}$ = -0.25mA	V_{CMOS}-0.3		V
I_{REF}	V_{REF} current @ $V_{REF,MAX}$	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	µA
$I_{SCK,CMD}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10 x no. RDRAMs[a]	10 x no. RDRAMs[a]	µA
$I_{SIN,SOUT}$	CMOS input leakage current @ ($0 \le V_{CMOS} \le V_{DD}$)	-10.0	10.0	µA

Table 6: SO-RIMM MODULE CAPACITY

SO-RIMM Module Capacity:	128/144 MB	96/108 MB	64/72 MB	32/36 MB	16/18 MB
Number of 128Mb or 144 Mb RDRAM devices:	8	6	4	2	1

Table 7: AC Electrical Specifications

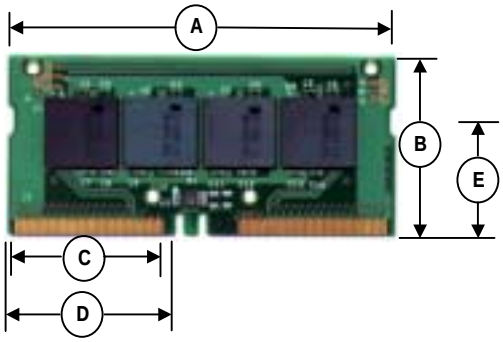
Symbol	Parameter and Conditions	Min	Typ	Max	Units
Z	Module Impedance (RSL).	25.2	28	30.8	Ω
	Module Impedance (CMOS).	23.8	28	32.2	Ω
T_{PD}	Propagation delay, all RSL signals[a].	-		See Table [b]	ns
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD}[c,d] for 4 device modules.	-21		21	ps
	Propagation delay variation of RSL signals with respect to T_{PD}[c,d] for 8 device modules.	-24		21	ps
$\Delta T_{PD-CMOS}$	Propagation Delay variation of SCK and CMD signals with respect to an average clock delay [c].	-100		100	ps
V_{α}/V_{IN}	Attenuation Limit.			See Table [b]	%
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time @20-80%).			See Table [b]	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time @20-80%).			See Table [b]	%

a. Average clock delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).
b. Table 8 lists parameters and specifications for different storage capacity SO-RIMM Modules that use 128Mb or 144Mb RDRAM devices.
c. T_{PD} or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).
d. If the SO-RIMM module meets the following specification, then it is compliant to the specification.

Table 8: AC Electrical Specifications for SO-RIMM Module

Symbol	SO-RIMM Module Capacity		128/ 144MB	64/72 MB	Units
	Number of 128/144 Mb RDRAMs:		8	4	
	Parameter and Condition for SO-RIMM modules	Freq.	Max	Max	
T_{PD}	Propagation Delay, all RSL signals.	-800	1.320	1.060	ns
		-711	1.320	1.060	ns
		-600	1.320	1.060	ns
V_{α}/V_{IN}	Attenuation Limit.	-800	16	12	%
		-711	16	12	%
		-600	10	8	%
V_{XF}/V_{IN}	Forward crosstalk coefficient (300ps input rise time @20-80%).	-800	4	2	%
		-711	4	2	%
		-600	4	2	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (300ps input rise time @20-80%).	-800	2.0	1.5	%
		-711	2.0	1.5	%
		-600	2.0	1.5	%
R_{DC}	DC Resistance.	-800	1.4	0.9	Ω
		-711	1.4	0.9	Ω
		-600	1.4	0.9	Ω

Figure 3: Physical Dimension



Dimension	Description	Min	Nom	Max	Unit
A	PCB length	67.45 2.656	67.60 2.661	67.75 2.667	mm in
B	PCB height	31.10 1.224	31.25 1.230	31.40 1.236	mm in
C	Center-center pad width from pad A1 to A40, A41 to A80, B1 to B40 or B41 to B80		25.35 0.998		mm in
D	Spacing from PCB left edge to center of connector left key notch		30.00 1.181		mm in
E	Spacing from bottom PCB edge to center of side edge retainer notch		20.00 0.787		mm in
F	PCB thickness	0.90 0.035	1.00 0.039	1.10 0.043	mm in
G	Heat spreader thickness from PCB surface (one side) to heat spreader top surface		3.50 0.138		mm in

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