Processing Signals At Increased Sample Rates With Multiple HSP45116's

It is possible to generate signals with sample rates higher than the rated speed of the HSP45116 Numerically Controlled Oscillator/Modulator by using two parts. Each NCOM is clocked at half the sample rate of the signal to be generated, and the frequency of each is set to half the desired frequency. The phase register of one NCOM is then set to offset the phase of its output by one half of a sample period. The vector inputs and outputs of the two parts are then multiplexed together to form a signal at twice the frequency that would normally be possible; see Figure 1.

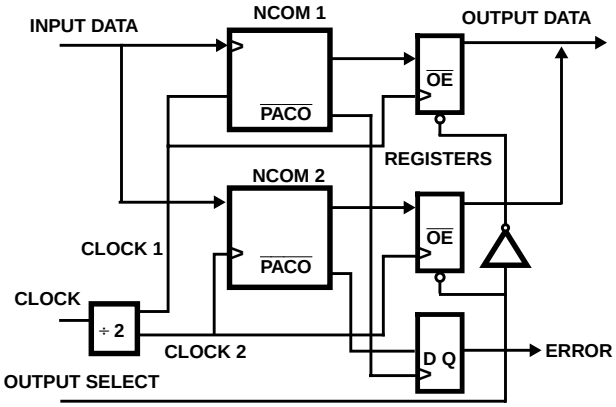

FIGURE 1. CIRCUIT BLOCK DIAGRAM

The value to be put into the phase register is one half of the sum of the center and offset frequency registers. This means that the phase offset between the two NCOMs is limited to the 16 bit resolution of the phase register, which limits the frequency resolution of the complete circuit to 15 bits.

The proper operation of this circuit can be verified by observing the $\overline{\text{PACO}}$ outputs of the two NCOMs. Since $\overline{\text{PACO}}$ is the inverted output of the phase accumulator and the phase offset is added to the output of the phase accumulator register, the alignment of the $\overline{\text{PACO}}$ pulses out of the two parts will not be affected by phase offsets (see HSP45116 Data Sheet, Figure 1). The timing of the $\overline{\text{PACO}}$ pulses is shown in Figure 2. The flip flop connected to the $\overline{\text{PACO}}$ outputs of NCOM 1 and NCOM 2 as shown in Figure 1 will detect an error in this alignment. Note that the only causes for $\overline{\text{PACO}}$ misalignment are improper configuration of the NCOMs or circuit noise which is severe enough to cause the parts to false trigger. Should the error signal go active, there will most likely be a problem with the entire circuit.

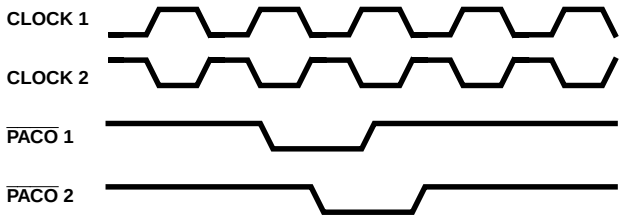

FIGURE 2. $\overline{\text{PACO}}$ TIMING

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