

When multiple correlators are cascaded for longer reference data sets, the Programmable Delay is used to adjust the timing between chips so that they can be connected with no external hardware. Figure 1 shows the portions of two correlators that would be active when two 45256's are set up to perform a 1 bit, 512 tap correlation. In this case, DOUT7 of one correlator is connected to DIN7 of the next one; CASOUT0-12 of the first part are connected to CASIN0-12 of the second one. (See the HSP45256 Data Sheet). Figure 2 shows the relevant portions of two Correlators which are

cascaded together; in this example, each is configured as 1x256. In the interest of clarity, the only portions shown are the final stage of the first correlator and the first stage of the second one. The data sample number at each stage for a given clock cycle is shown in the boxed in numbers. Note that the Programmable Delay of the first part is set to a delay of one (the minimum possible) and the second part is set to a delay of two. This assures that the proper samples are added in the Cascade Summer.

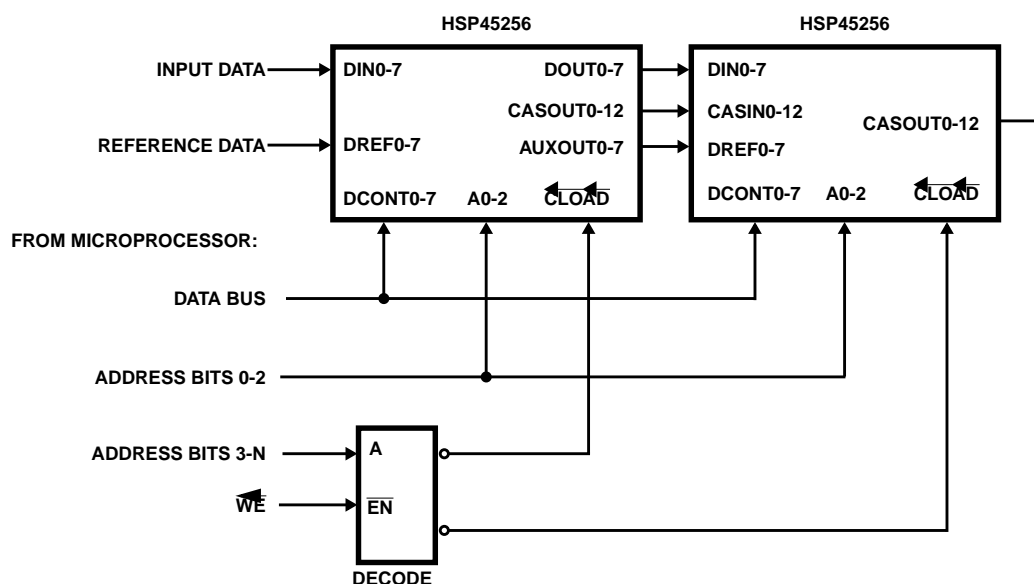


FIGURE 1. CIRCUIT BLOCK DIAGRAM

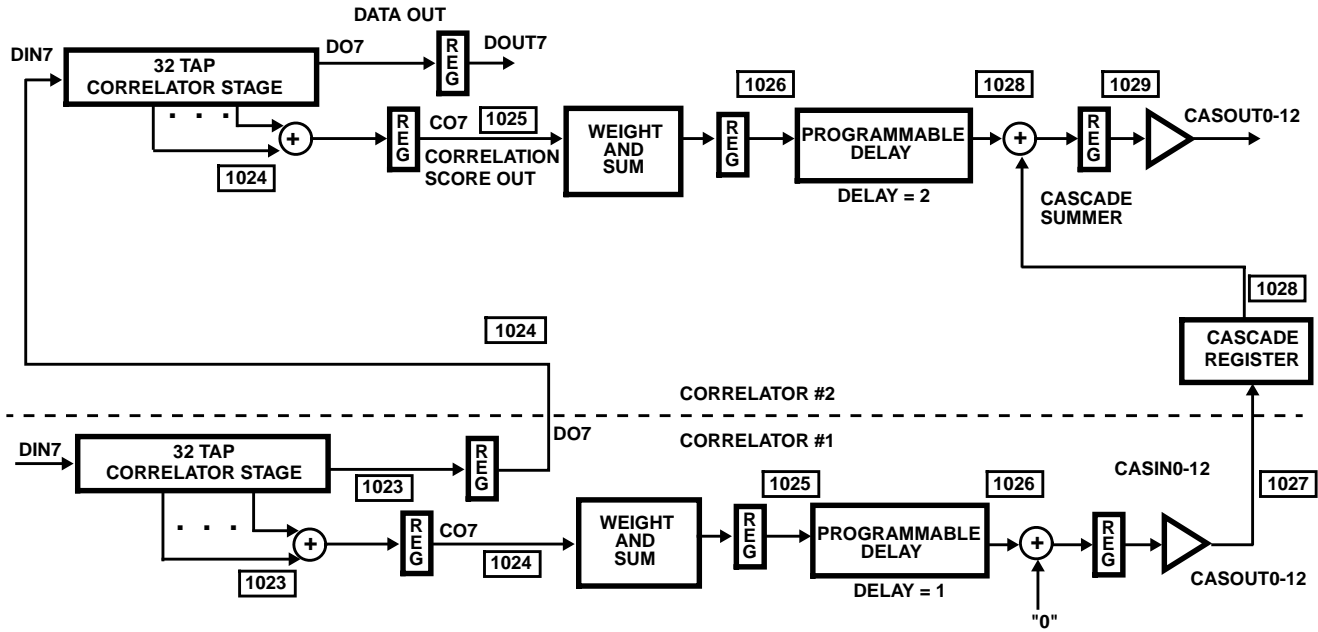


FIGURE 2. CASCADED CORRELATORS SHOWING RELATIVE CLOCK CYCLES

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