



## HW3000M/HW2000 *Home Wire*™ Home Phoneline Networking Physical Layer

### PHY Features

- Highly integrated home phoneline networking physical layer (PHY) solution with 802.3u-compatible media independent interface (MII):
  - HW3000M *HomePNA*\* PHY
  - HW2000 analog front end (AFE)
- Ideally suited for applications requiring add-on *HomePNA* functionality:
  - USB-*HomePNA* adapters
  - PC motherboards
- Support for the *HomePNA* Interface Specification 2.0:
  - Adaptive rate selection: 1 Mbit/s to 16 Mbits/s
  - Packet buffering, collision detection, and retransmission logic adhere to *HomePNA* 2.0 medium-specific demands
- Compliant with *HomePNA* PHY Specification 1.1:
  - Integrated 1 Mbit/s PHY on the HW3000M.
  - Automatically selects between *HomePNA* Revision 1.1/2.0 modulation and protocol based on capabilities of partner station on the network
- Support for multimedia and real-time applications using priority-based queuing quality of service (QoS):
  - Implements eight levels of packet priority
- Host configuration and status monitoring entirely through an MDIO/MDC interface
- Intelligent power management capabilities:
  - Disable Tx and Rx logic under idle conditions
- Support for various loopback test modes, including loopback test at the digital interface to the integrated *HomePNA* 1.1 PHY
- Compatible with existing services:
  - Voice
  - V.90 and emerging V.92 analog modes
  - G.Lite splitterless DSL (G.992.2)
  - Full-rate DSL (G.992.1)
  - ISDN

- Highly integrated HW2000 AFE:
  - Support for all *HomePNA* 2.0 front-end transmit and receive operations
  - Minimal additional components required
  - 10-bit ADC and DAC
  - Integrated crystal oscillator: 28 MHz fundamental mode crystal
  - On-chip filtering
- Low-power, 3.3 V, 0.20  $\mu$ m technology
- 100-pin TQFP

### Media Independent Interface

- *IEEE*† 802.3u-compatible media independent interface (MII):
  - Enhanced mode operation on MII
  - Direct connection to external media access controllers (MACs)
  - Support for universal serial bus (USB)-local area network (LAN) controllers
- Provides 24 MHz  $\pm$  5% Tx and Rx clocks to the external system MAC

### Additional Chip Set Features

- LED support:
  - Link activity
  - Rx activity
  - Tx activity
  - Collision detect
  - Carrier sense
- *IEEE* 1149.1 compliant JTAG test access port

\* *HomePNA* is an acronym for Home Phoneline Networking Alliance. It is a trademark of HomePNA, Inc.

† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

## **Description**

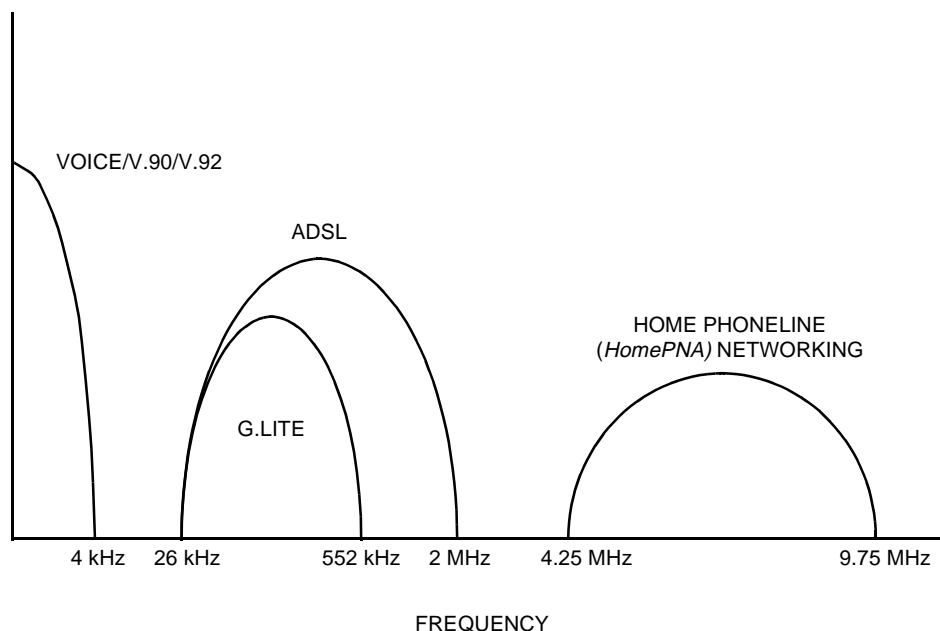
The Lucent Technologies Microelectronics Group's HW3000M/HW2000 *Home Wire* PHY is a highly integrated solution designed to quickly add high-speed networking over existing, residential telephone wiring to existing products, such as 10/100 Mb/s Ethernet designs. The *Home Wire* PHY provides a direct connection to an external *IEEE* 802.3 MAC or to a USB-to-Ethernet controller through its *IEEE* 802.3u-compatible MII. The *Home Wire* PHY provides automatic rate adaptation, instantaneously adjusting to the changing electrical characteristics of the home phoneline communications channel, in order to select the optimal speed which can reach a maximum of 16 Mb/s.

The two-device HW3000M/HW2000 *Home Wire* PHY fully supports the *HomePNA* Interface Specification 2.0. The *HomePNA* was formed to develop specifications for interoperable, home networked devices that use existing residential telephone wiring, regardless of the topology. The chip set is also fully compliant with the *HomePNA* PHY Specification Revision 1.1, in order to provide backwards compatibility with existing applications and home phoneline networks built around *HomePNA* 1.1 technology.

In order to provide a robust, cost-effective, and simple-to-use home phoneline networking solution, the *Home Wire* PHY is compatible with the existing *IEEE* 802.3u MII specification. Up to 25 PCs, peripherals, or network devices can be installed on a single home phoneline network that can span up to 1000 feet between the two farthest points.

The HW3000M/HW2000 *Home Wire* PHY is fully compatible with existing phone services such as voice, facsimile, V.90/V.92 modem connections, ISDN voice and data, ADSL, and G.Lite. Products based on the *Home Wire* PHY will not compromise or interrupt any of these services. Frequency division multiplexing (FDM) technology is used to simultaneously support existing and emerging telephone services along with networked *HomePNA* data traffic. The frequency ranges for *HomePNA* based products have been carefully selected to avoid interference from these various services that may be encountered in a typical home. As shown in Figure 1, signals from the *Home Wire* PHY are centered at 7 MHz, with the signal ranging from 4.25 MHz to 9.75 MHz. This frequency range is well above the frequencies used for existing phone services.

## Description (continued)



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**Figure 1. *Home Wire* PHY Compatibility with Existing Service**

The *Home Wire* PHY-based designs unleash the power of networking in the home by enabling a host of applications, allowing users to maximize their investment in peripheral devices, and take full advantage of existing narrowband or future broadband connections. The *Home Wire* PHY supports multimedia and real-time applications using priority-based queuing to ensure quality of service (QoS), enabling such applications as voice and video over IP in the home. The embedded *Home Wire* PHY provides the core technology for the following:

- Internet connection sharing
- Peripheral sharing (i.e., printers, scanners, etc.)
- File and application sharing
- Entertainment (i.e., multiplayer gaming)
- Home automation

- IP telephony
- Video over IP
- PC-to-PC intercom
- Residential gateways

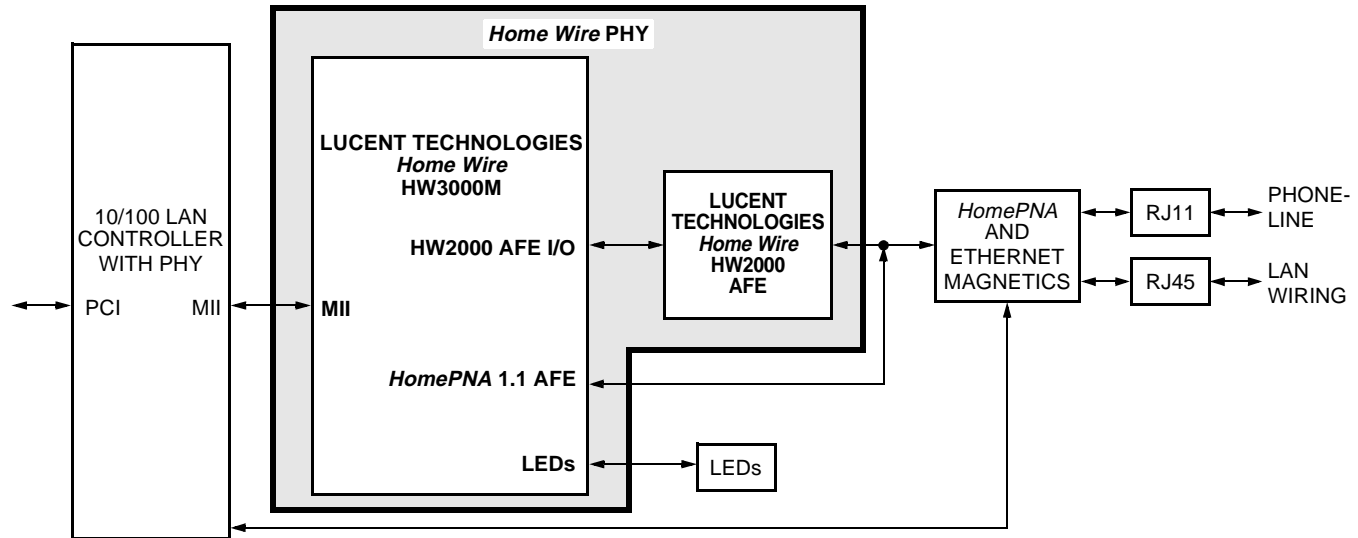
The *Home Wire* PHY is designed to support the rapid proliferation of *HomePNA* 2.0 technology into various embedded products and PCs that support an existing *IEEE* 802.3 MAC.

The *Home Wire* PHY will enable quick deployment of products such as combination LAN and *HomePNA* 2.0, which will allow a laptop user to take advantage of the office 10/100Base-T network and the residential home phoneline network. For users who do not want to install a card in their PC, a USB-*HomePNA* adapter powered by the *Home Wire* PHY is the ideal product.

## Functional Description

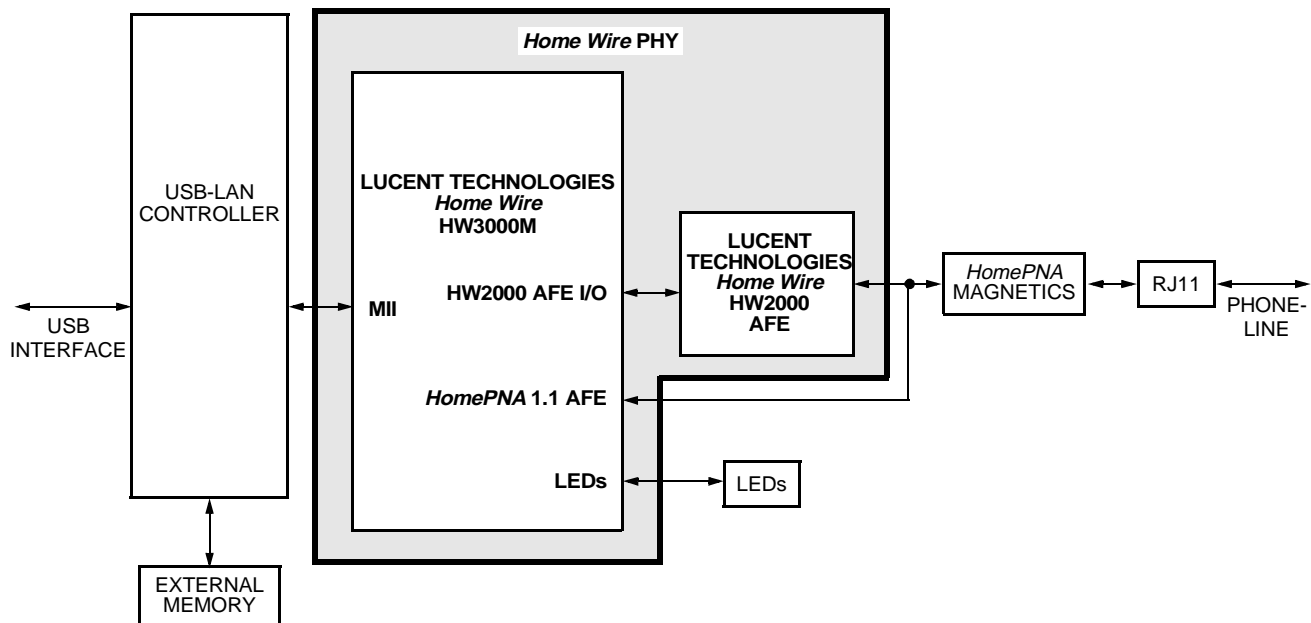
The HW3000M *Home Wire* PHY has been designed so that customers can add *HomePNA* 2.0 functionality to their existing motherboard and other products quickly and cost-effectively. The HW3000M serves as a transceiver that modulates/demodulates baseband network traffic to/from an *IEEE* 802.3 MAC to meet the signaling requirements set forth in the *HomePNA* 2.0 standard. On the host side, the HW3000M connects to an 802.3-compliant MAC via an MII. On the network side, it connects to the HW2000 AFE using a pair of high-speed parallel buses.

Figure 2 is a block diagram of a 10/100 LAN-based product with *HomePNA* 2.0 functionality provided by the *Home Wire* PHY. Figure 3 is a block diagram of a USB-*HomePNA* adapter using the *Home Wire* PHY.



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Figure 2. 10/100 LAN Adapter with *Home Wire* PHY System Block Diagram



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Figure 3. USB-*HomePNA* 2.0 Adapter with *Home Wire* PHY System Block Diagram

## Functional Description (continued)

### HW2000 AFE Interface

The HW3000M supports a 17-pin interface to the HW2000 AFE. The interface consists of a two-phase, multiplexed data converter interface with control logic used to control the positioning of the MSB of the data as well as the internal gain or attenuation of the HW2000 receiver and transmitter paths.

### Integrated *HomePNA* 1.1 PHY

In order to provide backwards compatibility with existing applications and home phoneline networks based on *HomePNA* 1.1 technology, the HW3000M supports an on-chip *HomePNA* 1.1 PHY.

The HW3000M supports a 4-pin 1M8 interface from the integrated PHY port to the external resistive hybrid.

### Media Independent Interface (MII)

The HW3000M supports an *IEEE* 802.3u-compatible MII that provides direct connection to external *IEEE* 802.3 MACs and other devices that support an MII, including PC motherboard chip sets and USB-Ethernet LAN controllers.

The HW3000M provides a 24 MHz  $\pm$  5% Tx and Rx clock to the external controller.

### JTAG Interface

The HW3000M supports an *IEEE* 1149.1 compliant JTAG boundary-scan test access port interface.

## HW2000 Overview

The HW2000 is the analog front-end for the HW3000M and provides the *HomePNA* 2.0 line interface functionality. The HW2000 is composed of the following functional blocks:

- Integrated crystal oscillator
- 10-bit ADC and DAC
- Variable gain amplifiers
- Line drivers
- Filtering

Only minimal additional components (i.e., resistive hybrid, magnetics) are required to implement the *HomePNA* 2.0 line interface functionality.

## *Home Wire* PHY: Support Tools

The primary HW3000M/HW2000 *Home Wire* PHY evaluation tool is the HW3000M/HW2000 *Home Wire* PHY evaluation module. This module is a complete *HomePNA* 2.0 transceiver with a standard MII connector. The module consists of a small form factor PCB with the *Home Wire* PHY, magnetics, dual RJII connector, MII connector, and voltage regulator. The *Home Wire* PHY module can be easily connected to a target system for quick evaluation of this mode of operation.

## Home Wire Chip Set Product Family Overview

Table 1. Product Feature Matrix

Feature	HW3130	HW3100	HW3000S	HW3000M
PCI Interface, Revision 2.2	✓	✓	—	—
Host-Controlled Modem Interface	✓	✓	—	—
Microprocessor-Slave Interface	—	—	✓	—
MII	✓	—	—	✓
Serial EEPROM Interface	✓	✓	✓	—
LED Interface	✓	✓	✓	✓
Integrated <i>HomePNA</i> Revision 1.1 PHY	✓	✓	✓	✓
HW2000 <i>HomePNA</i> 2.0 AFE Interface	✓	✓	✓	✓
Device Package	160-pin MQFP	144-pin TQFP	100-pin TQFP	100-pin TQFP

Key:

✓: Supported.

—: Not supported.

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