DESCRIPTION

The HY62V16100-(I)/HY62U16100-(I) is a high-speed, low power and 1M bits CMOS SRAM organized as 65,536 words by 16 bits. The HY62V16100-(I)/ HY62U16100-(I) uses sixteen common input and output lines and has an output enable pin which operates faster than address access time at a read cycle. The device is fabricated using HYUNDAI's advanced CMOS process and designed with high-speed low power circuit technology. It is particulary well suited for being used in high-density and low power system applications.

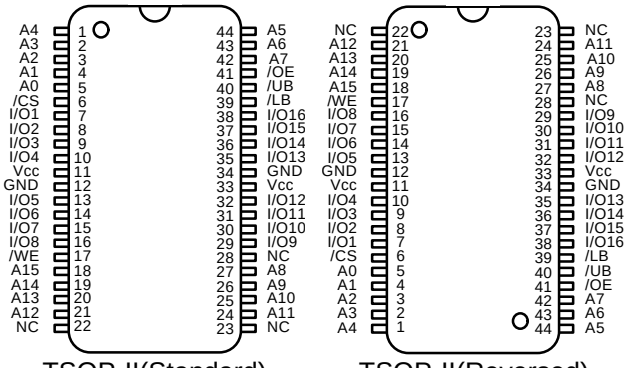
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Data Byte Control
  - LB : I/O1 ~ I/O8, UB : I/O9 ~ I/O16
- Battery backup(L/LL-part)
  - 2.0V(min) data retention
- Standard pin configuration
  - 44pin 400mil TSOP-II
    (Standard and Reversed)

Product No.	Supply Voltage(V)	Speed (ns)	Operation Current(mA)	Standby Current(uA)		Temperature. (°C)
				L	LL	
HY62V16100	3.3	85/100/120	5	50	10	0~70(Normal)
HY62V16100-I	3.3	85/100/120	5	50	15	-40~85(E.T.)
HY62U16100	3.0	100/120/150	5	50	10	0~70(Normal)
HY62U16100-I	3.0	100/120/150	5	50	10	-40~85(E.T.)

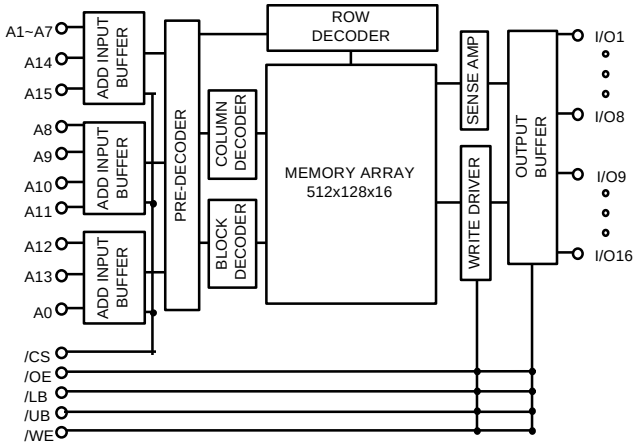
Note 1. E.T. : Extended Temperature, Normal : Normal Temperature
2. Current value is max.

PIN CONNECTION



TSOP-II(Standard) TSOP-II(Reversed)

BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Funtion	Pin Name	Pin Funtion
/CS	Chip Select	I/O1~I/O16	Data Input/Output
/WE	Write Enable	A0~A15	Address Input
/OE	Output Enable	Vcc	Power(3.3V/3.0V)
/LB	Low Byte Control(I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control(I/O9~I/O16)	NC	No Connection

ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62V16100LT2	85/100/120	L-part		TSOP-II Standard
HY62V16100LLT2	85/100/120	LL-part		TSOP-II Standard
HY62V16100LR2	85/100/120	L-part		TSOP-II Reversed
HY62V16100LLR2	85/100/120	LL-part		TSOP-II Reversed
HY62V16100LT2-I	85/100/120	L-part	E.T.	TSOP-II Standard
HY62V16100LLT2-I	85/100/120	LL-part	E.T.	TSOP-II Standard
HY62V16100LR2-I	85/100/120	L-part	E.T.	TSOP-II Reversed
HY62V16100LLR2-I	85/100/120	LL-part	E.T.	TSOP-II Reversed
HY62U16100LT2	100/120/150	L-part		TSOP-II Standard
HY62U16100LLT2	100/120/150	LL-part		TSOP-II Standard
HY62U16100LR2	100/120/150	L-part		TSOP-II Reversed
HY62U16100LLR2	100/120/150	LL-part		TSOP-II Reversed
HY62U16100LT2-I	100/120/150	L-part	E.T.	TSOP-II Standard
HY62U16100LLT2-I	100/120/150	LL-part	E.T.	TSOP-II Standard
HY62U16100LR2-I	100/120/150	L-part	E.T.	TSOP-II Reversed
HY62U16100LLR2-I	100/120/150	LL-part	E.T.	TSOP-II Reversed

Note 1. E.T. : Extended Temperature, Blank : Normal Temperature

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	-0.3 to 4.6	V	
T_A	Operating Temperature	0 to 70	°C	HY62V16100
				HY62U16100
		-40 to 85	°C	HY62V16100-I
				HY62U16100-I
T_{STG}	Storage Temperature	-65 to 125	°C	
P_D	Power Dissipation	1.0	W	
I_{OUT}	Data Output Current	50	mA	
T_{SOLDER}	Lead Soldering Temperature & Time	260 • 10	°C•sec	

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliablity.

RECOMMENDED DC OPERATING CONDITION

T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.)

Symbol	Parameter	Product	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	HY62V16100-(I)	3.0	3.3	3.6	V
		HY62U16100-(I)	2.7	3.0	3.3	V
Vss	Ground	HY62V16100-(I) HY62U16100-(I)	0	0	0	V
V_{IH}	Input High Voltage	HY62V16100-(I) HY62U16100-(I)	2.2	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	HY62V16100-(I) HY62U16100-(I)	-0.3	-	0.4	V

TRUTH TABLE

/CS	/WE	/OE	/LB	/UB	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X	X	X	Not Selected	Hi-Z	Hi-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disabled	Hi-Z	Hi-Z	Icc
L	X	X	H	H		Hi-Z	Hi-Z	
L	H	L	L	H	Read	D_{OUT}	Hi-Z	Icc
			H	L		Hi-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	Hi-Z	Icc
			H	L		Hi-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

Note:
1. H=V_{IH}, L=V_{IL}, X=don't care
2. UB, LB(Upper, Lower Byte enable)
   These active LOW inputs allow indiviual bytes to be written or read.
   When LB is LOW, data is written or read to the lower byte, I/O1 -I/O8.
   When UB is LOW, data is written or read to the Upper byte, I/O9 -I/O16.

DC ELECTRICAL CHARACTERISTICS

Vcc = 3.3V ± 10%/3.0V ±10%, T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.), unless otherwise specified

Symbol	Parameter		Test Condition		Min	Typ	Max	Unit
I_{LI}	Input Leakage Current		Vss ≤ V_{IN} ≤ Vcc		-1	-	1	uA
I_{LO}	Output Leakage Current		Vss ≤ V_{OUT} ≤ Vcc, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL} or /UB = V_{IH} or /LB = V_{IH}		-1	-	1	uA
Icc	Operating Power Supply Current		/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL} $I_{I/O}$ = 0mA		-	-	5	mA
I_{CC1}	Average Operating Current		/CS = V_{IL}, Min Duty Cycle = 100% $I_{I/O}$ = 0mA		-	-	50	mA
I_{SB}	TTL Standby Current (TTL Input)		/CS = V_{IH}		-	-	0.5	mA
I_{SB1}	Standby Current (CMOS Input)	HY62V16100	/CS = Vcc – 0.2V	L	-	-	50	uA
				LL	-	-	10	uA
		HY62V16100-I		L			50	uA
				LL	-	-	15	uA
		HY62U16100		L	-	-	50	uA
				LL	-	-	10	uA
		HY62U16100-I		L	-	-	50	uA
				LL	-	-	10	uA
V_{OL}	Output Low Voltage		I_{OL} = 2.1mA		-	-	0.4	V
V_{OH}	Output High Voltage		I_{OH} = -1mA		2.2	-	-	V

Note : Typical values are at Vcc = 3.3V/3.0V, T_A = 25°C

AC CHARACTERISTICS(I)

Vcc = 3.3V ± 10%, T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.), unless otherwise specified

#	Symbol	Parameter	-85		-10		-12		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	tRC	Read Cycle Time	85	-	100	-	120	-	ns
2	tAA	Address Access Time	-	85	-	100	-	120	ns
3	tACS	Chip Select Access Time	-	85	-	100	-	120	ns
4	tOE	Output Enable to Output Valid	-	45	-	50	-	60	ns
5	tBA	/LB, /UB Access Time	-	45	-	50	-	60	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
7	tOLZ	Output Enable to Output in Low Z	10	-	10	-	10	-	ns
8	tBLZ	/LB. /UB Enable to Output in Low Z	10	-	10	-	10	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	30	0	40	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	30	0	40	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	30	0	40	ns
12	tOH	Output Hold from Address Change	20	-	20	-	20	-	ns
	WRITE CYCLE								
13	tWC	Write Cycle Time	85	-	100	-	120	-	ns
14	tCW	Chip Selection to End of Write	70	-	80	-	100	-	ns
15	tAW	Address Valid to End of Write	70	-	80	-	100	-	ns
16	tBW	/LB, /UB Valid to End of Write	70	-	80	-	100	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	55	-	70	-	85	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	30	0	30	0	40	ns
21	tDW	Data to Write Time Overlap	35	-	40	-	50	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	10	-	10	-	10	-	ns

AC CHARACTERISTICS(II)

Vcc = 3.0V ± 10%, T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.), unless otherwise specified

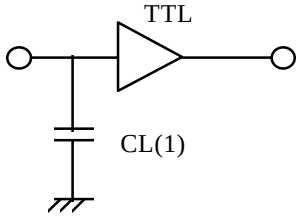
#	Symbol	Parameter	-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	TRC	Read Cycle Time	100	-	120	-	150	-	ns
2	TAA	Address Access Time	-	100	-	120	-	150	ns
3	TACS	Chip Select Access Time	-	100	-	120	-	150	ns
4	tOE	Output Enable to Output Valid	-	50	-	60	-	75	ns
5	tBA	/LB, /UB Access Time	-	50	-	60	-	75	ns
6	tCLZ	Chip Select to Output in Low Z	10	-	10	-	10	-	ns
7	tOLZ	Output Enable to Output in Low Z	10	-	10	-	10	-	ns
8	tBLZ	/LB. /UB Enable to Output in Low Z	10	-	10	-	10	-	ns
9	tCHZ	Chip Deselection to Output in High Z	0	30	0	40	0	50	ns
10	tOHZ	Out Disable to Output in High Z	0	30	0	40	0	50	ns
11	tBHZ	/LB, /UB Disable to Output in High Z	0	30	0	40	0	50	ns
12	tOH	Output Hold from Address Change	20	-	20	-	20	-	ns
	WRITE CYCLE								
13	tWC	Write Cycle Time	100	-	120	-	150	-	ns
14	tCW	Chip Selection to End of Write	80	-	100	-	120	-	ns
15	tAW	Address Valid to End of Write	80	-	100	-	120	-	ns
16	tBW	/LB, /UB Valid to End of Write	80	-	100	-	120	-	ns
17	tAS	Address Set-up Time	0	-	0	-	0	-	ns
18	tWP	Write Pulse Width	70	-	85	-	100	-	ns
19	tWR	Write Recovery Time	0	-	0	-	0	-	ns
20	tWHZ	Write to Output in High Z	0	30	0	40	0	50	ns
21	tDW	Data to Write Time Overlap	40	-	50	-	60	-	ns
22	tDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	tOW	Output Active from End of Write	10	-	10	-	10	-	ns

AC TEST CONDITIONS

T_A = 0°C to 70°C (Normal) / -40°C to 85°C (E.T.), unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.4V to 2.2V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

AC TEST LOADS



Note : Including jig and scope capacitance

CAPACITANCE

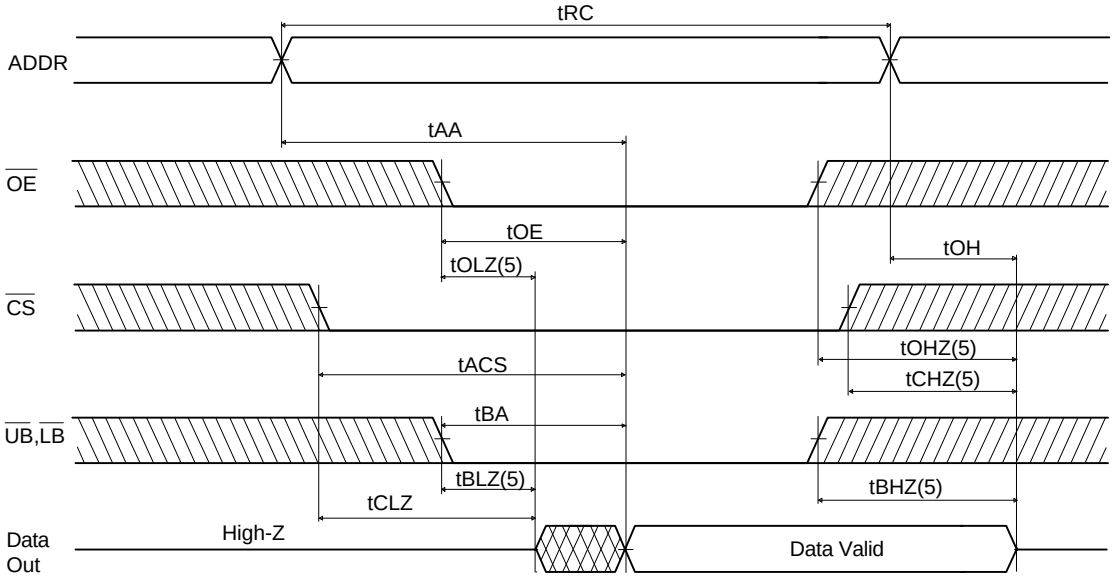
Temp = 25°C, f= 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance(ADD, /CS, /WE, /OE, /LB, /UB)	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance(I/O)	$V_{I/O}$ = 0V	8	pF

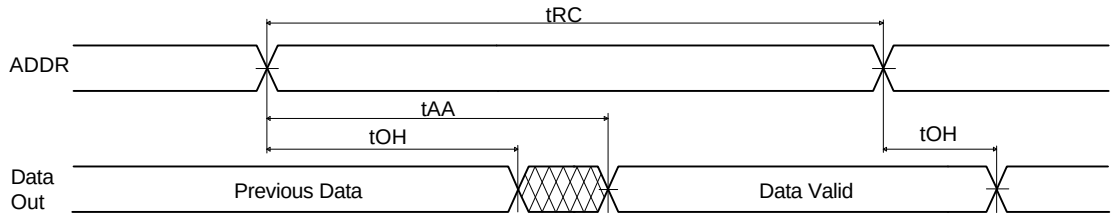
Note : This parameter is sampled and not 100% not tested

TIMING DIAGRAM

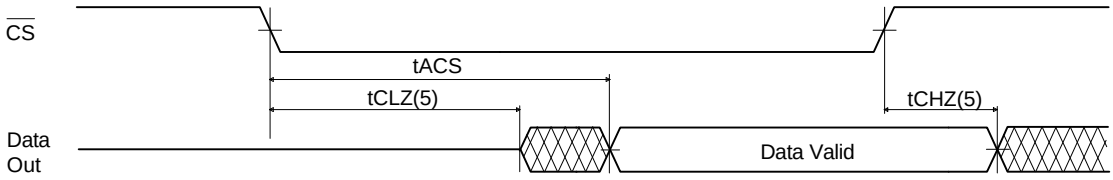
READ CYCLE 1(Note 1)



READ CYCLE 2(Note 1,2,4)

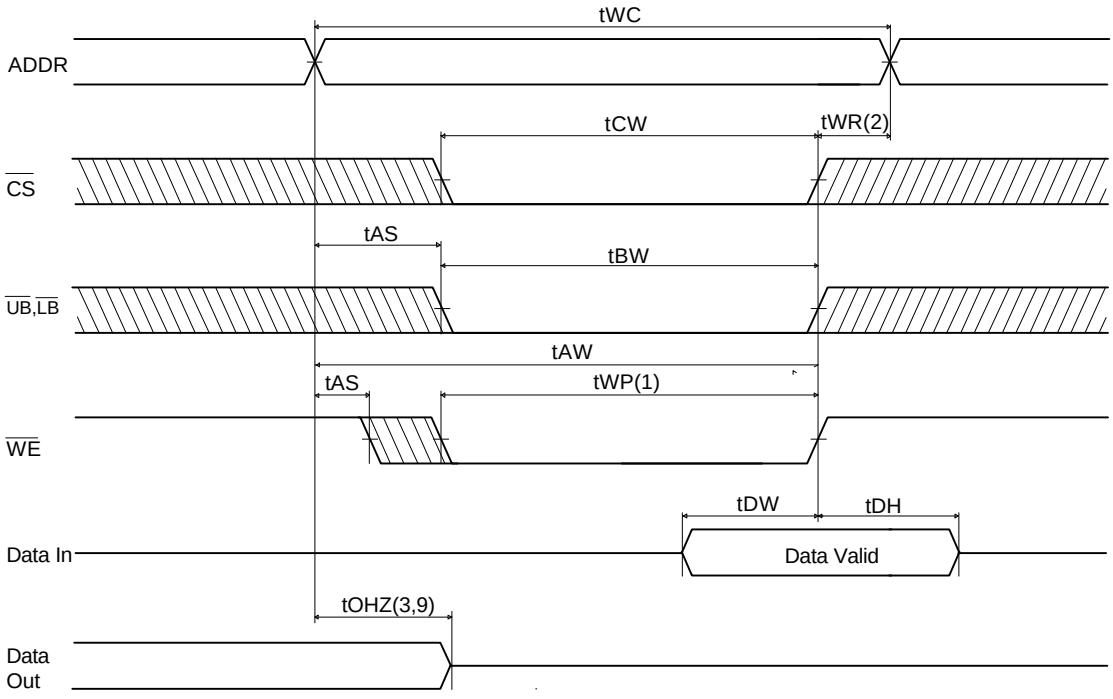


READ CYCLE 3(Note 1,3,4)

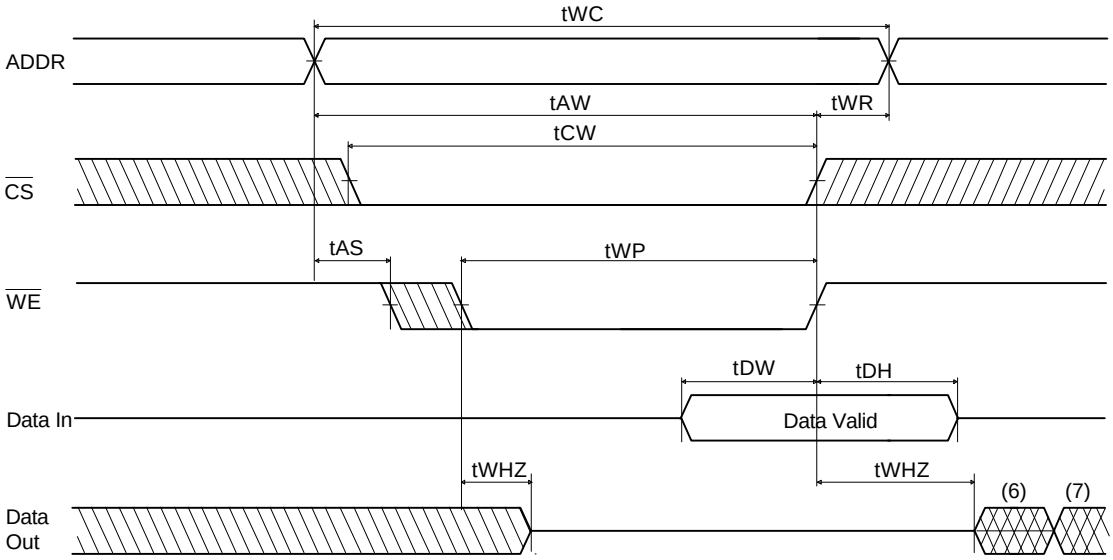


Notes:
1. /WE is high for the Read Cycle.
2. Device is continuously selected. /CS = V_{IL}
3. Address valid is prior to or coincident with /CS transition low
4. /OE = V_{IL}
5. Transition is measured + 200mV from steady state voltage.
   This parameter is sampled and not 100% tested.

WRITE CYCLE 1



WRITE CYCLE 2 (Note 5)



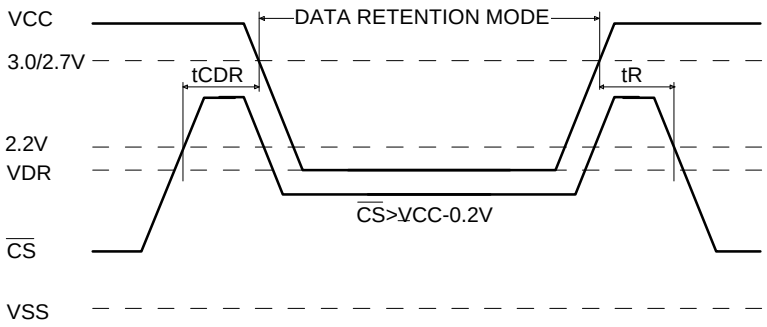
Notes:
1. A write occurs during the overlap(tWP) of a low /CS and low /WE .
2. tWR is measured from the earlier of /CS, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS, /LB and /UB low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. /OE is continuously low(/OE=V_{IL})
6. Q(data out) is the same phase with the write data of this write cycle.
7. Q(data out) is the read data of the next address.
8. If /CS is low during this period, I/O pins are in the output state.
   Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured +200mV from steady state.
   This parameter is sampled and not 100% tested.

DATA RETENTION ELECTRIC CHARATERISTIC

T_A = 0°C to 70°C (Normal)/ -40°C to 85°C (E.T.)

Symbol	Parameter		Test Condition		Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention				2	-	-	V
I_{CCDR}	Data Retention Current	HY62V16100	Vcc = 3.0V, /CS ≥ Vcc - 0.2V Vss≤V_{IN}≤Vcc	L	-	-	30	uA
				LL	-	-	10	uA
		HY62V16100-I		L	-	-	30	uA
				LL	-	-	15	uA
		HY62U16100		L	-	-	30	uA
				LL	-	-	10	uA
		HY62U16100-I		L	-	-	30	uA
				LL	-	-	15	uA
tCDR	Chip Deselect to Data Retention Time				0	-	-	ns
tR	Operating Recovery Time				5	-	-	ms

DATA RETENTION TIMING DIAGRAM



Note :
1. 3.0V : HY62V16100 and HY62V16100-I
2. 2.7V : HY62U16100 and HY62U16100-I

RELIABILITY SPEC.

TEST MODE		TEST SPEC.
ESD	HBM	≥ 2000V
	MM	≥ 250V
LATCH - UP		≤ -100mA
		≥ 100mA

PACKAGE INFORMATION

44pin 400mil Thin Small Outline Package