DESCRIPTION

The HY62UF16101 is a high speed, low power and 1M bit full CMOS SRAM organized as 65,536 words by 16bit. The HY62UF16101 uses high performance full CMOS process technology and designed for high speed low power circuit technology. It is particularly well suited for used in high density low power system application. This device has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 1.5V.

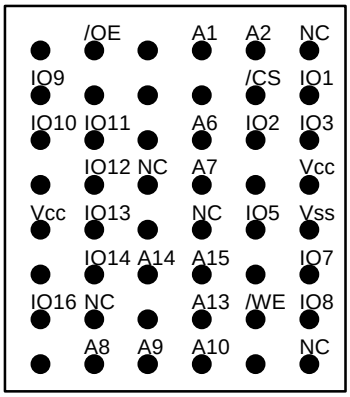
FEATURES

- Fully static operation and Tri-state output
- TTL compatible inputs and outputs
- Battery backup(LL-part)
  - 1.5V(min) data retention
- Standard pin configuration
  - 48ball uBGA

Product No.	Voltage (V)	Speed (ns)	Operation Current(mA)	Standby Current(uA) LL-part	Temperature (°C)
HY62UF16101	3.0	100/120/150	15	15	0~70(Normal)
HY62UF16101-I	3.0	100/120/150	15	15	-40~85(E.T.)

Note 1. E.T. : Extended Temperature, Normal : Normal Temperature
2. Current value is max.

PIN CONNECTION (Top View)



BLOCK DIAGRAM

PIN DESCRIPTION

Pin Name	Pin Funtion	Pin Name	Pin Funtion
/CS	Chip Select	I/O1~I/O16	Data Input/Output
/WE	Write Enable	A0~A15	Address Input
/OE	Output Enable	Vcc	Power(2.7V ~ 3.3V)
/LB	Lower Byte Control(I/O1~I/O8)	Vss	Ground
/UB	Upper Byte Control(I/O9~I/O16)	NC	No Connection

ORDERING INFORMATION

Part No.	Speed	Power	Temp.	Package
HY62UF16101LLM	100/120/150	LL-part		uBGA
HY62UF16101LLM-I	100/120/150	LL-part	E.T.	uBGA

Note 1. E.T. : Extended Temperature, Blank : Normal Temperature

ABSOLUTE MAXIMUM RATING (1)

Symbol	Parameter	Rating	Unit	Remark
V_{IN}, V_{OUT}	Input/Output Voltage	-0.2 to 3.6	V	
Vcc	Power Supply	-0.5 to 4.2	V	
T_A	Operating Temperature	0 to 70	°C	HY62UF16101
		-40 to 85	°C	HY62UF16101-I
T_{STG}	Storage Temperature	-55 to 150	°C	
P_D	Power Dissipation	1.0	W	
T_{SOLDER}	Ball Soldering Temperature & Time	260 • 10	°C • sec	

Note
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and the functional operation of the device under these or any other conditions above those indicated in the operation of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITION

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	2.7	3.0	3.3	V
Vss	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	-	Vcc+0.3	V
V_{IL}	Input Low Voltage	-0.3(1)	-	0.4	V

Note : 1. VIL = -1.5V for pulse width less than 30ns

TRUTH TABLE

/CS	/WE	/OE	/LB	/UB	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X	X	X	Not Selected	Hi-Z	Hi-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disabled	Hi-Z	Hi-Z	I_{CC}
L	X	X	H	H	Not Selected	Hi-Z	Hi-Z	I_{SB}, I_{SB1}
L	H	L	L	H	Read	D_{OUT}	Hi-Z	I_{CC1}
			H	L		Hi-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	Hi-Z	I_{CC1}
			H	L		Hi-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

Note:
1. H=V_{IH}, L=V_{IL}, X=don't care
2. UB, LB(Upper, Lower Byte enable)
   These active LOW inputs allow individual bytes to be written or read.
   When LB is LOW, data is written or read to the lower byte, I/O 1 -I/O 8.
   When UB is LOW, data is written or read to the Upper byte, I/O 9 -I/O 16.

DC ELECTRICAL CHARACTERISTICS

Vcc = 3.0V±10%, T_A = 0°C to 70°C(Normal)/ -40°C to 85°C(E.T.)

Sym	Parameter	Test Condition		Min.	Typ.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$		-1	-	1	uA
I_{LO}	Output Leakage Current	$V_{SS} \le V_{OUT} \le V_{CC}$, /CS = V_{IH} or /OE = V_{IH} or /WE = V_{IL} or /UB = V_{IH} and /LB = V_{IH}		-1	-	1	uA
I_{CC}	Operating Power Supply Current	/CS = V_{IL}, V_{IN} = V_{IH} or V_{IL}, $I_{I/O}$ = 0mA		-	8	15	mA
I_{CC1}	Average Operating Current	/CS = V_{IL}, Min Duty Cycle = 100% $I_{I/O}$ = 0mA		-	65	80	mA
I_{SB}	TTL Standby Current (TTL Input)	/CS = V_{IH} or /CS = V_{IL} or /UB, /LB = V_{IH}		-	-	1	mA
I_{SB1}	Standby Current (CMOS Input)	/CS ≥ Vcc - 0.2V or /UB, /LB ≥ Vcc - 0.2V		-	-	15	uA
V_{OL}	Output Low Voltage	Vcc = 3.0V	I_{OL} = 2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	Vcc = 3.0V	I_{OH} = -1.0mA	2.2	-	-	V

Note : Typical values are at Vcc = 3.0V

AC CHARACTERISTICS

Vcc = 3.0V±10%, T_A = 0°C to 70°C(Normal)/ -40°C to 85°C(E.T.), unless otherwise specified

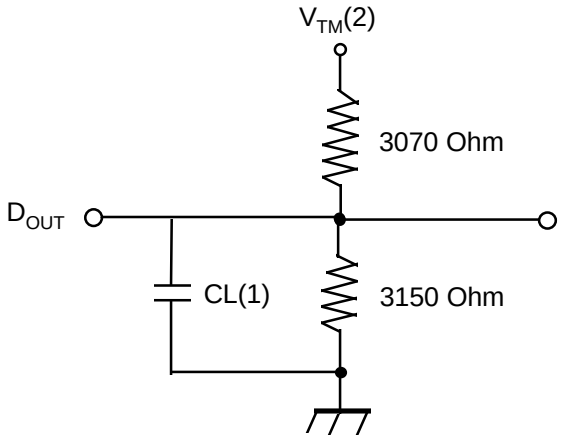
#	Symbol	Parameter	-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min	Max.	
	READ CYCLE								
1	TRC	Read Cycle Time	100	-	120	-	150	-	ns
2	TAA	Address Access Time	-	100	-	120	-	150	ns
3	TACS	Chip Select Access Time	-	100	-	120	-	150	ns
4	TOE	Output Enable to Output Valid	-	50	-	60	-	75	ns
5	TBA	/LB, /UB Access Time	-	100	-	120	-	150	ns
6	TCLZ	Chip Select to Output in Low Z	20	-	20	-	20	-	ns
7	TOLZ	Output Enable to Output in Low Z	5	-	10	-	10	-	ns
8	TBLZ	/LB, /UB Enable to Output in Low Z	10	-	10	-	10	-	ns
9	TCHZ	Chip Deselection to Output in High Z	0	30	0	40	0	50	ns
10	TOHZ	Out Disable to Output in High Z	0	30	0	40	0	50	ns
11	TBHZ	/LB, /UB Disable to Output in High Z	0	30	0	40	0	50	ns
12	TOH	Output Hold from Address Change	15	-	15	-	15	-	ns
	WRITE CYCLE								
13	TWC	Write Cycle Time	100	-	120	-	150	-	ns
14	TCW	Chip Selection to End of Write	80	-	100	-	120	-	ns
15	TAW	Address Valid to End of Write	80	-	100	-	120	-	ns
16	TBW	/LB, /UB Valid to End of Write	80	-	100	-	120	-	ns
17	TAS	Address Set-up Time	0	-	0	-	0	-	ns
18	TWP	Write Pulse Width	75	-	85	-	100	-	ns
19	TWR	Write Recovery Time	0	-	0	-	0	-	ns
20	TWHZ	Write to Output in High Z	0	35	0	40	0	50	ns
21	TDW	Data to Write Time Overlap	45	-	50	-	60	-	ns
22	TDH	Data Hold from Write Time	0	-	0	-	0	-	ns
23	TOW	Output Active from End of Write	10	-	10	-	10	-	ns

AC TEST CONDITIONS

T_A = 0°C to 70°C (Normal) / -40°C to 85°C (E.T.), unless otherwise specified

PARAMETER	Value
Input Pulse Level	0.4V to 2.0V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 100pF + 1TTL Load

AC TEST LOADS



Note
1. Including jig and scope capacitance
2. V_{TM} = 2.8V for Vcc = 3.0V : HY62UF16101-(I)

CAPACITANCE

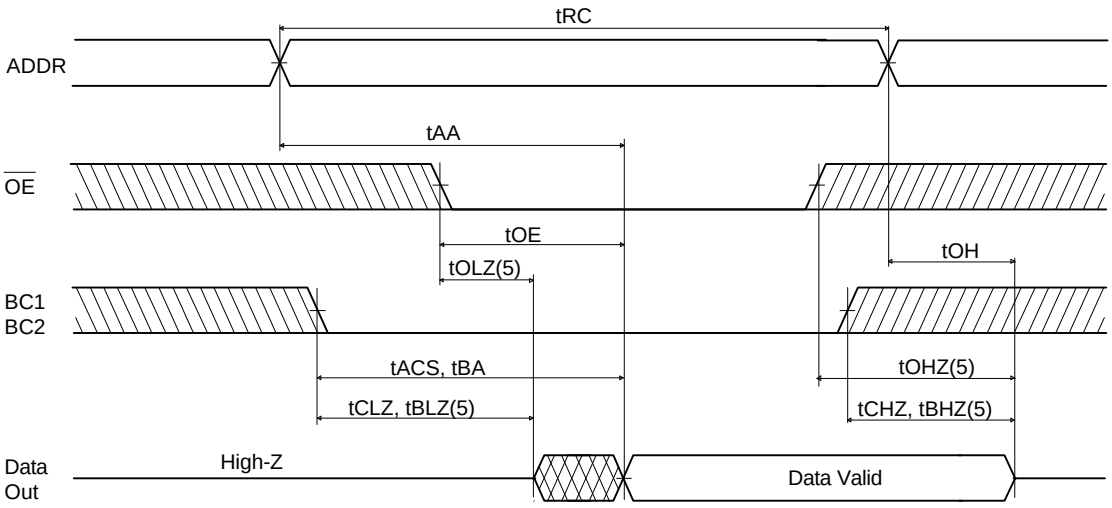
(Temp = 25°C, f= 1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance(Add, /CS, /WE, /UB, /LB, /OE)	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance(I/O)	$V_{I/O}$ = 0V	10	pF

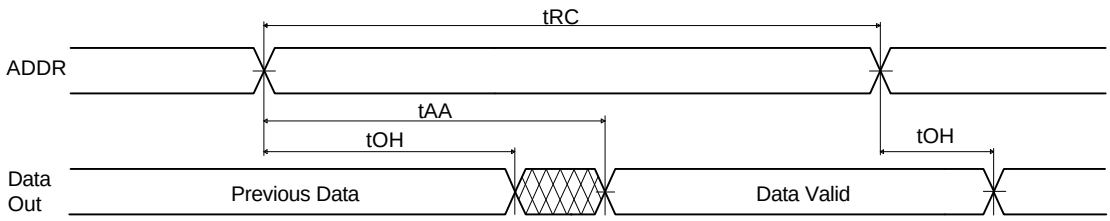
Note : These parameters are sampled and not 100% tested

TIMING DIAGRAM

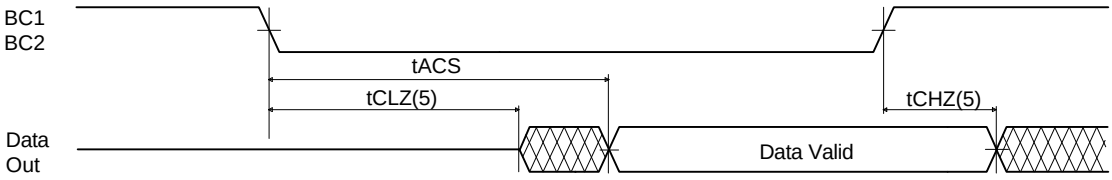
READ CYCLE 1(Note 1)



READ CYCLE 2(Note 1,2,4)

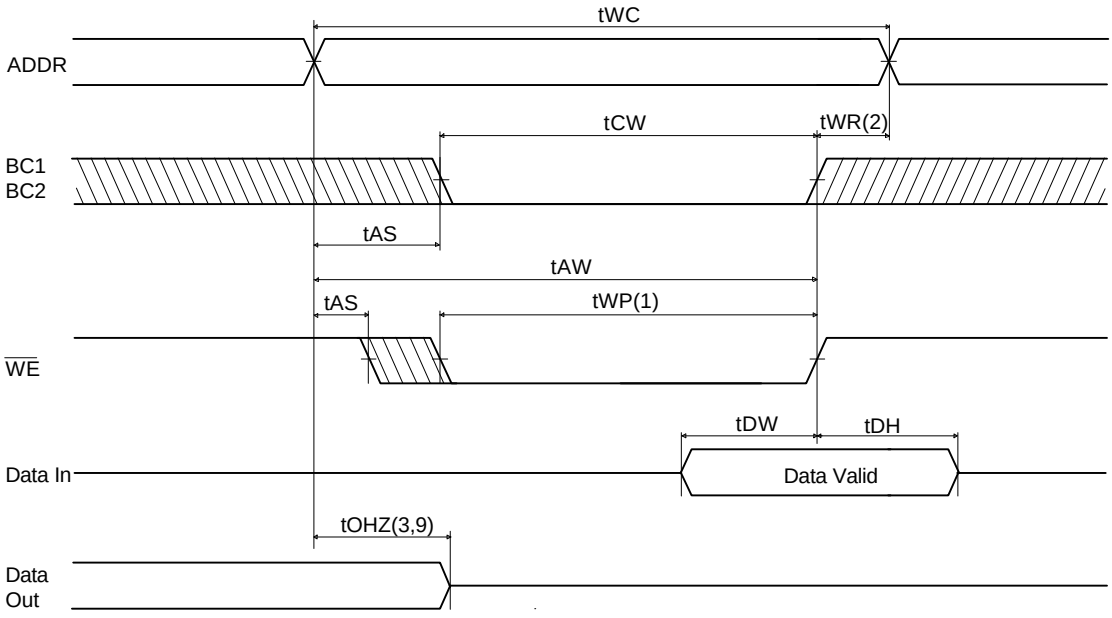


READ CYCLE 3(Note 1,3,4)

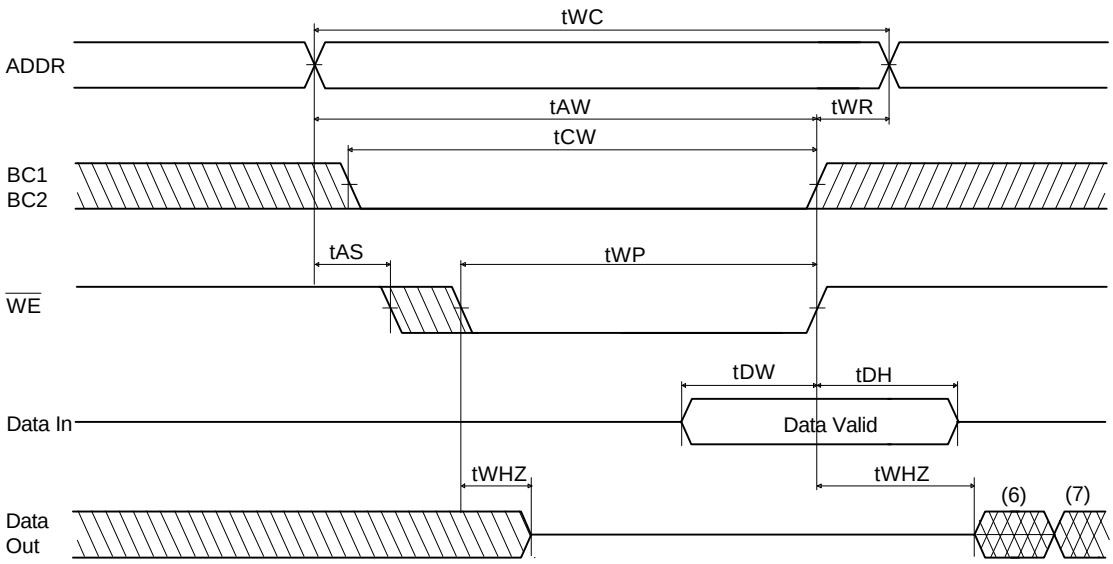


Notes:
1. Read Cycle occurs whenever a high on the /WE and /OE is low, while /UB or /LB and /CS are in active status.
2. /OE = V_{IL}
3. Transition is measured + 200mV from steady state voltage.
   This parameter is sampled and not 100% tested.
4. BC1 is high for the standby, low for active
   BC2 is high for the standby, low for active

WRITE CYCLE 1



WRITE CYCLE 2 (Note 5)



Notes:
1. A write occurs whenever a low on the /WE while /UB and/or /LB and /CS are in active state.
2. tWR is measured from the earlier of /CS, /LB, /UB, or /WE going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
4. If the /CS, /LB and /UB low transition occur simultaneously with the /WE low transition or after the /WE transition, outputs remain in a high impedance state.
5. /OE is continuously low(/OE=V_{IL})
6. Q(data out) is the same phase with the write data of this write cycle.
7. Q(data out) is the read data of the next address.
8. Transition is measured +200mV from steady state.
   This parameter is sampled and not 100% tested.
9. BC1 is high for the standby, low for active
   BC2 is high for the standby, low for active

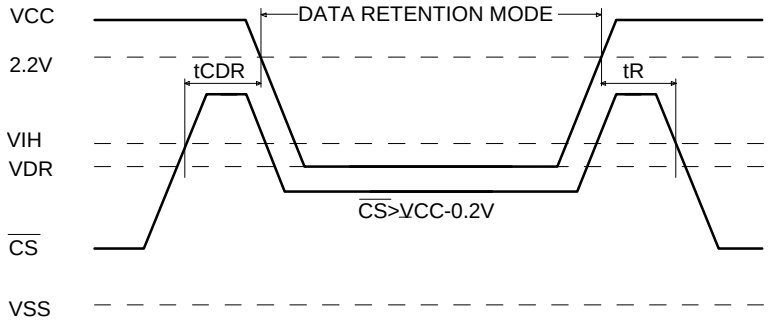
DATA RETENTION ELECTRIC CHARACTERISTIC

T_A = 0°C to 70°C (Normal)/-40°C to 85°C (E.T.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DR}	Vcc for Data Retention	/CS ≥ Vcc - 0.2V	1.5	-	3.3	V
I_{CCDR}	Data Retention Current	Vcc = 2.0V, /CS ≥ Vcc - 0.2V, Vss ≤ V_{IN} ≤ Vcc	-	-	15	uA
TCDR	Chip Deselect to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
Tr	Operating Recovery Time		tRC(2)	-	-	ns

Notes:
1. Typical values are under the condition of T_A = 25°C.
2. tRC is read cycle time.

DATA RETENTION TIMING DIAGRAM

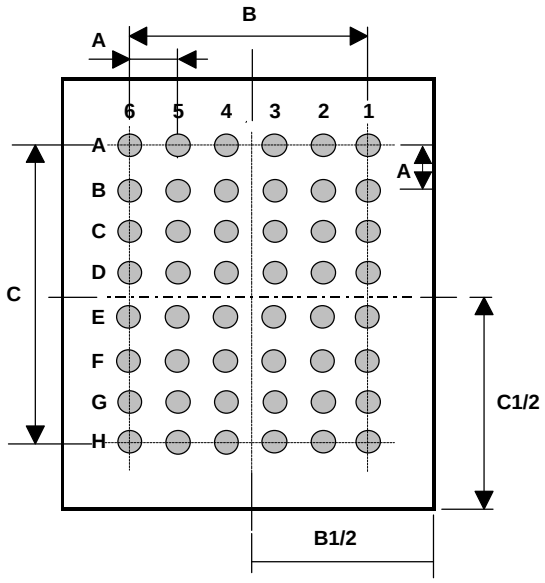


RELIABILITY SPEC.

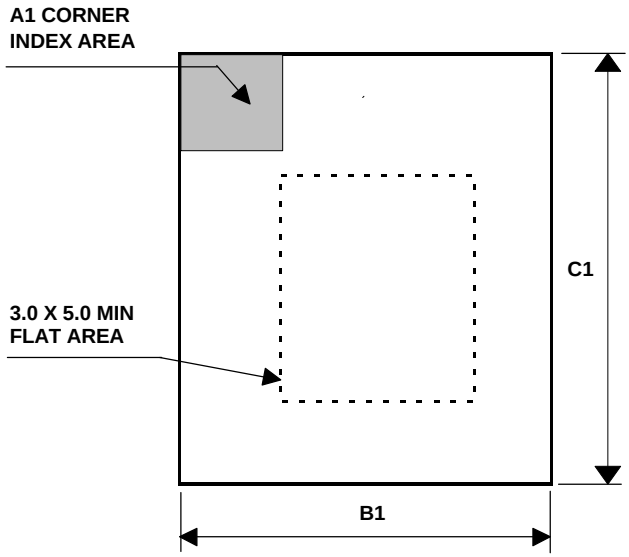
TEST MODE		TEST SPEC.
ESD	HBM	≥ 2500V
	MM	≥ 250V
LATCH – UP		≤ -200mA
		≤ 200mA

PACKAGE INFORMATION

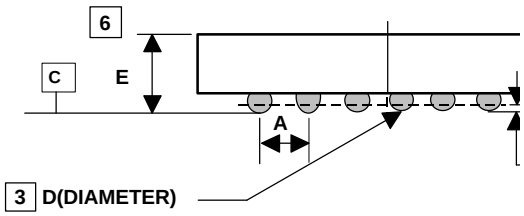
48ball Micro Ball Grid Array Package(M)



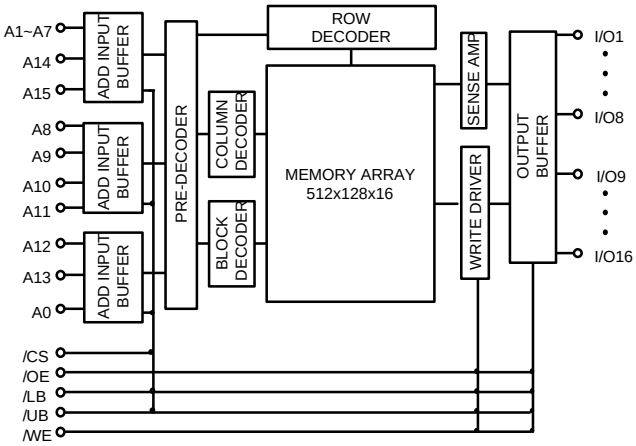
BUMP VIEW



TOP VIEW



SIDE VIEW



Symbol	Min.	Typ.	Max
A	-	0.75	-
B	-	3.75	-
B1	6.15	6.2	6.3
C	-	5.25	-
C1	6.25	6.3	6.4
D	0.3	0.35	0.4
E	0.85	0.9	0.95
E1	0.6	0.65	0.7
E2	0.2	0.25	0.3
r	-	-	0.08

ł. 5M-1994.

3. DIMENSION “D” IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

4. PRIMARY DATUM C(SEATING PLANE) IS DEFINED BY THE CROWN OF THE SOLDER BALLS.

5. SOLDER BALL ARRAY MAY BE DEPOPULATED BY OMISSION BALLS FROM A FULL MATRIX NO SHIFTING OF MATRIX PATTERN IS ALLOWED.

6. THIS IS A CONTROLLING DIMENSION.